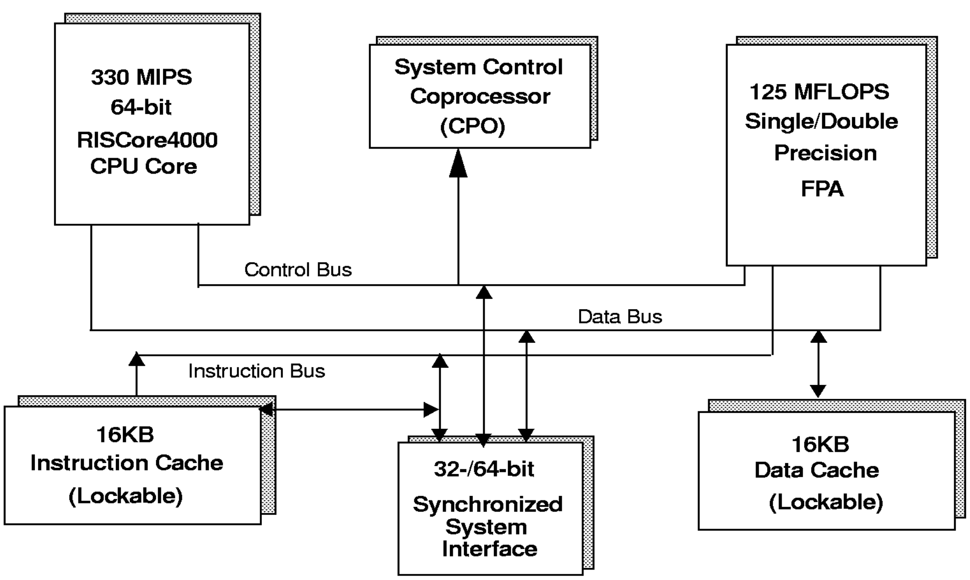
RISController™ Embedded 64-bit Microprocessor, based on RISCore4000™

RC64474™
RC64475™
Advance Information

Features

- *High performance 64-bit microprocessor, based on the RISCore4000*
  - *Minimized branch and load delays, through streamlined 5-stage scalar pipeline.*
  - *Single and double precision floating-point unit*
  - *125 peak MFLOP/s at 250 MHz*
  - *330 Dhrystone MIPS at 250 MHz*
  - *Flexible RC4700-compatible MMU*
  - *Joint TLB on-chip, for virtual-to-physical address mapping*
- *On-chip two-way set associative caches*
  - *16KB instruction cache (I-cache)*
  - *16KB data cache (D-cache)*
- *Optional I-cache and D-cache locking (per set), provides improved real-time support*
- *Enhanced, flexible bus interface allows simple, low-cost design*
  - *64-bit Bus Interface option, 1000MB/s bandwidth support*
  - *32-bit Bus Interface option, 500MB/s bandwidth support*
  - *SDRAM timing protocol, through delayed data in write cycles*
  - *RC4000/RC5000 family bus-protocol compatibility*
  - *Bus runs at fraction of pipeline clock (1/2 to 1/8)*
- *Implements MIPS-III Instruction Set Architecture (ISA)*
- *3.3V with 5V tolerant I/O*
- *Software compatible with entire RISController Series of Embedded Microprocessors*
- *Industrial temperature range support*
- *Active power management*
  - *Powers down inactive units, through sleep-mode feature*
- *100% pin compatibility between RC64474 and RC4640*
- *100% pin compatibility between RC64475 and RC4650*
- *RC64474 available in 128-pin QFP package, for 32-bit only systems*
- *RC64475 available in 208-pin QFP package, for full 64/32 bit systems*
- *Simplified board-level testing, through full Joint Test Action Group (JTAG) boundary scan*
- *Windows® CE compliant*

Block diagram



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Device overview[1]

Extending Integrated Device Technology's (IDT) RISCore4000 based choices (see Table 1), the RC64474 and RC64475 are high performance 64-bit microprocessors targeted towards applications that require high bandwidth, real-time response and rapid data processing and are ideal for products ranging from internetworking equipment (switches, routers) to multimedia systems such as web browsers, set-top boxes, video games, and Windows®CE based products. Based on IDT's RISCore4000, these processors are rated at 330 Dhrystone MIPS and 125 Million floating point operations per second, at 250 MHz. The internal cache bandwidth for these devices is over 3GB/second. The 64-bit external bus bandwidth is at more than 1000MB/s, and the 32-bit external bus bandwidth is at 500MB/s.

The RC64474 is packaged in a 128-pin footprint QFP package and uses a 32-bit external bus, offering the ideal combination of 64-bit processing power and 32-bit low-cost memory systems. The RC64475 is packaged in a 208-pin QFP footprint package and uses the full 64-bit external bus. The RC64475 is ideal for applications requiring 64-bit performance and 64-bit external bandwidth.

IDT's RISCore4000 is a 250MHz 64-bit execution core that uses a 5-stage pipeline, eliminating the "issue restrictions" associated with other more complex pipelines. The RISCore4000 implements the MIPS-III Instruction Set Architectue (ISA) and is upwardly compatible with applications that run on earlier generation parts.

1. Detailed system operation information is provided in the RC64474/RC64475 user's manual.

Implementation of the MIPS-III architecture results in 64-bit operations, improved performance for commonly used code sequences in operating system kernels, and faster execution of floating-point intensive applications.

The **RISCore4000 integer unit** implements a load/store architecture with single cycle ALU operations (logical, shift, add, subtract) and an autonomous multiply/divide unit. The ALU consists of the integer adder and logic unit. The adder performs address calculations in addition to arithmetic operations, and the logic unit performs all of the processor's logical and shift operations. Each unit is highly optimized and can perform an operation in a single pipeline cycle. Both 32- and 64-bit data operations are performed by the RISCore4000, utilizing 32 general purpose 64-bit registers (GPR) that are used for integer operations and address calculation. A complete on-chip floating-point co-processor (CP1), which includes a floating-point register file and execution units, forms a "seamless" interface, decoding and executing instructions in parallel with the integer unit.

CP1's floating-point execution units support both single and double precision arithmetic—as specified in the IEEE Standard 754—and are separated into a multiply unit and a combined add/convert/divide/square root unit. Overlap of multiplies and add/subtract is supported, and the multiplier is partially pipelined, allowing the initiation of a new multiply instruction every fourth pipeline cycle.

The **floating-point register file** is made up of thirty-two 64-bit registers. The floating-point unit can take advantage of the 64-bit wide data cache and issue a co-processor load or store doubleword instruction in every cycle. The RISCore4000's **system control coprocessor (CP0) registers** are also incorporated on-chip and provide the path through which the virtual memory system's page mapping is examined and changed, exceptions are handled, and any operating mode selections are controlled.

RISCore4000 Family

	RC4640	RC4650	RC4700	RC64474	RC64475
CPU	64-bit RISCore4000 w/ DSP extensions	64-bit RISCore4000 w/ DSP extensions	64-bit RISCore4000	64-bit RISCore4000	64-bit RISCore4000
Performance	>260MIPS	>260MIPS	>260MIPS	>330MIPS	>330MIPS
FPA	67 mflops, single precision only	67 mflops, single precision only	100 mflops, single and double precision	125 mflops, single and double precision	125 mflops, single and double precision
Caches	8kB/8kB, 2-way, lockable	8kB/8kB, 2-way, lockable	16kB/16kB, 2-way	16kB/16kB, 2-way, lockable	16kB/16kB, 2-way, lockable
External Bus	32-bit	32- or 64-bit	64-bit	32-bit, Superset pin compatible w/RC4640	31-or 64-bit, Superset pin compatible w/ RC4650
Voltages	3.3V	3.3V	3.3V	3.3V, 5V tolerant IO	3.3V, 5V tolerant IO
Frequencies	100-200 MHz	100-200 MHz	100-200 MHz	180-250 MHz	180-250 MHz
Packages	128 PQFP	208 MQUAD	208 MQUAD	128 QFP	208 QFP
MMU	Base-Bounds	Base-Bounds	96 page TLB	96 page TLB	96 page TLB
Key Features	Cache locking, on-chip MAC, 32-bit external bus	Cache locking, on-chip MAC, 32-bit & 64 bit bus option	Large Primary caches	Cache locking, JTAG, syncDRAM mode, 32-bit external bus	Cache locking, JTAG, syncDRAM mode, 32-64- bit bus option

Table 1 RISCore4000 Processor Family

A secure user processing environment is provided through the **user, supervisor, and kernel operating modes** of virtual addressing to system software. Bits in a status register determine which of these modes is used.

If configured for 64-bit **virtual addressing**, the virtual address space layout becomes an upwardly compatible extension of the 32-bit virtual address space layout. Figure 1 is an illustration of the address space layout for the 32-bit virtual address operation.

0xFFFFFFFF – 0xE0000000	Kernel virtual address space (kseg3) Mapped, 0.5GB
0xDFFFFFFF – 0xC0000000	Supervisor virtual address space (sseg) Mapped, 0.5GB
0xBFFFFFFF – 0xA0000000	Uncached kernel physical address space (kseg1) Unmapped, 0.5GB
0x9FFFFFFF – 0x80000000	Cached kernel physical address space (kseg0) Unmapped, 0.5GB
0x7FFFFFFF – 0x00000000	User virtual address space (useg) Mapped, 2.0GB

Figure 1 Kernel Mode Virtual Addressing (32-bit Mode)

The RC64474/RC64475's **Memory Management Unit (MMU)** controls the virtual memory system's page mapping and consists of a translation lookaside buffer (TLB) used for the virtual memory-mapping sub-system.

This large, **fully associative TLB** maps 96 virtual pages to their corresponding physical addresses. The TLB is organized as 48 pairs of even-odd entries and maps a virtual address and address space identifier into the large, 64GB physical address space. To assist in controlling the amount of mapped space and the replacement characteristics of various memory regions, two mechanisms are provided. First, the page size can be configured on a **per-entry basis**, to map a page size of 4KB to 16MB (in increments of 4x).

The second mechanism controls the replacement algorithm, when a TLB miss occurs. A random replacement algorithm is provided to select a TLB entry to be written with a new mapping; however, the processor provides a mechanism whereby a system specific number of mappings can be locked into the TLB and avoid being randomly replaced, which facilitates the design of real-time systems, by allowing deterministic access to critical software.

The TLB also contains information to control the cache coherency protocol for each page. However, hardware-based cache coherency is not supported.

The RC64474 and RC64475 enhance IDT's entire RISCore4000 series through the implementation of features such as boundary scan, to facilitate board level testing; enhanced support for SyncDRAM, to simplify system implementation and improve performance; and 5V tolerant I/Os, to enable interfacing with 5V devices.

The RC64474/475 processors offer a **direct migration path** for designs based on IDT's RC4640/RC4650 processors[2], through full pin and socket compatibility. Also, full 64-bit-family software and bus-protocol compatibility ensures the RC64474/475 access to an existing market and development infrastructure, allowing quicker time to market.

Development tools

An array of hardware and software tools are available to assist system designers in the rapid development of RC64474/475 based systems. This accessibility allows a wide variety of customers to take full advantage of the device's high-performance features while addressing today's aggressive time-to-market demands.

Cache memory

To keep the RC64474 and RC64475's high-performance pipeline full and operating efficiently, on-chip instruction and data caches have been incorporated. Each cache has its own data path and can be accessed in the same single pipeline clock cycle.

The 16KB two-way set associative **instruction cache (I-cache)** is virtually indexed, physically tagged and word parity protected. Because this cache is virtually indexed, the virtual-to-physical address translation occurs in parallel with the cache access, further increasing performance by allowing both operations to occur simultaneously. The instruction cache provides a peak instruction bandwidth of 1000MB/sec at 250MHz.

The 16KB two-way set associative **data cache (D-cache)** is byte parity protected and has a fixed 32-byte (eight words) line size. Its tag is protected with a single parity bit. To allow simultaneous address translation and data cache access, the D-cache is virtually indexed and physically tagged. The data cache can provide 8 bytes each clock cycle, for a peak bandwidth of 2GB/sec.

To lock critical sections of code and/or data into the caches for quick access, a **"cache locking"** feature has been implemented. Once enabled, a cache is said to be locked when a particular piece of code or data is loaded into the cache and that cache location will not be selected later for refill by other data. This feature locks a set (8KB) of Instruction and/or Data.

2. To ensure socket compatibility, refer to Table 8 and Table 9 at back of data sheet.

Table 2 lists the RC64474/475 Instruction and data cache attributes.

Characteristics	Instruction	Data
Size	16KB	16KB
Organization	2-way set associative	2-way set associative
Line size	16B	16B
read unit	32-bits	32-bits
write policy	na	write-back, write-through with or without write-allocate
Line transfer order	sub-block order, for load	sub-block order, for load sequential order, for store
Miss restart after transfer of:	entire line	miss word
Parity	per-word	per-byte
Cache locking	per set	per set

Table 2 RC64474/RC64475 Instruction/Data Cache Attributes

System interfaces

The RC64475 supports a 64-bit system interface that is bus compatible with the RC4650 system interface. The system interface consists of a 64-bit Address/Data bus with eight check bits and a 9-bit command bus that is parity protected.

During 64-bit operation, RC64475 system address/data (SysAD) transfers are protected with an 8-bit parity check bus, SysADC. When initialized for 32-bit operation, the RC64475's SysAD can be viewed as a 32-bit multiplexed bus that is protected by 4 parity check bits.

The RC64474 supports a 32-bit system interface[3] that is bus compatible with the RC4640. During 32-bit operation, SysAD transfers are performed on a 32-bit multiplexed bus (SysAD 0:31) that is protected by 4 parity check bits (SysADC 0:6).

Writes to external memory—whether they are cache miss write-backs, stores to uncached or write-through addresses—use the on-chip **write buffer**. The write buffer holds a maximum of four 64-bit addresses and 64-bit data pairs. The entire buffer is used for a data cache writeback and allows the processor to proceed in parallel with memory updates.

Six handshake signals: RdRdy*, WrRdy*, ExtRqst*, Release*, ValidOut*, and ValidIn*; **six interrupt inputs** and a **simple timing** specification that is capable of transferring data between the processor and memory at a peak rate of 1000MB/sec are included in the system interface. A boot-time selectable option to run the system interface as 32-bits wide—using basically the same protocols as the 64-bit system—is also supported.

A **boot-time mode control interface** initializes fundamental processor modes. The boot-time mode control interface is a serial interface that operates at a very low frequency (MasterClock divided by 256). This low-frequency operation allows the initialization information to be kept in a low-cost EPROM; alternatively, the twenty-or-so bits could be generated by the system interface ASIC or a simple PAL. The boot-time serial stream and configuration options are listed in Table 3 on page 5.

The **clocking interface** allows the CPU to be easily mated with external reference clocks. The CPU input clock is the bus reference clock and can be between 25 and 125MHz. An on-chip **phase-locked-loop (PLL)** generates the pipeline clock (PClock) through multiplication of the system interface clock by values of 2,3,4,5,6,7 or 8, as defined at system reset. This allows the pipeline clock to be implemented at a significantly higher frequency than the system interface clock. The RC64474/475 support single data (one to eight bytes) and 8-word block transfers on the SysAD bus.

The RC64474/475 implement additional **write protocols** that **double the effective write bandwidth**. The write re-issue has a repeat rate of 2 cycles per write. Pipelined writes have the same 2-cycle per write repeat rate but can issue an additional write after WrRdy* de-asserts.

Choosing a 32- or 64-bit wide system interface dictates whether a cache line block transaction requires 4 double word data cycles or 8 single word cycles as well as whether a single data transfer—larger than 4 bytes—must be divided into two smaller transfers.

Board-level testing during Run-Time mode is facilitated through the full JTAG boundary scan facility. Six pins—TDI, TDO, TMS, TCK, TRST* and JTAG32*—have been incorporated to support the standard JTAG interface.

System enhancement

To facilitate discrete **interface to SDRAM**, the RC64474/475 bus interface is enhanced with a programmable delay that is inserted between the write address and the write data, during write cycles (for both block and non-block writes).

The bus delay can be defined as 0 to 7 MasterClock cycles and is activated and controlled through mode bit (17:15) settings selected during the reset initialization sequence. The '000' setting provides the same write operations timing as the RC4640, RC4650, and RC5000 processors.

3. More details are provided in the RC64474/475 user's guide.

Table 3 lists the boot-time mode stream.

Serial Bit	Description	Value & Mode Setting
0	Reserved	Must be zero
4:1	**Writeback data rate** System interface data rate for block writes only: bit 4 is MSB	64-bit: 0→ dddd 1→ ddxddx 2 → ddxxddxx 3 → dxdxdx 4 → ddxxxddxxx 5 → ddxxxddxxx 6 → dxxdxxdxxdxx 7→ ddxxxxxxddxxxxxx 8 → dxxxdxxxdxxxdxxx 9:15 Reserved 32-bit 0→ wwwwwwww 1→ wwxwwxwwxwwx 2→ wwxxwwxxwwxxwwxx 3→ wxwxwxwxwxwxwxwx 4→ wwxxxwwxxxwwxxxwwxxx 5→ wwxxxwwxxxwwxxxwwxxx 6→ wxxwxxwxxwxxwxxwxxwxxwxx 7→ wwxxxxxxwwxxxxxxwwxxxxxxwwxxxxxx 8→ wxxxwxxxwxxxwxxxwxxxwxxxwxxxwxxx 9:15 Reserved
7:5	**Clock Multiplier** MasterClock is multiplied internally to generate PClock	Clock multiplier: 0 Multiply by 2 1 Multiply by 3 2 Multiply by 4 3 Multiply by 5 4 Multiply by 6 5 Multiply by 7 6 Multiply by 8 7 Reserved
8	**EndBit** Specifies byte ordering	0 → Little endian 1 → Big endian
10:9	**Non-block write** Selects non-block write type. **Bit 10 is MSB.**	00 → RC4x00 compatible 01 → Reserved 10 → pipelined writes 11 → write re-issue
11	**TmrIntEn** Disables the timer interrupt on Int*[5]	0 → Enabled Timer Interrupt 1 → Disabled Timer Interrupt
12	**System interface bus width**	0 → 64-bit system interface 1 → 32-bit system interface
14:13	**Drv_Out** output driver slew rate control. **Bit 14 is MSB.** Affects only non-clock outputs.	Output driver strength: 10 → 100% strength (fastest) 11 → 83% strength 00 → 67% strength 01 → 50% strength (slowest)
17:15	**WAdrWData_Del** Write address to write data delay in MasterClock cycles.	000 → 0 cycles 001 → 1 cycle 010 → 2 cycles 011 → 3 cycles 100 → 4 cycles 101 → 5 cycles 110 → 6 cycles 111 → 7 cycles
255:18	Reserved	Must be 0

Table 3 Boot-time Mode Stream

Power management

Executing the WAIT instruction enables the processor to enter Standby mode. The internal clocks will shut down, thus freezing the pipeline. The PLL, internal timer, and some of the input pins (Int[5:0]*, NMI*, ExtReq*, Reset*, and ColdReset*) will continue to run. Once the CPU is in Standby Mode, any interrupt, including the internally generated timer interrupt, will cause the CPU to exit Standby Mode.

Thermal considerations

The RC64474/475 are guaranteed in a case temperature range of 0° to +85° C, for commercial temperature devices; - 40° to +85° for industrial temperature devices. The type of package, speed (power) of the device, and airflow conditions affect the equivalent ambient temperature conditions that will meet this specification.

The equivalent allowable ambient temperature, T_A, can be calculated using the thermal resistance from case to ambient ($\varnothing_{CA}$) of the given package. The following equation relates ambient and case temperatures:

$T_A = T_C - P * \varnothing_{CA}$

where P is the maximum power consumption at hot temperature, calculated by using the maximum I_{CC} specification for the device.

Typical values for $\varnothing_{CA}$ at various airflows are shown in Table 4. Note that the RC64474/475 processors implement advanced power management, which substantially reduces the typical power dissipation of the device.

Preliminary

	∅CA					
Airflow (ft/min)	**0**	**200**	**400**	**600**	**800**	**1000**
128 QFP	21	13	10	9	8	7
208 QFP	20	12	9	8	7	6

Table 4 Thermal Resistance (∅CA) at Various Airflows

Pin description table

The following is a list of system interface pins available on the RC64474/475. Pin names ending with an asterisk (*) are active when low.

Pin Name	Type	Description
System Interface		
ExtRqst*	I	**External request** An external agent asserts ExtRqst* to request use of the System interface. The processor grants the request by asserting Release*.
Release*	O	**Release interface** In response to the assertion of ExtRqst* or a CPU read request, the processor asserts Release* and signals to the requesting device that the system interface is available.
RdRdy*	I	**Read Ready** The external agent asserts RDRdy* to indicate that it can accept a processor read request.
WrRdy*	I	**Write Ready** An external agent asserts WrRdy* when it can now accept a processor write request.
ValidIn*	I	**Valid Input** Signals that an external agent is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
ValidOut*	O	**Valid output** Signals that the processor is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
SysAD(63:0)	I/O	**System address/data bus** A 64-bit address and data bus for communication between the processor and an external agent. During address phases only, SysAd(35:0) contains invalid address information. The remaining SysAD(63:36) pins are not used. The whole 64-bit SysAD(63:0) are used during the data transfer phase. In 32-bit mode and in the RC64474, SysAD(63:32) is not used, regardless of Endianness. A 32-bit address and data communication between processor and external agent is performed via SysAD(31:0).
SysADC(7:0)	I/O	**System address/data check bus** An 8-bit bus containing parity check bits for the SysAD bus during data bus cycles. In 32-bit mode and in the RC64474, SysADC(7:4) is not used. The SysADC(3:0) contains check bits for SysAD(31:0).
SysCmd(8:0)	I/O	**System command/data identifier bus** A 9-bit bus for command and data identifier transmission between the processor and an external agent.
SysCmdP	I/O	**System Command Parity** A single, even-parity bit for the Syscmd bus. This signal is always driven low.
Clock/Control Interface		
MasterClock	I	**Master Clock** Master clock input establishes the processor and bus operating frequency. It is multiplied internally by 2,3,4,5,6,7,8 to generate the pipeline clock (PClock). This clock must be driven by 3.3V (Vcc) clock signals, regardless of the 5V tolerant pin setting.
VccP	I	**Quiet Vcc for PLL** Quiet Vcc for the internal phase locked loop.

Table 5 Pin Descriptions (Page 1 of 3)

Pin Name	Type	Description
VssP	I	**Quiet Vss for PLL** Quiet VSS for the internal phase locked loop.
5V Tolerant	I	**5V Tolerant I/O** This pin is used to convert the I/O ring of the RC4740/50 to 5V tolerant. In pure 3.3V systems whreno 5V sigas will be driven in the CPU, this pin must be driven with Vcc (3.3V). In systems where the RC4740/50 is expected to be driven with 5V signals, this input must be driven with 5V.
Interrupt Interface		
Int*(5:0)	I	**Interrupt** Six general processor interrupts, bit-wise ORed with bits 5:0 of the interrupt register.
NMI*	I	Non-maskable interrupt Non-maskable interrupt, ORed with bit 6 of the interrupt register.
Initialization Interface		
V_{CC}Ok	I	**V_{CC} is OK** When asserted, this signal indicates to the processor that the power supply has been above the Vcc minimum for more than 100 milliseconds and will remain stable. The assertion of VCCOk initiates the initialization sequence.
ColdReset*	I	**Cold reset** This signal must be asserted for a power on reset or a cold reset. ColdReset must be de-asserted synchronously with MasterClock.
Reset*	I	**Reset** This signal must be asserted for any reset sequence. It can be asserted synchronously or asynchronously for a cold reset, or synchronously to initiate a warm reset. Reset must be de-asserted synchronously with MasterClock.
ModeClock	O	**Boot-mode clock** Serial boot-mode data clock output at the system clock frequency divided by two hundred fifty-six.
ModeIn	I	**Boot-mode data in** Serial boot-mode data input.
JTAG Interface		
TDI	I	**JTAG Data In** On the rising edge of TCK, serial input data are shifted into either the Instruction register or Data register, depending on the TAP controller state.
TDO	O	**JTAG Data Out** On the falling edge of TCK, the TDO is serial data shifted out from either the instruction or data register. When no data is shifted out, the TDO is tri-stated (high impedance).

Table 5 Pin Descriptions (Page 2 of 3)

Pin Name	Type	Description
TCK	I	**JTAG Clock Input** An input test clock used to shift into or out of the boundary-scan register cells. TCK is independent of the system and processor clock with nominal 40-60% duty cycle.
TMS	I	**JTAG Command Select** The logic signal received at the TMS input is decoded by the TAP controller to control test operation. TMS is sampled on the rising edge of TCK.
TRST*	I	**JTAG Reset** The TRST* pin is an active-low signal used for asynchronous reset of the debug unit, independent of the processor logic. During normal CPU operation, the JTAG controller will be held in the reset mode, asserting this active low pin. When asserted low, this pin will also cause the TDO into tristate mode.
JTAG32*	I	**JTAG 32-bit scan** This pin is used to control length of the scan chanin for SYsAD (32-bit or 64-bit) for the JTAG mode. When set to Vss, 32-bit bus mode is selected. In this mode, only SysAD(31:0) are part of the scan chain. When set to Vcc, 64-bit bus mode is selected. In this mode, SysAD(63:0) are part of the scan chain. This pin has a built-in pull-down device to guarantee 32-bit scan, if it is left uncovered.
JR_Vcc	I	**JTag VCC** This pin has an internal pull-down to continuously reset the JTAG controller (if left unconnected) bypassing the TRst* pin. When supplied with Vcc, the TRst* pin will be the primary control for the JTAG reset.

Table 5 Pin Descriptions (Page 3 of 3)

Logic diagram — RC64474/RC64475

Figure 2 illustrates the direction and functional groupings for the processor signals.

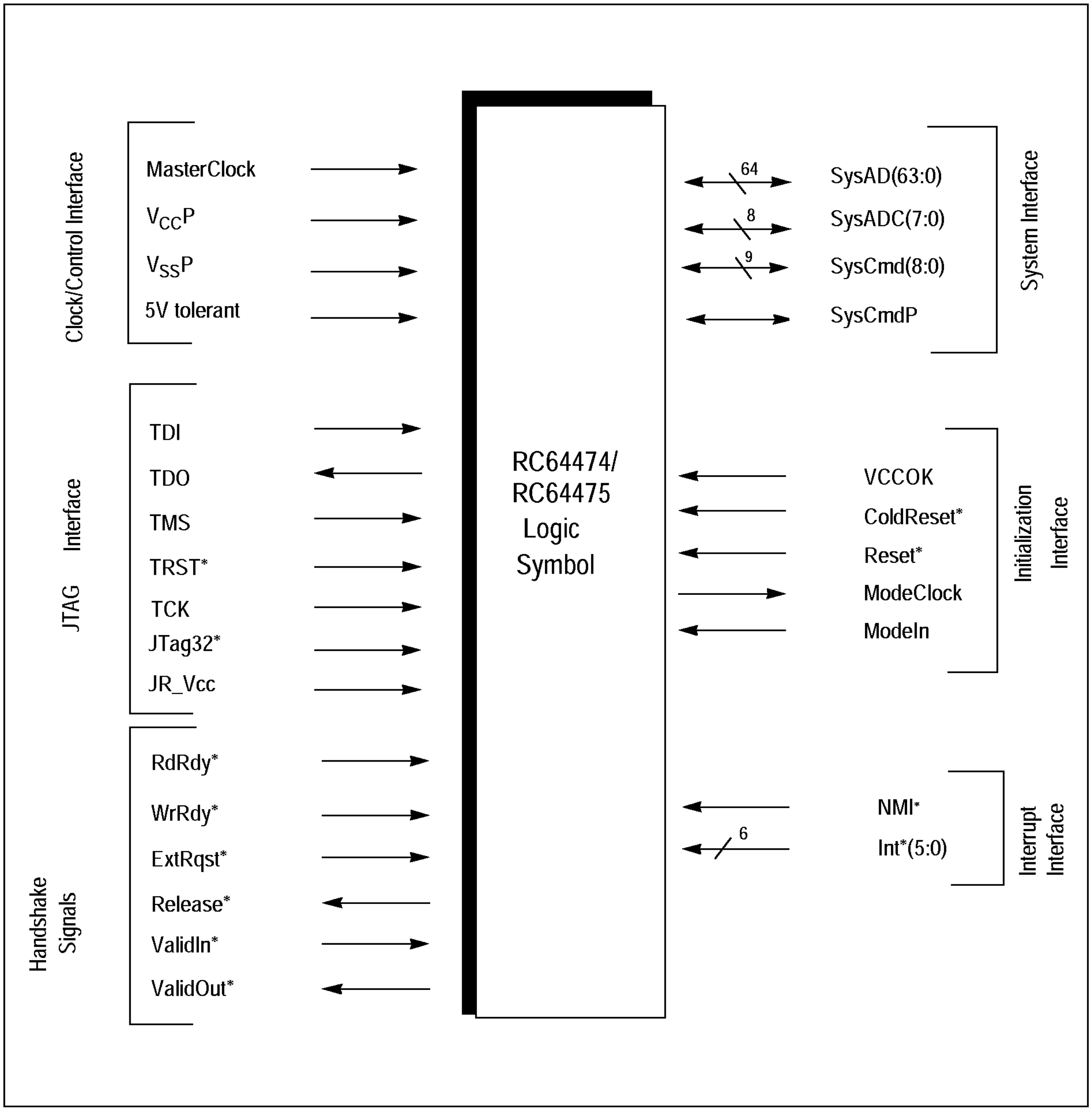


Figure 2 Logic Diagram for RC64474/RC64475

RC64475 208-pin QFP package pin-out

Pin names followed by an asterisk (*) are active when low. For maximum flexibility and compatibility with future designs, N.C. pins should be left floating.

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	N.C.	53	JTAG32*	105	N.C.	157	N.C.
2	N.C.	54	N.C.	106	N.C.	158	N.C.
3	N.C.	55	N.C.	107	N.C.	159	SysAD59
4	N.C.	56	N.C.	108	N.C.	160	ColdReset*
5	N.C.	57	SysCmd2	109	N.C.	161	SysAD28
6	N.C.	58	SysAD36	110	N.C.	162	VCC
7	N.C.	59	SysAD4	111	N.C.	163	VSS
8	N.C.	60	SysCmd1	112	N.C.	164	SysAD60
9	N.C.	61	VSS	113	N.C.	165	Reset*
10	SysAD11	62	VCC	114	SysAD52	166	SysAD29
11	VSS	63	SysAD35	115	ExtRqst*	167	SysAD61
12	VCC	64	SysAD3	116	VCC	168	SysAD30
13	SysCmd8	65	SysCmd0	117	VSS	169	VCC
14	SysAD42	66	SysAD34	118	SysAD21	170	VSS
15	SysAD10	67	VSS	119	SysAD53	171	SysAD62
16	SysCmd7	68	VCC	120	RdRdy*	172	SysAD31
17	VSS	69	SysAD2	121	Modein	173	SysAD63
18	VCC	70	Int5*	122	SysAD22	174	VCC
19	SysAD41	71	SysAD33	123	SysAD54	175	VSS
20	SysAD9	72	SysAD1	124	VCC	176	VCCOK
21	SysCmd6	73	VSS	125	VSS	177	SysADC3
22	SysAD40	74	VCC	126	Release*	178	SysADC7
23	VSS	75	Int4*	127	SysAD23	179	N.C.
24	VCC	76	SysAD32	128	SysAD55	180	TDI
25	SysAD8	77	SysAD0	129	NMI*	181	TRst*
26	SysCmd5	78	Int3*	130	VCC	182	TCK
27	SysADC4	79	VSS	131	VSS	183	TMS
28	SysADC0	80	VCC	132	SysADC2	184	TDO
29	VSS	81	Int2*	133	SysADC6	185	VCCP
30	VCC	82	SysAD16	134	SysAD24	186	VSSP
31	SysCmd4	83	SysAD48	135	VCC	187	MasterClock
32	SysAD39	84	Int1*	136	VSS	188	VCC
33	SysAD7	85	VSS	137	SysAD56	189	VSS
34	SysCmd3	86	VCC	138	SysAD25	190	SysADC5
35	VSS	87	SysAD17	139	SysAD57	191	SysADC1

Table 6 RC64475 208-pin QFP Package Pin-Out (Page 1 of 2)

Pin	Function	Pin	Function	Pin	Function	Pin	Function
36	VCC	88	SysAD49	140	5VTolerant	192	VCC
37	SysAD38	89	Int0*	141	VSS	193	VSS
38	SysAD6	90	SysAD18	142	N.C	194	SysAD47
39	ModeClock	91	VSS	143	SysAD26	195	SysAD15
40	WrRdy*	92	VCC	144	SysAD58	196	SysAD46
41	SysAD37	93	SysAD50	145	N.C.	197	VCC
42	SysAD5	94	ValidIn*	146	VCC	198	VSS
43	VSS	95	SysAD19	147	VSS	199	SysAD14
44	VCC	96	SysAD51	148	SysAD27	200	SysAD45
45	N.C.	97	VSS	149	N.C.	201	SysAD13
46	N.C.	98	VCC	150	JR_Vcc	202	SysAD44
47	N.C.	99	ValidOut*	151	N.C.	203	VSS
48	N.C.	100	SysAD20	152	N.C.	204	VCC
49	N.C.	101	N.C.	153	N.C.	205	SysAD12
50	N.C.	102	N.C.	154	N.C.	206	SysCmdP
51	N.C.	103	N.C.	155	N.C.	207	SysAD43
52	N.C.	104	N.C.	156	N.C.	208	N.C.

Table 6 RC64475 208-pin QFP Package Pin-Out (Page 2 of 2)

RC64474 128-pin QFP package pin-out

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	JTAG32*	33	Vcc	65	Vcc	97	Vcc
2	SysCmd2	34	Vss	66	SysAD28	98	Vss
3	Vcc	35	SysAD13	67	ColdReset*	99	SysAD19
4	Vss	36	SysAD14	68	SysAD27	100	ValidIn*
5	SysAD5	37	Vss	69	Vss	101	Vcc
6	WrRdy*	38	Vcc	70	Vcc	102	Vss
7	ModeClock	39	SysAD15	71	JR_Vcc	103	SysAD18
8	SysAD6	40	Vss	72	SysAD26	104	Int0*
9	Vcc	41	Vcc	73	N.C.	105	SysAD17
10	Vss	42	SysADC1	74	Vss	106	Vcc
11	SysCmd3	43	Vss	75	5VTolerant	107	Vss
12	SysAd7	44	Vcc	76	SysAD24	108	Int1*
13	SysCmd4	45	MasterClock	77	Vss	109	SysAD16
14	Vcc	46	VssP	78	Vcc	110	Int2*
15	Vss	47	VccP	79	SysAD24	111	Vcc
16	SysAdC0	48	TDO	80	SysADC2	112	Vss

Table 7 RC64474 128-pin QFP Package Pin-out (Page 1 of 2)

Pin	Function	Pin	Function	Pin	Function	Pin	Function
17	SysCmd5	49	TMS	81	Vss	113	Int3*
18	SysAD8	50	TCK	82	Vcc	114	SysAD0
19	Vcc	51	TRst*	83	NMI*	115	Int4*
20	Vss	52	TDI	84	SysAD23	116	Vcc
21	SysCmd6	53	Vss	85	Release*	117	Vss
22	SysAD9	54	SysADC3	86	Vss	118	SysAD2
23	Vcc	55	VccOK	87	Vcc	119	Int5*
24	Vss	56	Vss	88	SysAD22	120	SysAD2
25	SysCCmd7	57	Vcc	89	Modein	121	Vcc
26	SysAD10	58	SysAD31	90	RdRdy*	122	Vss
27	SysCmd8	59	Vss	91	SysAD21	123	SysCmd0
28	Vcc	60	Vcc	92	Vss	124	SysAd3
29	Vss	61	SysAD30	93	Vcc	125	Vcc
30	SysAD11	62	SysAD29	94	ExtRqst*	126	Vss
31	SysCmdP	63	Reset*	95	SysAD20	127	SysCmd1
32	SysAD12	64	Vss	96	ValidOut*	128	SysAD4

Table 7 RC64474 128-pin QFP Package Pin-out (Page 2 of 2)

Socket compatibility—RC64474 & RC4640

To ensure socket compatibility between the RC4640 and the RC64474 devices, several pin changes are required, as shown below.

Pin	RC4640	RC64474	Compatible to RC4640?	Comments
1	N.C	JTAG32*	Yes.	Pin has an internal pull-down, to enable 32-bit scan. Can also be left a N.C.
48	Vss	TDO	Yes.	Can be driven with Vss, if JTAG is not needed. Is tristated when TRsT* is low.
49	Vss	TMS	Yes.	Can be driven with Vss if JTAG is not needed.
50	Vss	TCK	Yes.	Can be driven with Vss if JTAG is not needed.
51	Vss	TRsT*	Yes.	Can be driven with Vss if JTAG is not needed.
52	Vss	TDI	Yes.	Can be driven with Vss if JTAG is not needed.
71	N.C.	JR_Vcc	Yes.	Can be left N.C. in RC64474, if JTAG is not need. If JTAG is needed, it must be driven to Vcc.
75	Vcc	5V Tolerant	Yes.	In 3.3V systems, this pin must be driven with 3.3V to maintain full RC4640 compatibility. If 5V tolerant I/Os are needed, then this pin must be driven with 5V, which does not maintain RC4640 compatibility.

Table 8 RC64474/R4640 Socket Compatibility

Socket compatibility—RC64475 & RC4650

Pin	RC4650 32-bit	RC64475 32-bit	RC4650 64-bit	RC64475 64-bit	Compatible to RC4640?	Comments
53	N.C.	JTAG32*	N.C.	JTAG32*	Yes	In 32-bit, this pin can be left unconnected because of internal pull-down. In 64-bit, this assumes that JTAG will not be used. If using JTAG, this pin must be at Vcc.
140	Vcc	5VTolerant	Vcc	5VTolerant	Yes	In **3.3V** systems, this pin must be driven with 3.3V to maintain full RC4650 compsibility. If **5V tolerant** I/Os are needed, then this pin must be driven with 5V, which does not maintain RC4650 compatibility.
150	N.C.	JR_Vcc	N.C	JR_Vcc	Yes	In RC64475, can be left a N.C, if JTAG is not need. If JTAG is needed, it must be driven to Vcc.
180	N.C.	TDI	N.C.	TDI	Yes	If JTAG is not needed, can be left a N.C.
181	N.C.	TRsT*	N.C.	TRsT*	Yes	If JTAG is not needed, can be left a N.C.
182	N.C.	TCK	N.C.	TCK	Yes	If JTAG is not needed, can be left a N.C.
183	N.C.	TMS	N.C.	TMS	Yes	If JTAG is not needed, can be left a N.C.
184	N.C.	TDO	N.C.	TDO	Yes	If JTAG is not needed, can be left a N.C.

Table 9 RC64475/RC4650 Socket Compatibility

Absolute maximum ratings(1)

Symbol	Rating	RC64474/475 3.3V±5% Commercial	RC64474/475 3.3V±5% Industrial	Unit
V_{TERM}	Terminal Voltage with respect to GND	–0.5(2) to +4.6	–0.5(2) to +4.6	V
T_C	Operating Temperature(case)	0 to +85	-40 to +85	°C
T_{BIAS}	Case Temperature Under Bias	–55 to +125	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	–55 to +125	°C
I_{IN}	DC Input Current	20(3)	20(3)	mA
I_{OUT}	DC Output Current	50(4)	50(4)	mA

NOTES TO ABSOLUTE MAXIMUM RATING TABLE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN} minimum = –2.0V for pulse width less than 15ns. V_{IN} should not exceed V_{CC} +0.5 Volts.
3. When $V_{IN} < 0V$ or $V_{IN} > V_{CC}$
4. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

Recommended operation temperature and supply voltage

Grade	Temperature	Gnd	RC64474/475
			V_{CC}
Commercial	0°C to +85°C (Case)	0V	3.3V±5%
Industrial	-40 + 85°C (Case)	0V	3.3V±5%

DC electrical characteristics

Commercial Temperature Range—RC64474/64475

(V_{CC} = 3.3±5%, T_{CASE} = 0°C to +85°C)

Parameter	RC64474/RC64475 180MHz		RC64474/RC64475 200MHz		RC64474/RC64475 250MHz		Conditions
	Minimum	Maximum	Minimum	Maximum	Minimum	Maximum	
VOL	—	0.1V	—	0.1V	—	0.1V	|IOUT|= 20uA
VOH	VCC - 0.1V	—	VCC - 0.1V	—	VCC - 0.1V	—	
VOL	—	0.4V	—	0.4V	—	0.4V	|IOUT|= 4mA
VOH	2.4V	—	2.4V	—	2.4V	—	
VIL	–0.5V	0.2VCC	–0.5V	0.2VCC	–0.5V	0.2VCC	—
V_{IH}	2.0V	V_{CC} + 0.5V	2.0V	V_{CC} + 0.5V	2.0V	V_{CC} + 0.5V	—
I_{IN}	—	±10uA	—	±10uA	—	±10uA	$0 \leq V_{IN} \leq V_{CC}$
C_{IN}	—	10pF	—	10pF	—	10pF	—
C_{OUT}	—	10pF	—	10pF	—	10pF	—
I/O_{LEAK}	—	20uA	—	20uA	—	20uA	Input/Output Leakage

Power consumption—RC64474

Parameter		RC64474 180MHz		RC64474 200MHz		RC64474 250MHz		Conditions
		Typical(9)	Max	Typical(9)	Max	Typical(9)	Max	
System Condition:		180/45MHz		200/50MHz		250/62.5		—
I_{CC}	standby	—	75 mA[b]	—	100 mA[b]	—	100mA[b]	C_L = 0pF(8)
		—	150 mA[b]	—	200 mA[b]	—	200mA[b]	C_L = 50pF
	active	530 mA[b]	630 mA[b]	600mA[b]	700 mA[b]	700 mA[b]	850mA	C_L = 0pF No SysAd activity(8)
		630mA[b]	750 mA[b]	700 mA[b]	850 mA[b]	850mA	1000mA	C_L = 50pF R4x00 compatible writes, T_C = 25°C
		750 mA[b]	900 mA[a]	850 mA[b]	1000 mA[a]	1000mA	1200mA	C_L = 50pF Pipelined writes or write re-issue, T_C = 25°C(8)

a. These are the specifications IDT tests to insure compliance.
b. These are not tested. They are the results of engineering analysis and are provided for reference only.

Power consumption—RC64475

Parameter		RC64475 180MHz		RC64475 200MHz		RC64475 250MHz		Conditions
		Typical(9)	Max	Typical(9)	Max	Typical(9)	Max	
System Condition:		180/45MHz		200/50MHz		250/62.5MHz		—
I_{CC}	standby	—	60 mA[b]	—	60 mA[b]	—	100 mA[b]	C_L = 0pF(8)
		—	110 mA[b]	—	110 mA[b]	—	110 mA[b]	C_L = 50pF
	active, 64-bit bus option[c]	720 mA[b]	850 mA[b]	850 mA[b]	1000 mA[b]	935 mA[b]	1100 mA[b]	C_L = 0pF No SysAd activity(8)
		850 mA[b]	1000 mA[b]	1000 mA[b]	1200 mA[b]	1100mA[b]	1360mA[b]	C_L = 50pF R4x00 compatible writes, T_C = 25°C
		1000 mA[b]	1200 mA[a]	1200 mA[b]	1400 mA[a]	1360 mA[b]	1600 mA[b]	C_L = 50pF Pipelined writes or write re-issue, T_C = 25°C(8)

a. These are the specifications IDT tests to insure compliance.

b. These are not tested. They are the results of engineering analysis and are provided for reference only.

c. In 32-bit bus option, use RC64474 power consumption values.

Timing characteristics—RC64474/RC64475

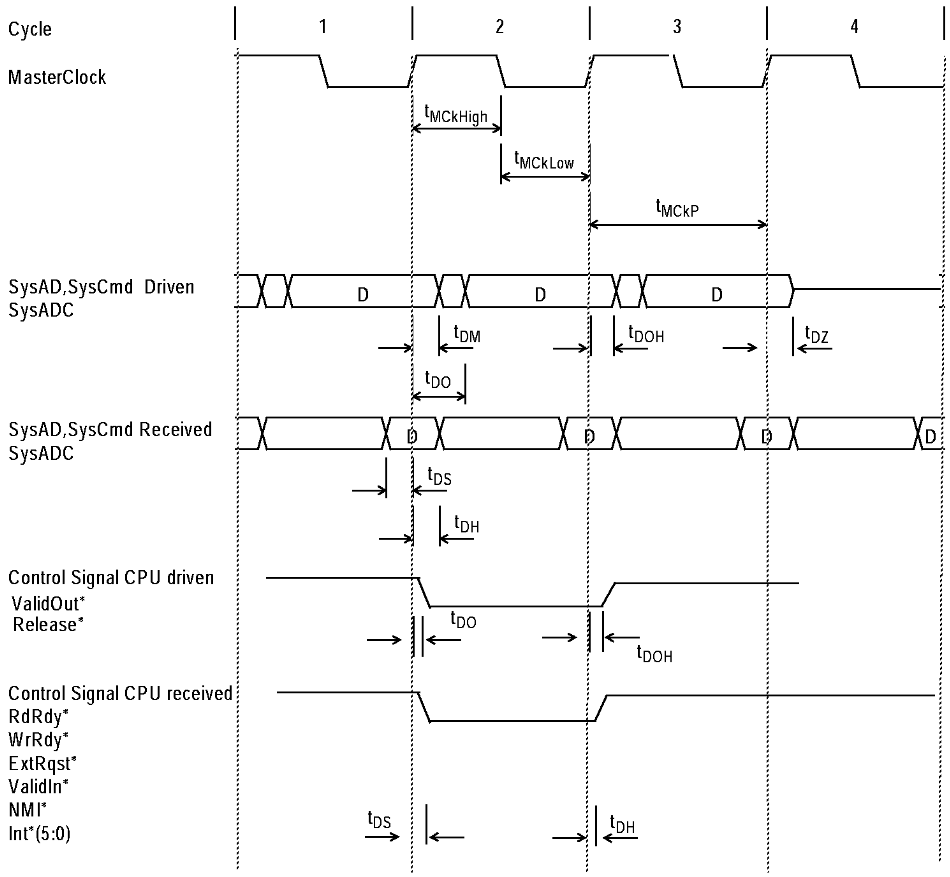


Figure 3 System Clocks Data Setup, Output, and Hold timing

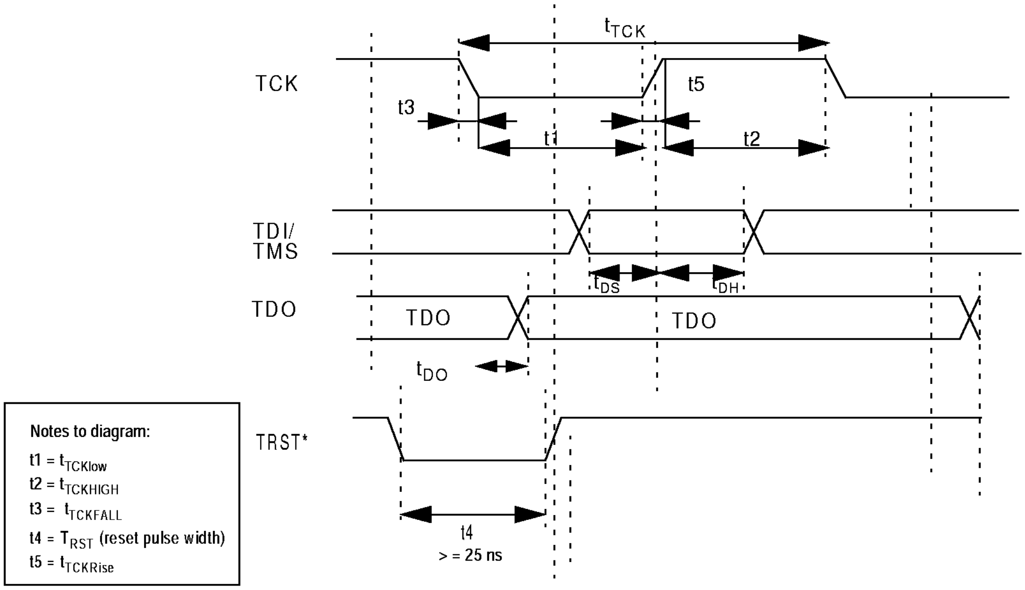


Figure 4 Standard JTAG timing

AC electrical characteristics

Commercial Temperature Range RC64474/RC64475

(V_{CC}=3.3V ± 5%; T_{CASE} = 0×C to +85°C)

Clock Parameters

Parameter	Symbol	Test Conditions	RC64474/ RC64475 180MHz		RC64474/ RC64475 200MHz		RC64474/ RC64475 250MHz		Units
			Min	Max	Min	Max	Min	Max	
Pipeline clock Frequency	PClk		50	180	50	200	50	250	MHz
MasterClock HIGH	t_{MCHIGH}	Transition ≤ 5ns	3	—	3	—	2.5	—	ns
MasterClock LOW	t_{MCLOW}	Transition ≤ 5ns	3	—	3	—	2.5	—	ns
MasterClock Frequency	_	—	25	90	25	100	25	125	MHz
MasterClock Period	t_{MCP}	—	11.1	40	10	40	8	40	ns
Clock Jitter for MasterClock	$t_{JitterIn}$	—	—	±250	—	±250	—	±250	ps
MasterClock Rise Time	t_{MCRise}	—	—	2.5	—	2	—	2	ns
MasterClock Fall Time	t_{MCFall}	—	—	2.5	—	2	—	2	ns
ModeClock Period	$t_{ModeCKP}$	—	—	256* t_{MCP}	—	256* t_{MCP}	—	256* t_{MCP}	ns
JTAG Clock Input	t_{TCK}	—	10	—	10	—	10	—	ns
JTAG Clock HIGH	$t_{TCKHIGH}$	—	4	—	4	—	4	—	ns
JTAG Clock Low	t_{TCKLOW}	—	4	—	4	—	4	—	ns
JTAG Clock Rise Time	$t_{TCKRise}$	—	—	2.5	—	2.5	—	2.5	ns
JTAG Clock Fall Time	$t_{TCKFall}$	—	—	2.5	—	2.5	—	2.5	ns

NOTES TO RC64474/475 AC/DC ELECTRICAL CHARACTERISTIC TABLES:

5. Operation of the RC64474/RC64475 is only guaranteed with the Phase Lock Loop enabled.
6. Timings are measured from 1.5V of the clock to 1.5V of the signal.
7. Capacitive load for all output timings is 50pF.
8. Guaranteed by design.
9. Typical integer instruction mix and cache miss rates.

Capacitive load deration—RC64474/RC64475

Parameter	Symbol	Test Conditions	180MHz		200MHz†		250MHz†		Units
			Min	Max	Min	Max	Min	Max	
Load Derate	C_{LD}	—	—	2	—	2	—	2	ns/25pF

System interface parameters

Parameter	Symbol	Test Conditions	RC64474/ RC64475 180MHz		RC64474/ RC64475 200MHz		RC64474/ RC64475 250MHz		Units
			Min	Max	Min	Max	Min	Max	
Data Output(7)	t_{DM}= Min t_{DO} = Max	$mode_{14..13}$ = 10 (fastest)	1.0(8)	6	1.0(8)	5	1.0(8)	5	ns
		$mode_{14..13}$ = 01 (slowest)	2.0(8)	9	2.0(8)	9	2.0(8)	9	ns
Data Output Hold	t_{DOH}*	$mode_{14..13}$ = 10 (fastest)	1.0	—	1.0	—	1.0	—	ns
Data Setup	t_{DS}	t_{rise} = 5ns t_{fall} = 5ns	3	—	3	—	3	—	ns
Data Hold	t_{DH}		1.0	—	1.0	—	1.0	—	ns

* 50pf loading on external output signals, fastest settings. Also applies to JTAG signals (TRST*,TDO,TDI,TMS)

Boot-Time interface parameters

Parameter	Symbol	RC64474/ RC64475 180 MHz		RC64474/ RC64475 200 MHz		RC64474/ RC64475 250MHz		Units
		Min	Max	Min	Max	Min	Max	
Mode Data Setup	t_{DS}	3	—	3	—	3	—	Master Clock Cycle
Mode Data Hold	t_{DH}	0	—	0	—	0	—	Master Clock Cycle

Mode configuration interface reset sequence

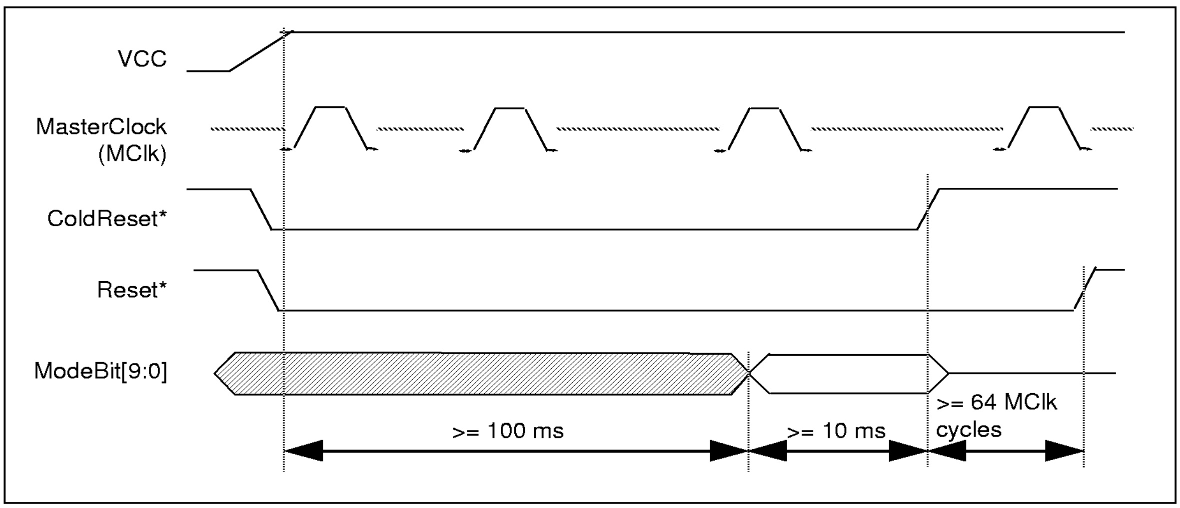
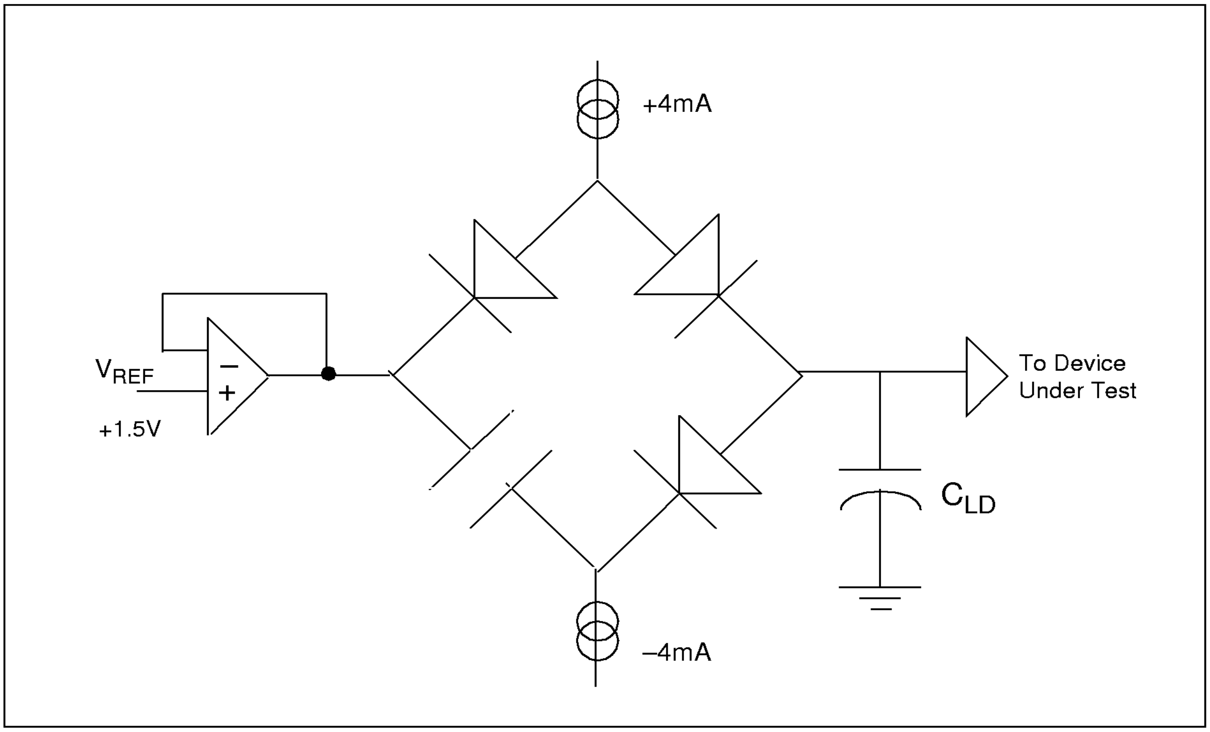


Figure 5 Mode Configuration Interface Reset Sequence

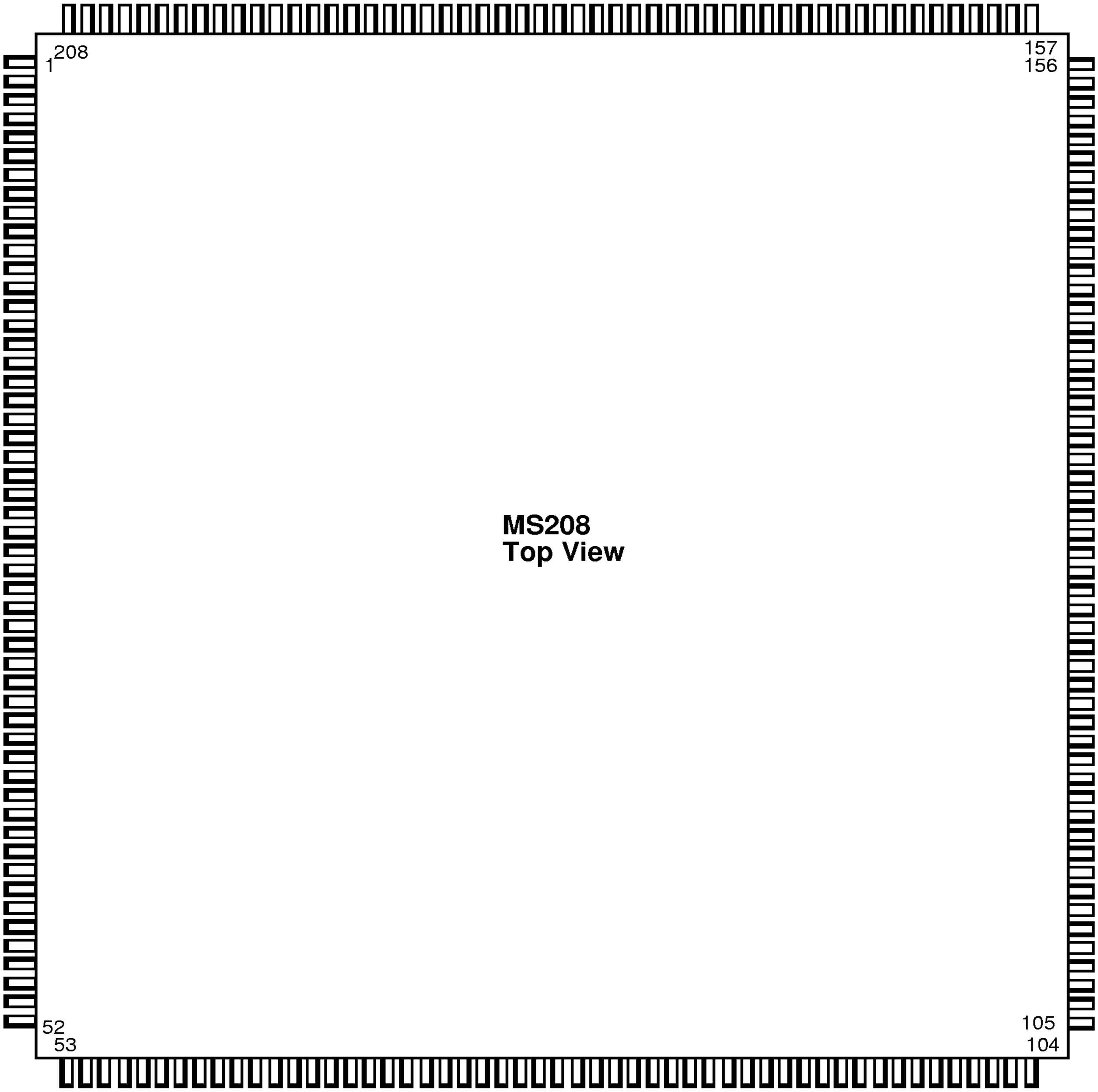
Output loading for AC testing



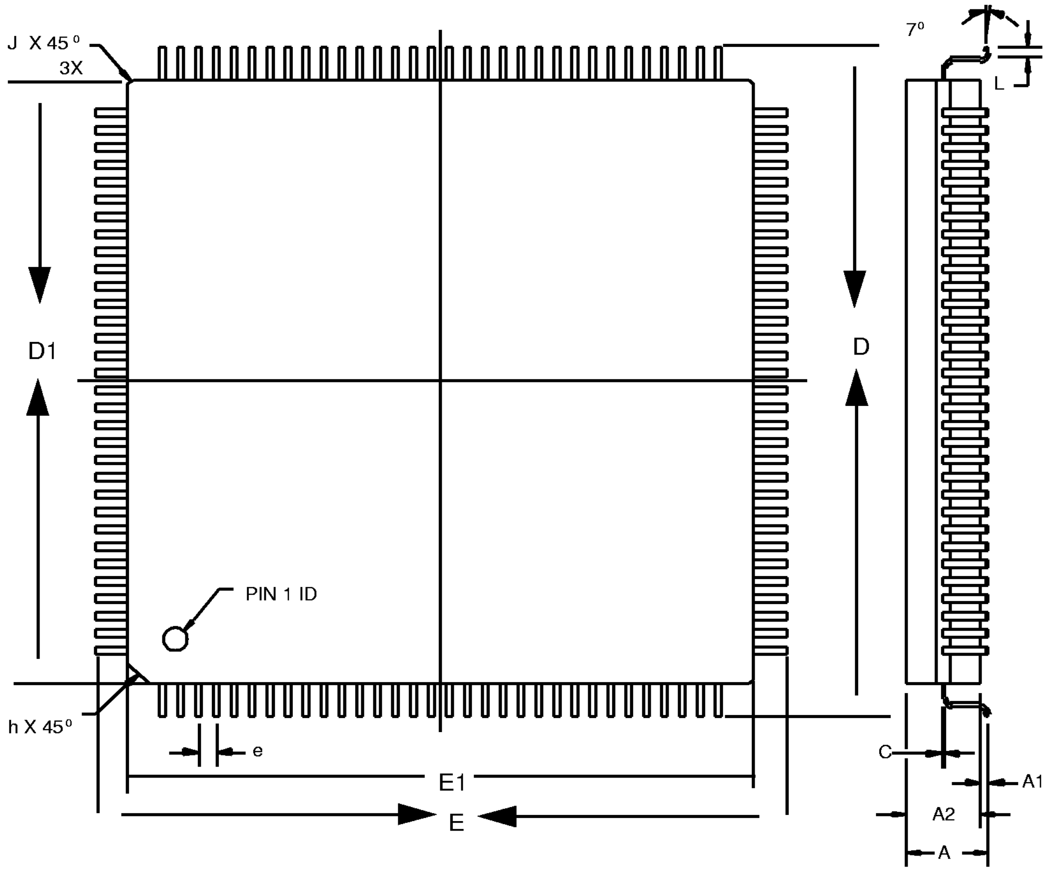
Signal	Cld
All Signals	50 pF

RC64475 physical specifications

The RC64475 is available in a 208-pin power quad (PQUAD) package.



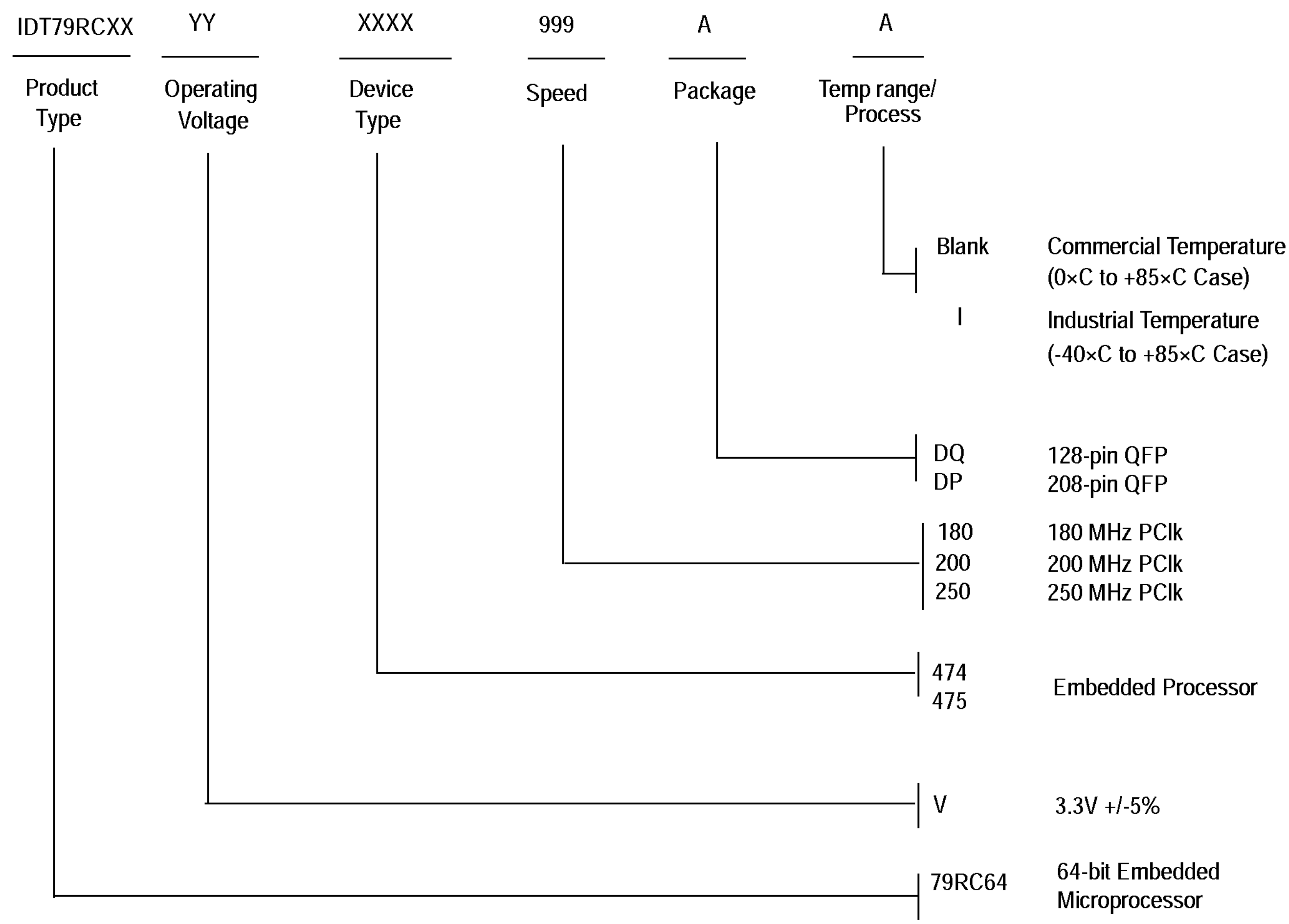
RC64474 128-pin PQFP package



SYMBOLS	MIN	MAX
A	3.50	3.86
A1	.25	.51
A2	3.17	3.43
b	.30	.45
C	.13	.23
D/E	31.00	31.40
D1/E1	27.59	27.79
e	.80 BSC	
J	.20 REF	
h	.89 REF	
L	.68	-

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.

Ordering information



Valid combinations

IDT79RC64V474 - 180, 200, 250 DQ	128-pin QFP package, Commercial Temperature
IDT79RC64V475 - 180, 200, 250 DP	208-pin QFP package, Commercial Temperature
IDT79RC64V474 - 180, 200, 250 DQI	128-pin QFP package, Industrial Temperature
IDT79RC64V474 - 180, 200, 250 DPI	208-pin QFP package, Industrial Temperature

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