Integrated Device Technology, Inc.

256K (16K x 16-BIT) & 128K (8K x 16-BIT) CMOS STATIC RAM PLASTIC SIP MODULES

IDT 8MP656S
IDT 8MP628S

FEATURES:

- High-density 256K/128K CMOS static RAM modules
- 16K x 16 organization (IDT8MP656S) with 8K x 16 option (IDT8MP628)
- Upper byte (I/O_{9-16}) and lower byte (I/O_{1-8}) separated control
  - Flexibility in application
- Fast access times
  - 40ns (max.)
- Low power consumption
  - Active: less than 825mW (typ. in 16K x 16 organization)
  - Standby: less than 20mW (typ.)
- Cost-effective plastic surface mounted RAM packages on an epoxy laminate (FR-4) substrate
- Offered in an SIP (single in-line) package for maximum space-savings
- Utilizes IDT7164s—high-performance 64K static RAMs produced with advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

The IDT8MP656S/IDT8MP628S are 256K/128K-bit high-speed CMOS static RAMs constructed on an epoxy laminate substrate using four IDT7164 8K x 8 static RAMs (IDT8MP656S) or two IDT7164 static RAMs (IDT8MP628S) in plastic surface mount packages.

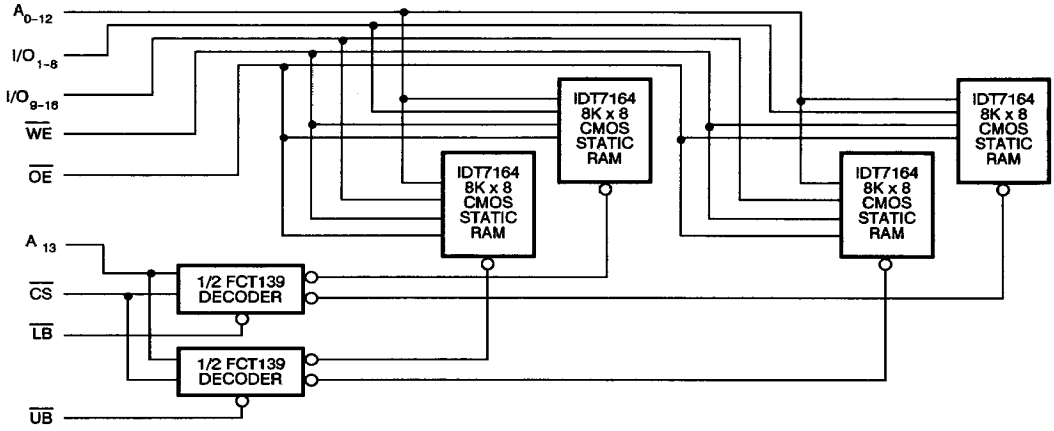
Functional equivalence to proposed monolithic static RAMs is achieved by utilization of an on-board decoder that interprets the higher order address A_{13} to select one of the two 8K x 16 RAMs as the by-16 output and using $\overline{LB}$ and $\overline{UB}$ as two extra chip select functions for lower byte (I/O_{1-8}) and upper byte (I/O_{9-16}) control, respectively. (On the IDT8MP628S 8K x 16 option, A_{13} needs to be externally grounded for proper operation.) Extremely high speeds are achievable by the use of IDT7164s, fabricated in IDT's high-performance, high-reliability CEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 256K/128K static RAMs available.

The IDT8MP656S/IDT8MP628S are available with maximum operating power consumption of only 1.8W (IDT8MP656S 16K x 16 option). The modules also offer a full standby mode of 330mW (max.).

The IDT8MP656S/IDT8MP628S are offered in a 40-pin plastic SIP. For the JEDEC standard 40-pin DIP, refer to the IDT8M656S/IDT8M628S.

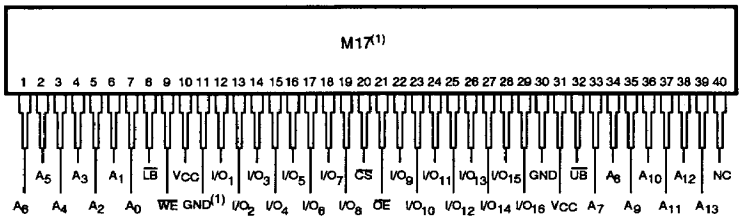
All inputs and outputs of the IDT8MP656S/IDT8MP628S are TTL-compatible and operate from a single 5V supply. (NOTE: Both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



SIP
FRONT VIEW

NOTE:
1. For module dimensions, please refer to module drawing M17 in the packaging section.

PIN NAMES

A_{0-13}	Addresses
I/O_{1-16}	Data Input/Output
$\overline{CS}$	Chip Select
V_{CC}	Power
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground
$\overline{UB}$	Upper Byte Control
$\overline{LB}$	Lower Byte Control

NOTES:
1. Both V_{CC} pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation.
2. On IDT8MP628S, 128K (8K x 16-Bit) option, A_{13}(Pin 39) is required external grounding for proper operation.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5 (1)	–	0.8	V

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%, V_{CC} (Min.) = 4.5V, V_{CC} (Max.) = 5.5V, V_{LC} = 0.2V, V_{HC} = V_{CC} = - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS	IDT8MP656S MIN.	IDT8MP656S TYP.	IDT8MP656S MAX.	IDT8MP628S MIN.	IDT8MP628S TYP.	IDT8MP628S MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	—	15	—	—	15	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	—	15	—	—	15	µA
I_{CCX16}	Operating Current In X16 Mode	$\overline{CS}$, $\overline{UB}$ & $\overline{LB}$ = V_{IL} V_{CC} = Max., Output Open f = f_{MAX}	—	165	330	—	150	300	mA
I_{CCX8}	Operating Current In X8 Mode	$\overline{CS}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL} V_{CC} = Max., Output Open f = f_{MAX}	—	100	200	—	80	170	mA
I_{SB} & I_{SB1}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH} or UB ≥ V_{IH} and $\overline{LB}$ ≥ V_{IH} V_{CC} = Max. Output Open	—	4	60	—	2	30	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	—	—	2.4	—	—	V

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

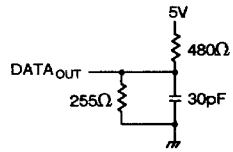


Figure 1. Output Load

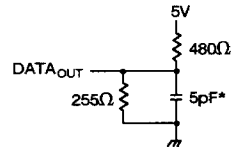


Figure 2. Output Load (for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW}, t_{WHZ})

*Including scope and jig.

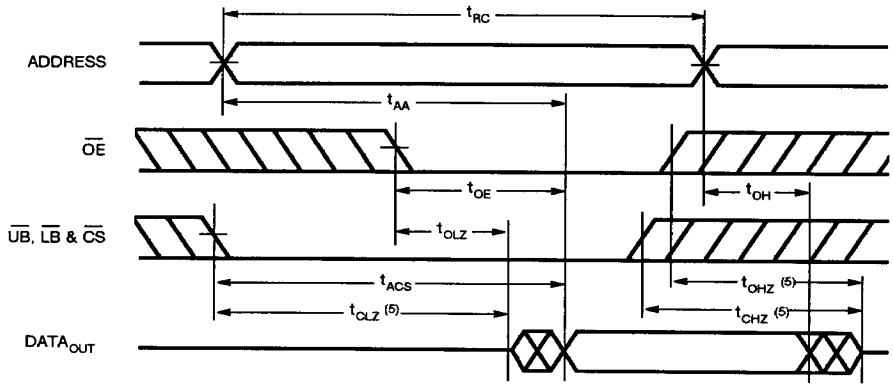
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETERS	IDT8MP656S40 IDT8MP628S40 MIN.	MAX.	IDT8MP656S50 IDT8MP628S50 MIN.	MAX.	IDT8MP656S70 IDT8MP628S70 MIN.	MAX.	IDT8MP656S85 IDT8MP628S85 MIN.	MAX.	UNIT
READ CYCLE										
t_{RC}	Read Cycle Time	40	–	50	–	70	–	85	–	ns
t_{AA}	Address Access Time	–	40	–	50	–	70	–	85	ns
t_{ACS}	Chip Select Access Time	–	40	–	50	–	70	–	85	ns
$t_{CLZ1,2}$ (1)	Chip Select to Output in Low Z	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	25	–	30	–	40	–	50	ns
t_{OLZ} (1)	Output Enable to Output in Low Z	5	–	5	–	5	–	5	–	ns
t_{CHZ} (1)	Chip Select to Output in High Z	–	15	–	20	–	30	–	35	ns
t_{OHZ} (1)	Output Disable to Output in High Z	–	15	–	20	–	30	–	35	ns
t	Output Hold from Address Change	5	–	5	–	5	–	5	–	ns
t_{PU} (1)	Chip Select to Power Up Time	0	–	0	–	0	–	0	–	ns
t_{PD} (1)	Chip Deselect to Power Down Time	–	40	–	50	–	70	–	85	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	40	–	50	–	70	–	85	–	ns
t_{CW}	Chip Selection to End of Write	5	–	45	–	65	–	75	–	ns
t_{AW}	Address Valid to End of Write	35	–	45	–	65	–	75	–	ns
t_{AS}	Address Set-up Time	5	–	5	–	10	–	10	–	ns
t_{WP}	Write Pulse Width	30	–	40	–	55	–	65	–	ns
t_{WR}	Write Recovery Time	5	–	5	–	5	–	10	–	ns
t_{WHZ} (1)	Write Enable to Output in High Z	–	15	–	20	–	25	–	30	ns
t_{DW}	Data to Write Time Overlap	15	–	20	–	30	–	35	–	ns
t_{DH}	Data Hold from Write Time	5	–	5	–	5	–	5	–	ns
t_{OW} (1)	Output Active from End of Write	5	–	5	–	5	–	5	–	ns

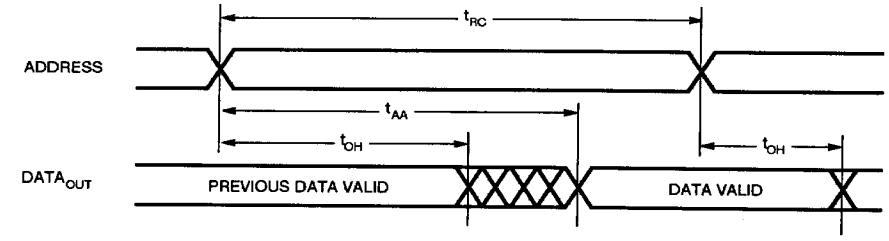
NOTE:
1. This parameter guaranteed but not tested.

13

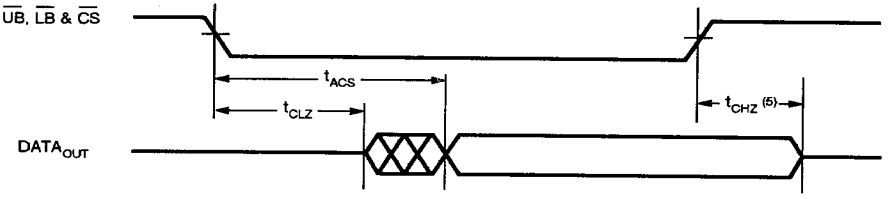
TIMING WAVEFORM OF READ CYCLE NO. 1[1]



TIMING WAVEFORM OF READ CYCLE NO. 2[1, 2, 4]



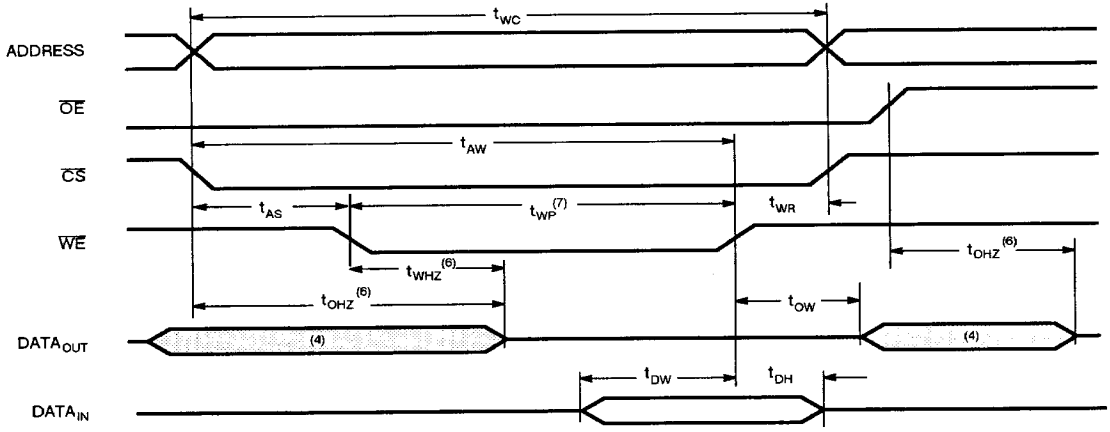
TIMING WAVEFORM OF READ CYCLE NO. 3[1, 3, 4]



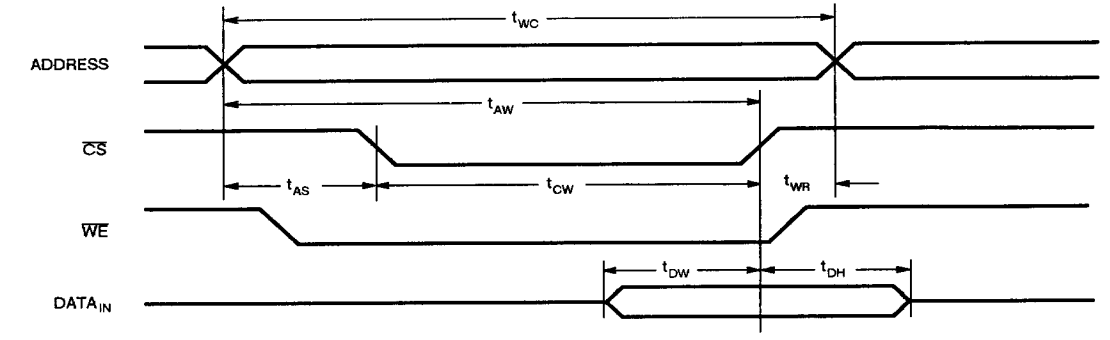
NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{UB}$, $\overline{LB}$ = V_{IL} for 16 output active.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}
5. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3, 7]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)[1, 2, 3, 5]



13

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse (t_{WP}) > t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

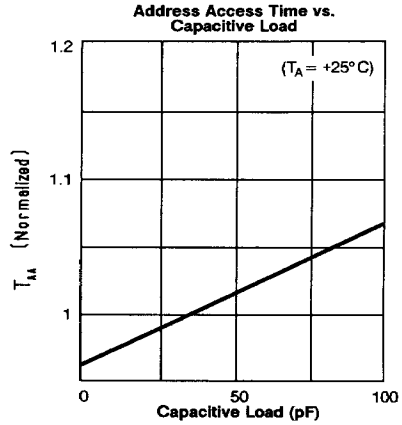
TRUTH TABLE

MODE	$\overline{CS}$	$\overline{UB}$	$\overline{LB}$	$\overline{OE}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	X	X	X	High Z	Standby
Standby	L	H	H	X	X	High Z	Standby
Read	L	L	L	L	H	$D_{OUT\ 1-16}$	Active
Lower Byte Read	L	H	L	L	H	$D_{OUT\ 1-8}$	Active (X8)
Upper Byte Read	L	L	H	L	H	$D_{OUT\ 9-16}$	Active (X8)
Read	L	L	L	H	H	High Z	Active
Lower Byte Read	L	H	L	H	H	High Z	Active (X8)
Upper Byte Read	L	L	H	H	H	High Z	Active (X8)
Write	L	L	L	X	L	$D_{IN\ 1-16}$	Active
Lower Byte Write	L	H	L	X	L	$D_{IN\ 1-8}$	Active (X8)
Upper Byte Write	L	L	H	X	L	$D_{IN\ 9-16}$	Active (X8)

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	40	pF

NOTE:
1. This parameter is sampled and not 100% tested.



ORDERING INFORMATION