



SPI/I²C® Compatible, Temperature Sensor, Four Channel ADC and Quad Voltage Output DAC

Preliminary Technical Data

ADT7516/7517/7518

FEATURES

ADT7516 - Four 12-Bit DACs

ADT7517 - Four 10-Bit DACs

ADT7518 - Four 8-Bit DACs

Buffered Voltage Output

Guaranteed Monotonic By Design Over All Codes

10-Bit Temperature to Digital Converter

10-Bit Four Channel ADC :

DC Input Bandwidth

Input Range: 0 V to 2.25 V

Temperature range: -40°C to +125°C

Temperature Sensor Accuracy of $\pm 0.5^{\circ}\text{C}$

Supply Range : + 2.7 V to + 5.5 V

DAC Output Range: 0 - 2V_{REF}

Power-Down Current 1 μ A

Internal 2.25 V_{Ref} Option

Double-Buffered Input Logic

Buffered Reference Input Option

Power-on Reset to Zero Volts

Simultaneous Update of Outputs (LDAC Function)

On-Chip Rail-to-Rail Output Buffer Amplifier

I²C®, SPI™, QSPI™, MICROWIRE™ and DSP-Compatible 4-wire Serial Interface

16-Lead QSOP Package

APPLICATIONS

Portable Battery Powered Instruments

Personal Computers

Smart Battery Chargers

Telecommunications Systems

Electronic Test Equipment

Domestic Appliances

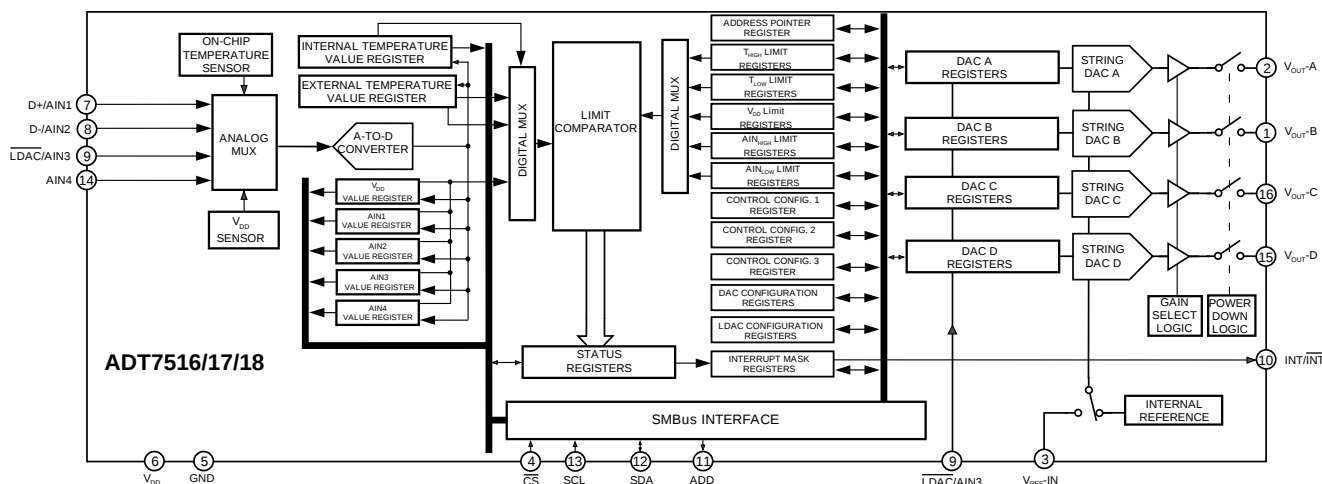
Process Control

GENERAL DESCRIPTION

The ADT7516/7517/7518 combines a 10-Bit Temperature-to-Digital Converter, a 10-Bit Four Channel ADC and a quad 12/10/8-Bit DAC respectively, in a 16-Lead QSOP package. This includes a bandgap temperature sensor and a 10-bit ADC to monitor and digitize the temperature reading to a resolution of 0.25 °C. The ADT7516/17/18 operates from a single +2.7 V to + 5.5 V supply. The input voltage range on the ADC channels has a range of 0V to 2.25V and the input bandwidth is DC. The reference for the ADC channels is derived internally. The output voltage of the DAC ranges from 0 V to V_{DD} , with an output voltage settling time of typ 7 msec. The ADT7516/17/18 provides two serial interface options, a four-wire serial interface which is compatible with SPITM, QSPITM, MICROWIRETM and DSP interface standards; and a two-wire SMBus/I²C interface. It features a standby mode that is controlled via the serial interface.

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FUNCTIONAL BLOCK DIAGRAM



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MICROWIRE is a trademark of National Semiconductor Corporation.
The ADT7316/7317/7318 is protected by the following U.S. patent
numbers and by other intellectual property rights :
6,169,442 6,097,239 US Patent Pending
5,867,012 5,764,174

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: <http://www.analog.com>
Fax: 781/326-8703 Analog Devices, Inc., 2003

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ADT7516/7517/7518

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The reference for the four DACs is derived either internally or from a reference pin. The outputs of all DACs may be updated simultaneously using the software LDAC function or external LDAC pin. The ADT7516/7517/7518 incorporates a power-on-reset circuit, which ensures

that the DAC output powers-up to zero volts and it remains there until a valid write takes place.

The ADT7516/7517/7518's wide supply voltage range, low supply current and SPI/I²C-compatible interface, make it ideal for a variety of applications, including personal computers, office equipment and domestic appliances.

ADT7516/ADT7517/ADT7518-SPECIFICATIONS¹(V_{DD}=2.7 V to 5.5 V, GND=0 V, REF_{IN}=2.25 V, unless otherwise noted)

Parameter ²	Min	Typ	Max	Units	Conditions/Comments
DAC DC PERFORMANCE^{3,4}					
ADT7518					
Resolution		8		Bits	
Relative Accuracy		±0.15	±1	LSB	
Relative Accuracy		tbd	tbd	LSB	Excluding Offset and Gain errors
Differential Nonlinearity		±0.02	±0.25	LSB	Guaranteed Monotonic by design over all codes
ADT7517					
Resolution		10		Bits	
Relative Accuracy		±0.5	±4	LSB	
Relative Accuracy		tbd	tbd	LSB	Excluding Offset and Gain errors
Differential Nonlinearity		±0.05	±0.5	LSB	Guaranteed Monotonic by design over all codes
ADT7516					
Resolution		12		Bits	
Relative Accuracy		±2	±16	LSB	
Relative Accuracy		tbd	tbd	LSB	Excluding Offset and Gain errors
Differential Nonlinearity		±0.02	±0.9	LSB	Guaranteed Monotonic by design over all codes
Offset Error		±0.4	±3	% of FSR	
Offset Error Match			±0.5	LSB	
Gain Error		±0.3	±1.25	% of FSR	
Gain Error Match			±0.5	LSB	
Lower Deadband		20	60	mV	Lower Deadband exists only if Offset Error is Negative. See Figure 5.
Upper Deadband		tbd	tbd	mV	Upper Deadband exists if V _{REF} = V _{DD} and Offset plus Gain Error is positive. See Figure 6.
Offset Error Drift ⁶		-12		ppm of FSR/°C	
Gain Error Drift ⁶		-5		ppm of FSR/°C	
DC Power Supply Rejection Ratio ⁶		-60		dB	ΔV _{DD} = ±10%
DC Crosstalk ⁶		200		μV	Reference Figure 4
ADC DC ACCURACY					Max V _{DD} = 5 V
Resolution			10	Bits	
Integral Nonlinearity			±2	LSB	
Differential Nonlinearity			±0.9	LSB	
Offset Error			±2	% of FSR	
Offset Error Match			±0.5	LSB	
Gain Error			±2	% of FSR	
Gain Error Match			±0.5	LSB	
ADC Bandwidth			DC	Hz	
ANALOG INPUTS					
Input Voltage Range	0		2.25	V	AIN1 to AIN4. C4 = 0 in Control Config. 3.
	0		V _{DD}	V	AIN1 to AIN4. C4 = 1 in Control Config. 3.
AIN Conversion Time		712		μs	Averaging (16 samples) on.
		44.5		μs	Averaging off.
DC Leakage Current			±1	μA	
Input Capacitance		tbd	tbd	pF	
Input Resistance		tbd		Ω	

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Parameter ²	Min	Typ	Max	Units	Conditions/Comments
THERMAL CHARACTERISTICS					Internal Reference used. Averaging on.
INTERNAL TEMPERATURE SENSOR					
Accuracy @ $V_{DD}=3.3V \pm 10\%$			± 0.5	$^{\circ}C$	$T_A = 40^{\circ}C$
		± 0.5	± 2	$^{\circ}C$	$T_A = 0^{\circ}C$ to $+85^{\circ}C$
		± 2	± 3	$^{\circ}C$	$T_A = -40^{\circ}C$ to $+125^{\circ}C$
Accuracy @ $V_{DD}=5V \pm 5\%$			± 1	$^{\circ}C$	$T_A = 40^{\circ}C$
		± 2	± 3	$^{\circ}C$	$T_A = 0^{\circ}C$ to $+85^{\circ}C$
		± 3	± 4	$^{\circ}C$	$T_A = -40^{\circ}C$ to $+125^{\circ}C$
Resolution			10	Bits	Equivalent to $0.25^{\circ}C$
Long Term Drift		0.5		$^{\circ}C/1000hrs$	
Conversion Time		25.92		ms	Averaging (16 samples) on.
		1.62		ms	Averaging off.
EXTERNAL TEMPERATURE SENSOR					
Accuracy @ $V_{DD}=3.3V \pm 10\%$			± 1	$^{\circ}C$	External Transistor = 2N3906.
			± 2	$^{\circ}C$	$T_A = 40^{\circ}C$
			± 3	$^{\circ}C$	$T_A = 0^{\circ}C$ to $+85^{\circ}C$.
				$^{\circ}C$	$T_A = -40^{\circ}C$ to $+125^{\circ}C$
Accuracy @ $V_{DD}=5V \pm 5\%$			± 1.5	$^{\circ}C$	$T_A = 40^{\circ}C$
		± 2	± 3	$^{\circ}C$	$T_A = 0^{\circ}C$ to $+85^{\circ}C$
		± 3	± 4	$^{\circ}C$	$T_A = -40^{\circ}C$ to $+125^{\circ}C$
Resolution			10	Bits	Equivalent to $0.25^{\circ}C$
Conversion Time		16.8		ms	Averaging (16 samples) on.
		1.05		ms	Averaging off.
Output Source Current		180		μA	High Level
		11		μA	Low Level
THERMAL VOLTAGE OUTPUT					
8-Bit DAC Output					
Resolution	1			$^{\circ}C$	
Scale Factor		8.79		mV/ $^{\circ}C$	0- V_{REF} Output. $T_A = -40^{\circ}C$ to $+125^{\circ}C$
		17.58		mV/ $^{\circ}C$	0-2 V_{REF} Output. $T_A = -40^{\circ}C$ to $+125^{\circ}C$
10-Bit DAC Output					
Resolution	0.25			$^{\circ}C$	
Scale Factor		2.2		mV/ $^{\circ}C$	0- V_{REF} Output. $T_A = -40^{\circ}C$ to $+125^{\circ}C$
		4.39		mV/ $^{\circ}C$	0-2 V_{REF} Output. $T_A = -40^{\circ}C$ to $+125^{\circ}C$
ROUND ROBIN UPDATE RATE ⁶					
Averaging On		29.48		ms	Time to complete one measurement cycle.
Averaging Off		1.842		ms	Pins 7 and 8 configured for AIN1 and AIN2
Averaging On		44.86		ms	Pins 7 and 8 configured for AIN1 and AIN2
Averaging Off		2.8		ms	Pins 7 and 8 configured for D+ and D-
DAC EXTERNAL REFERENCE INPUT ⁷					
V_{REF} Input Range	1		V_{DD}	V	Buffered Reference
V_{REF} Input Impedance		>10		M Ω	Buffered reference and Power-Down Mode
Reference Feedthrough		-90		dB	Frequency=10KHz
Channel-to-Channel Isolation		-75		dB	Frequency=10KHz
ON-CHIP REFERENCE					
Reference Voltage ⁷		2.25		V	
Temperature Coefficient ⁷		80		ppm/ $^{\circ}C$	
OUTPUT CHARACTERISTICS ⁷					
Output Voltage ⁸	0.001		$V_{DD}-0.001$	V	This is a measure of the minimum and maximum drive capability of the output amplifier
DC Output Impedance		0.5		Ω	
Short Circuit Current		25		mA	$V_{DD} = +5V$
		16		mA	$V_{DD} = +3V$
Power Up Time		2.5		μs	Coming out of Power Down Mode. $V_{DD} = +5V$
		5		μs	Coming out of Power Down Mode. $V_{DD} = +3.3V$

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DIGITAL INPUTS⁷				
Input Current		± 1	μA	$V_{IN} = 0V \text{ to } V_{DD}$
V_{IL} , Input Low Voltage		0.8	V	
V_{IH} , Input High Voltage	1.89		V	
Pin Capacitance	3	10	pF	All Digital Inputs
SCL, SDA Glitch Rejection		50	ns	Input Filtering Suppresses Noise Spikes of Less than 50ns.
$\overline{LDAC}$ Pulse Width	20		ns	Edge triggered input.
DIGITAL OUTPUT				
Output High Voltage, V_{OH}	2.4		V	$I_{SOURCE} = I_{SINK} = 200 \mu A$
Output Low Voltage, V_{OL}		0.4	V	$I_{OL} = 3 \text{ mA}$
Output High Current, I_{OH}		1	mA	$V_{OH} = 5 \text{ V}$
Output Capacitance, C_{OUT}		50	pF	
$\overline{INT}/\overline{INT}$ Output Saturation Voltage		0.8	V	$I_{OUT} = 4 \text{ mA}$
I²C TIMING CHARACTERISTICS^{9,10}				
Serial Clock Period, t_1	2.5		μs	Fast-Mode I ² C. See Figure 1
Data In Setup Time to SCL High, t_2				
Data Out Stable after SCL Low, t_3	0		ns	See Figure 1
SDA Low Setup Time to SCL Low (Start Condition), t_4	50		ns	See Figure 1
SDA High Hold Time after SCL High (Stop Condition), t_5	50		ns	See Figure 1
SDA and SCL Fall Time, t_6		90	ns	See Figure 1
SPI TIMING CHARACTERISTICS^{11,12}				
$\overline{CS}$ to SCLK Setup Time, t_1	0		ns	See Figure 2
SCLK High Pulsewidth, t_2	50		ns	See Figure 2
SCLK Low Pulse, t_3	50		ns	See Figure 2
Data Access Time after SCLK Falling edge, t_4^{12}		35	ns	See Figure 2
Data Setup Time Prior to SCLK Rising Edge, t_5	20		ns	See Figure 2
Data Hold Time after SCLK Rising Edge, t_6	0		ns	See Figure 2
$\overline{CS}$ to SCLK Hold Time, t_7	0		ns	See Figure 2
$\overline{CS}$ to DOUT High Impedance, t_8		40	ns	See Figure 2
POWER REQUIREMENTS				
V_{DD}	2.7	5.5	V	
V_{DD} Settling Time		50	ms	V_{DD} settles to within 10% of it's final voltage level
I_{DD} (Normal Mode) ¹⁴		2	mA	$V_{DD} = +3.3 \text{ V}$, $V_{IH} = V_{DD}$ and $V_{IL} = \text{GND}$
		2.2	mA	$V_{DD} = +5 \text{ V}$, $V_{IH} = V_{DD}$ and $V_{IL} = \text{GND}$
I_{DD} (Power Down Mode)	TBD	3	μA	$V_{DD} = +3.3 \text{ V}$, $V_{IH}=V_{DD}$ and $V_{IL}=\text{GND}$
	TBD	10	μA	$V_{DD} = +5 \text{ V}$, $V_{IH}=V_{DD}$ and $V_{IL}=\text{GND}$
Power Dissipation	TBD	6.6	μW	$V_{DD} = +3.3 \text{ V}$. Normal Mode
	TBD	10	μW	$V_{DD} = +3.3 \text{ V}$. Shutdown Mode

Notes:

¹ Temperature ranges are as follows: A Version: -40°C to +125°C.

² See Terminology.

³ DC specifications tested with the outputs unloaded.

⁴ Linearity is tested using a reduced code range: ADT7516 (code 115 to 4095); ADT7517 (code 28 to 1023); ADT7518 (code 8 to 255)

⁵ See Terminology.

⁶ Round Robin is the continuous sequential measurement of the following channels : V_{DD} , Internal Temperature, External Temperature/ (AIN1, AIN2), AIN3 and AIN4.

⁷ Guaranteed by Design and Characterization, not production tested

⁸ In order for the amplifier output to reach its minimum voltage, Offset Error must be negative. In order for the amplifier output to reach its maximum voltage ($V_{REF}=V_{DD}$) "Offset plus Gain" Error must be positive.

⁹ The SDA & SCL timing is measured with the input filters turned on so as to meet the Fast-Mode I²C specification. Switching off the input filters improves the transfer rate but has a negative affect on the EMC behaviour of the part.

¹⁰ Guaranteed by design. Not tested in production.

¹¹ Guaranteed by design and characterization, not production tested.

¹² All input signals are specified with $t_r = t_f = 5 \text{ ns}$ (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.

¹³ Measured with the load circuit of Figure 3.

¹⁴ I_{DD} spec. is valid for all DAC codes and fullscale analog input voltage. Interface inactive. All DACs and ADC active. Load currents excluded. Specifications subject to change without notice.

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DAC AC CHARACTERISTICS¹

($V_{DD} = +2.7V$ to $+5.5V$; $R_L = 4k7\Omega$ to GND; $C_L = 200pF$ to GND;
 $4K7\Omega$ to V_{DD} ; All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter ²	Min	Typ @ 25°C	Max	Units	Conditions/Comments
Output Voltage Settling Time					$V_{REF} = V_{DD} = +5V$
ADT7518		6	8	μs	1/4 Scale to 3/4 Scale change (40 Hex to C0 Hex)
ADT7517		7	9	μs	1/4 Scale to 3/4 Scale change (100 Hex to 300 Hex)
ADT7516		8	10	μs	1/4 Scale to 3/4 Scale change (400 Hex to C00 Hex)
Slew Rate		0.7		V/ μs	
Major-Code Change Glitch Energy		12		nV-s	1 LSB change around major carry.
Digital Feedthrough		0.5		nV-s	
Digital Crosstalk		1		nV-s	
Analog Crosstalk		0.5		nV-s	
DAC-to-DAC Crosstalk		3		nV-s	
Multiplying Bandwidth		200		kHz	$V_{REF} = 2V \pm 0.1V_{pp}$
Total Harmonic Distortion		-70		dB	$V_{REF} = 2.5V \pm 0.1V_{pp}$. Frequency=10kHz.

NOTES

¹Guaranteed by Design and Characterization, not production tested

²See Terminology

Specifications subject to change without notice.

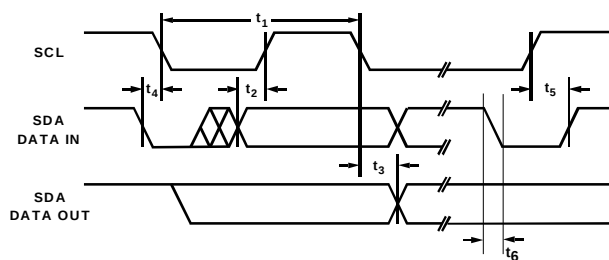


Figure 1. Diagram for I²C Bus Timing

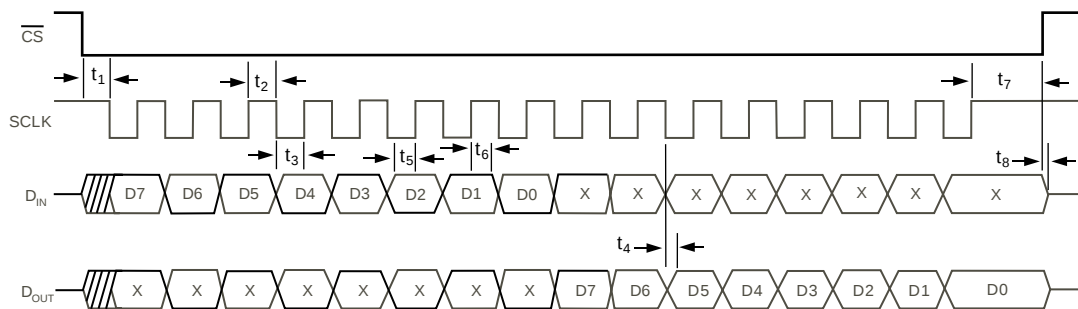


Figure 2. Diagram for SPI Bus Timing

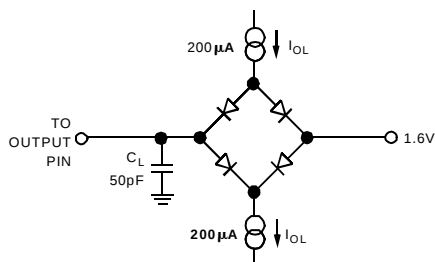


Figure 3. Load Circuit for Access Time and Bus Relinquish Time

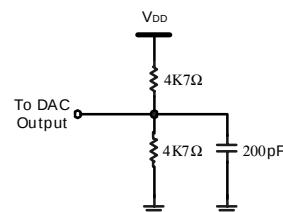


Figure 4. Load Circuit for DAC Outputs

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ABSOLUTE MAXIMUM RATINGS¹

V _{DD} to GND	-0.3 V to +7 V
Analog Input Voltage to GND	-0.3 V to V _{DD} + 0.3 V
Digital Input Voltage to GND	-0.3 V to V _{DD} + 0.3 V
Digital Output Voltage to GND	-0.3 V to V _{DD} + 0.3 V
Reference Input voltage to GND	-0.3 V to V _{DD} + 0.3V
Operating Temperature Range	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
16-Lead QSOP Package	
Power Dissipation ²	(T _j max - T _A) / θ _{JA}
Thermal Impedance ³	
θ _{JA} Junction-to-Ambient	105.44 °C/W
θ _{JC} Junction-to-Case	38.8 °C/W
IR Reflow Soldering	
Peak Temperature	+220°C (-0/+5°C)
Time at Peak Temperature	10 to 20 secs
Ramp-up Rate	2-3°C/sec
Ramp-down Rate	-6°C/sec

Notes:

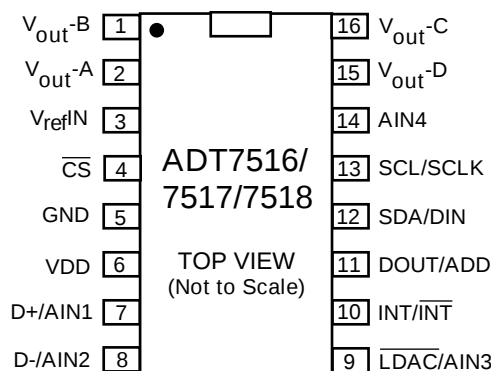
¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

²Values relate to package being used on a 4-layer board.

³Junction-to-Case resistance is applicable to components featuring a preferential flow direction, eg. components mounted on a heat sink. Junction-to-Ambient resistance is more useful for air-cooled PCB-mounted components.

Table 1. I²C Address Selection

ADD Pin	I ² C Address
Low	1001 000
Float	1001 010
High	1001 011

PIN CONFIGURATION
QSOP

ORDERING GUIDE

Model	Temperature Range	DAC Resolution	Package Description	Package Options
ADT7518ARQ	-40°C to +125°C	8-Bits	16-Lead QSOP	RQ-16
ADT7517ARQ	-40°C to +125°C	10-Bits	16-Lead QSOP	RQ-16
ADT7516ARQ	-40°C to +125°C	12-Bits	16-Lead QSOP	RQ-16

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADT7516/7517/7518 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



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ADT7516/7517/7518 PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	V _{OUTB}	Buffered Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
2	V _{OUTA}	Buffered Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
3	V _{REFIN}	Reference Input Pin for all four DACs. This input is buffered and has an input range from 1 V to V _{DD} .
4	$\overline{CS}$	SPI - Active low control Input. This is the frame synchronization signal for the input data. When $\overline{CS}$ goes low, it enables the input register and data is transferred in on the rising edges and out on the falling edges of the subsequent serial clocks. It is recommended that this pin be tied high to V _{DD} when operating the serial interface in I ² C mode.
5	GND	Ground Reference Point for All Circuitry on the part. Analog and Digital Ground.
6	V _{DD}	Positive Supply Voltage, +2.7 V to +5.5 V. The supply should be decoupled to ground.
7	D+/AIN1	D+. Positive connection to external temperature sensor. AIN1. Analog Input. Single ended analog input channel. Input range is 0 V to 2.25 V or 0 V to 5 V.
8	D-/AIN2	D-. Negative connection to external temperature sensor. AIN2. Analog Input. Single ended analog input channel. Input range is 0 V to 2.25 V or 0 V to 5 V.
9	$\overline{LDAC}$ /AIN3	$\overline{LDAC}$. Active low control input that transfers the contents of the input registers to their respective DAC registers. A falling edge on this pin forces any or all DAC registers to be updated if the input registers have new data. A minimum pulse width of 20ns must be applied to the $\overline{LDAC}$ pin to ensure proper loading of a DAC register. This allows simultaneous update of all DAC outputs. Bit C3 of Control Configuration 3 register enables $\overline{LDAC}$ pin. Default is with LDAC pin controlling the loading of DAC registers. AIN3. Analog Input. Single ended analog input channel. Input range is 0 V to 2.25 V or 0 V to 5 V.
10	INT/ $\overline{INT}$	Over Limit Interrupt. The output polarity of this pin can be set to give an active low or active high interrupt when temperature, V _{DD} or AIN limits are exceeded. Default is active low.
11	DOUT/ADD	SPI Serial Data Output. Logic Output. Data is clocked out of any register at this pin. Data is clocked out on the falling edge of SCLK. Open Drain output - needs a pullup resistor. ADD - I ² C serial bus address selection pin. Logic input. A low on this pin gives the address 1001 000, leaving it floating gives the address 1001 010 and setting it high gives the address 1001 011. The I ² C address set up by the ADD pin is not latched by the device until after this address has been sent twice. On the 8 th SCL cycle of the second valid communication, the serial bus address is latched in. Any subsequent changes on this pin will have no affect on the I ² C serial bus address.
12	SDA/DIN	SDA. I ² C Serial Data Input. I ² C serial data to be loaded into the parts registers is provided on this input. DIN. SPI Serial Data Input. Serial data to be loaded into the parts registers is provided on this input. Data is clocked into a register on the rising edge of SCLK.
13	SCL/SCLK	Serial Clock Input. This is the clock input for the serial port. The serial clock is used to clock data out of any register of the ADT7516/7517/7518 and also to clock data into any register that can be written to.
14	AIN4	Analog input. Single ended analog input channel. Input range is 0 V to 2.25 V or 0 V to 5 V.
15	V _{OUTD}	Buffered Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation.
16	V _{OUTC}	Buffered Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation.

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TERMINOLOGY**RELATIVE ACCURACY**

Relative accuracy or integral nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. Typical INL versus Code plots can be seen in TPCs 1, 2, and 3.

DIFFERENTIAL NONLINEARITY

Differential Nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ± 1 LSB maximum ensures monotonicity. The DAC and ADC are guaranteed monotonic by design. Typical DAC DNL versus Code plots can be seen in TPCs 4, 5, and 6.

OFFSET ERROR

This is a measure of the offset error of the DAC and the output amplifier. (See Figures 5 and 6.) It can be negative or positive. It is expressed in mV.

OFFSET ERROR MATCH

This is the difference in Offset Error between any two channels

GAIN ERROR

This is a measure of the span error of the DAC. It is the deviation in slope of the actual DAC transfer characteristic from the ideal expressed as a percentage of the full-scale range.

GAIN ERROR MATCH

This is the difference in Gain error between any two channels.

OFFSET ERROR DRIFT

This is a measure of the change in offset error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

GAIN ERROR DRIFT

This is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

LONG TERM TEMPERATURE DRIFT

This is a measure of the change in temperature error with the passage of time. It is expressed in °C/1000hrs. The concept of long-term stability has been used for many years to describe by what amount an IC's parameter would shift during its lifetime. This is a concept that has been typically applied to both voltage references and monolithic temperature sensors. Unfortunately, integrated circuits cannot be evaluated at room temperature (25°C) for 10 years or so to determine this shift. As a result, manufacturers very typically perform accelerated life-time testing of integrated circuits by operating ICs at elevated temperatures (between 125°C and 150°C) over a shorter period of time (typically, between 500 and 1000 hours). As a result of this operation, the lifetime of an integrated circuit

is significantly accelerated due to the increase in rates of reaction within the semiconductor material. As a result of this operation, the lifetime of an integrated circuit is significantly accelerated due to the increase in rates of reaction within the semiconductor material.

DC POWER-SUPPLY REJECTION RATIO (PSRR)

This indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. It is measured in dBs. V_{REF} is held at 2 V and V_{DD} is varied $\pm 10\%$.

DC CROSSTALK

This is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC while monitoring another DAC. It is expressed in μV .

REFERENCE FEEDTHROUGH

This is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated (i.e., $\overline{LDAC}$ is high). It is expressed in dBs.

CHANNEL-TO-CHANNEL ISOLATION

This is the ratio of the amplitude of the signal at the output of one DAC to a sine wave on the reference input of another DAC. It is measured in dBs.

MAJOR-CODE TRANSITION GLITCH ENERGY

Major-code transition glitch energy is the energy of the impulse injected into the analog output when the code in the DAC register changes state. It is normally specified as the area of the glitch in nV secs and is measured when the digital code is changed by 1 LSB at the major carry transition (011...11 to 100...00 or 100...00 to 011...11).

DIGITAL FEEDTHROUGH

Digital feedthrough is a measure of the impulse injected into the analog output of a DAC from the digital input pins of the device but is measured when the DAC is not being written to. It is specified in nV secs and is measured with a full-scale change on the digital input pins, i.e., from all 0s to all 1s or vice versa.

DIGITAL CROSSTALK

This is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is measured in stand-alone mode and is expressed in nV secs.

ANALOG CROSSTALK

This is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s and vice versa) while keeping $\overline{LDAC}$ high. Then pulse $\overline{LDAC}$ low and monitor the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nV secs.

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DAC-TO-DAC CROSSTALK

This is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s and vice versa) with $\overline{\text{LDAC}}$ low and monitoring the output of another DAC. The energy of the glitch is expressed in nV secs.

MULTIPLYING BANDWIDTH

The amplifiers within the DAC have a finite bandwidth. The multiplying bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

TOTAL HARMONIC DISTORTION

This is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measure of the harmonics present on the DAC output. It is measured in dBs.

ROUND ROBIN

This term is used to describe the ADT7516/17/18 cycling through the available measurement channels in sequence, taking a measurement on each channel.

DAC OUTPUT SETTLING TIME

This is the time required, following a prescribed data change, for the output of a DAC to reach and remain within ± 0.5 LSB of the final value. A typical prescribed change is from 1/4 scale to 3/4 scale.

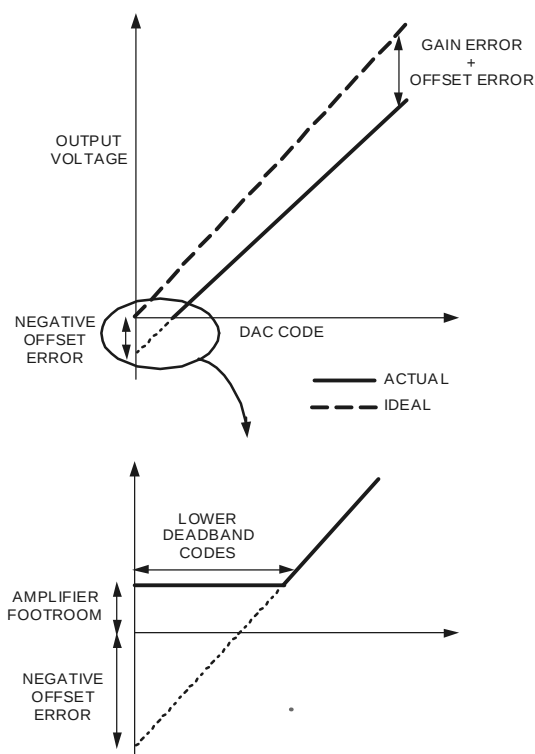


Figure 5. DAC Transfer Function with Negative Offset

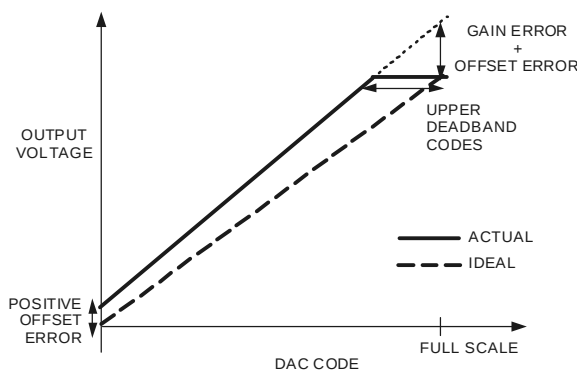
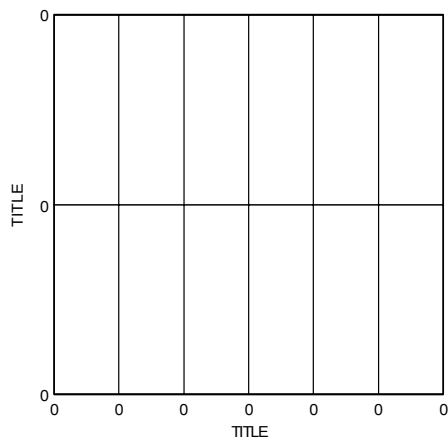


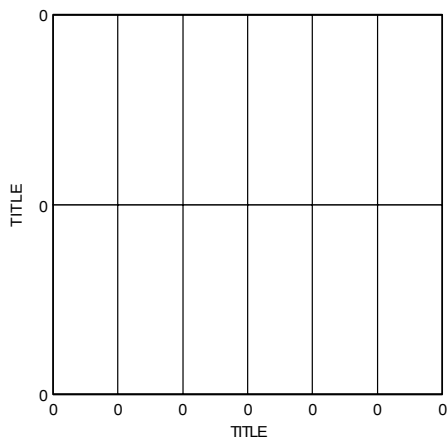
Figure 6. DAC Transfer Function with Positive Offset ($V_{\text{REF}} = V_{\text{DD}}$)

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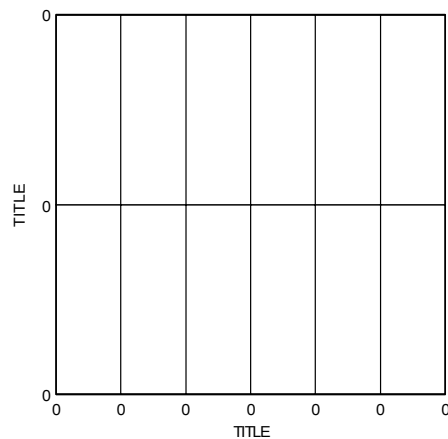
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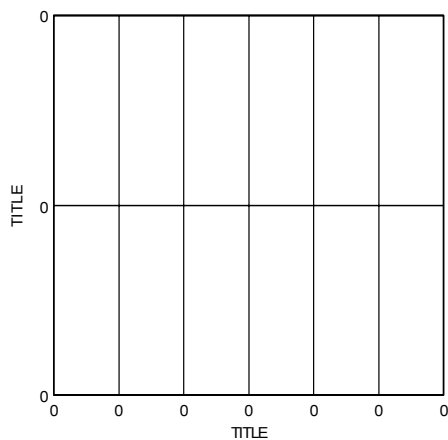
TPC 1. ADT7518 Typical DAC INL Plot



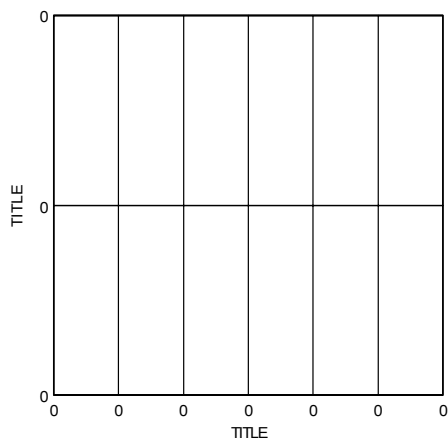
TPC 2. ADT7517 Typical DAC INL Plot



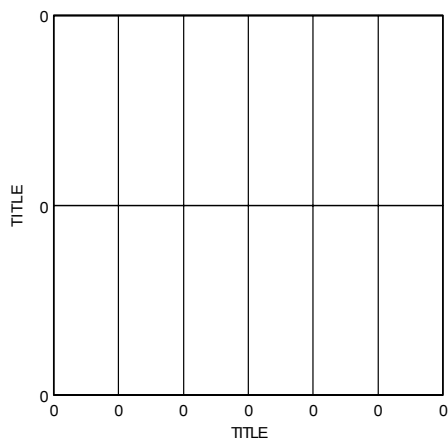
TPC 3. ADT7516 Typical DAC INL Plot



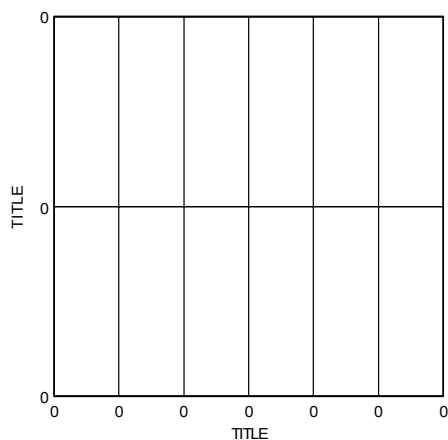
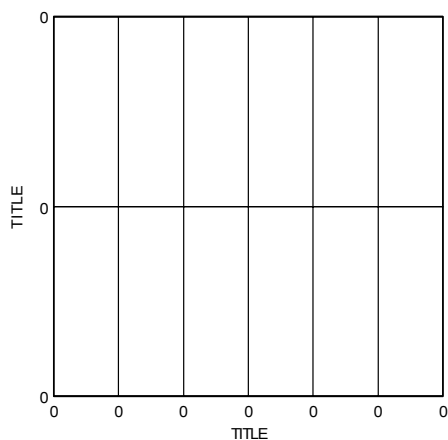
TPC 4. ADT7518 Typical DAC DNL Plot



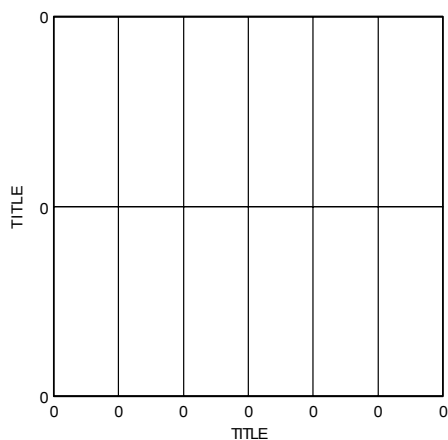
TPC 5. ADT7517 Typical DAC DNL Plot



TPC 6. ADT7516 Typical DAC DNL Plot

TPC 7. ADT7518 DAC INL and DNL Error vs V_{REF} 

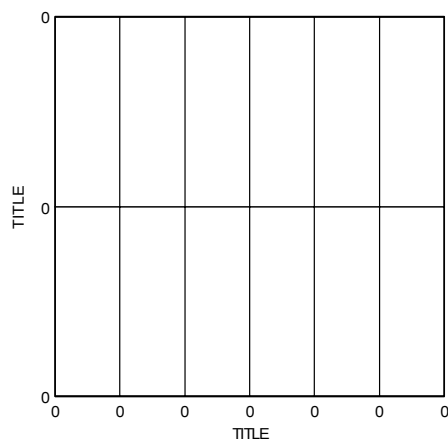
TPC 8. ADT7518 DAC INL Error and DNL Error vs Temperature



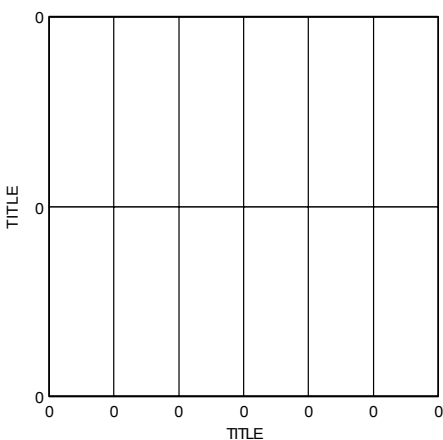
TPC 9. ADT7518 DAC Offset Error and Gain Error vs Temperature

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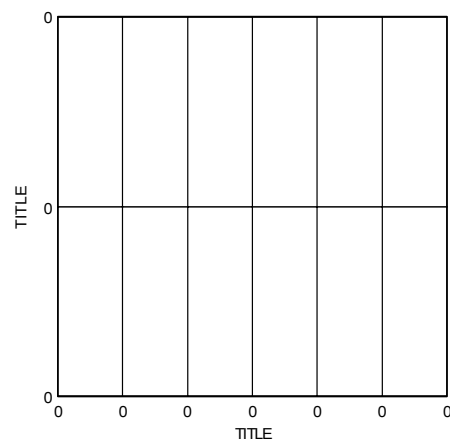
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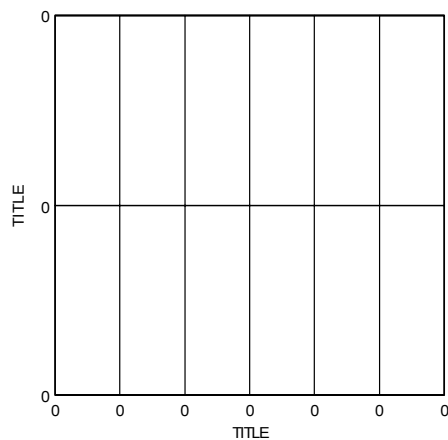
TPC 10. DAC Offset Error and Gain Error vs V_{DD}



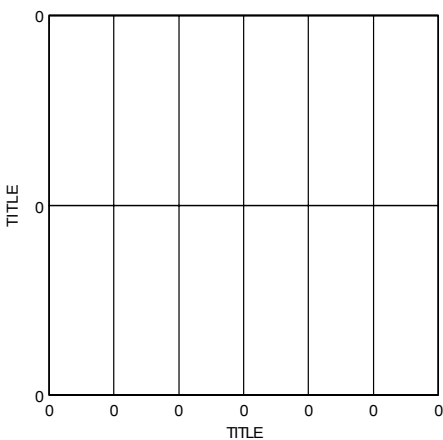
TPC 11. DAC V_{OUT} Source and Sink Current Capability



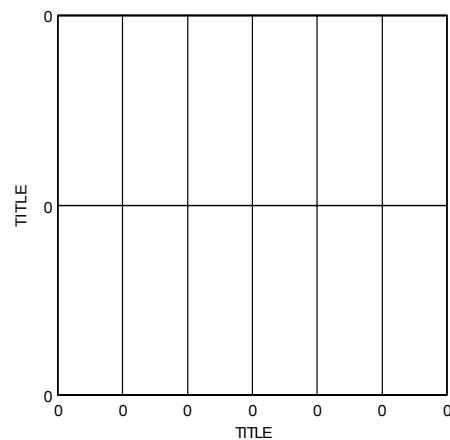
TPC 12. Supply Current vs. DAC Code



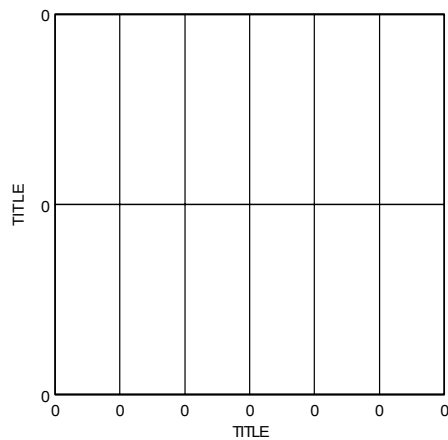
TPC 13. Supply Current vs. Supply Voltage



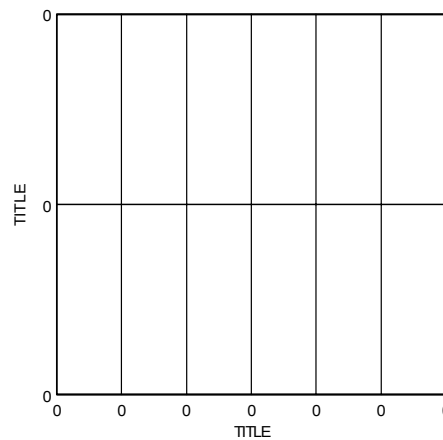
TPC 14. Power-Down Current vs. Supply Voltage



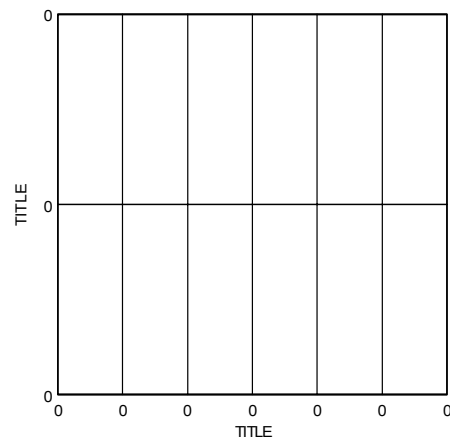
TPC 15. DAC Half-Scale Settling (1/4 to 3/4 Scale Code Change)



TPC 16. Exiting Power-Down to Midscale



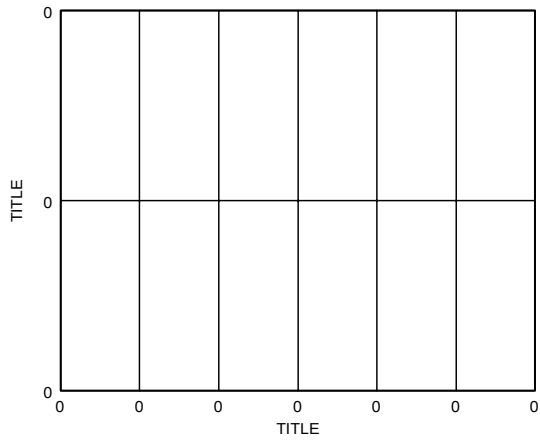
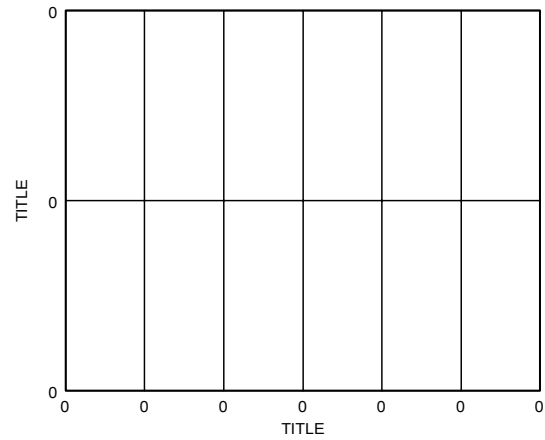
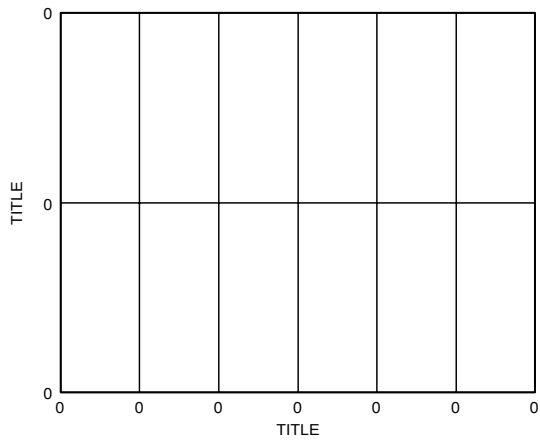
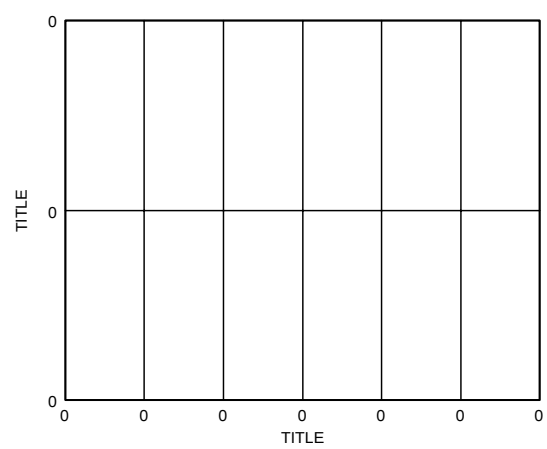
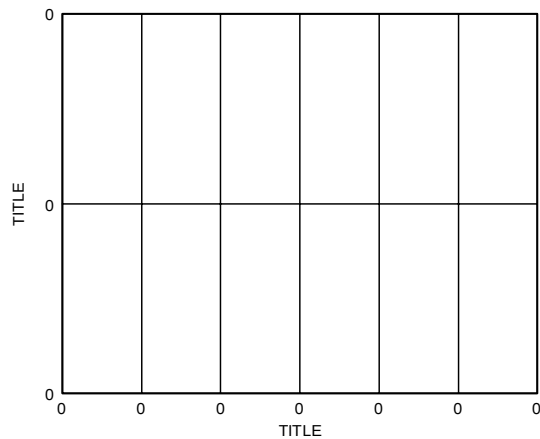
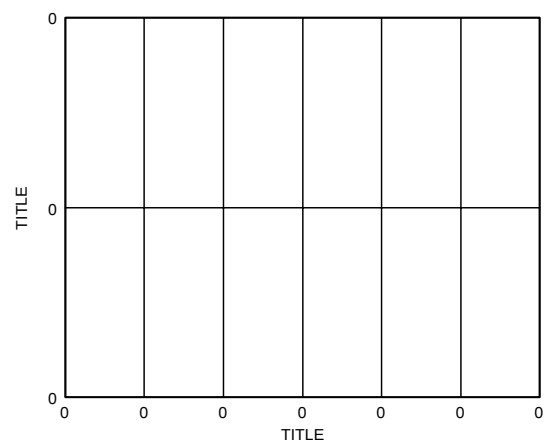
TPC 17. ADT7516 DAC Major-Code Transition Glitch Energy



TPC 18. DAC Multiplying Bandwidth (Small-Signal Frequency Response)

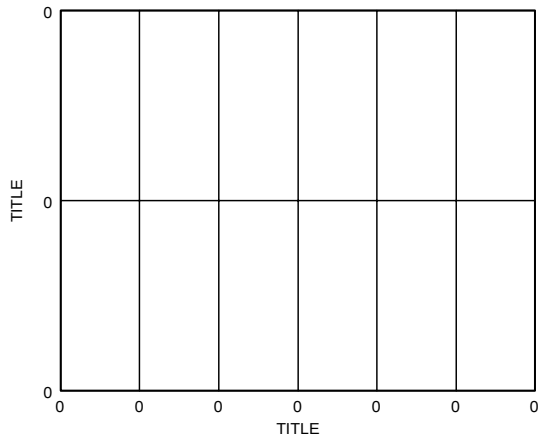
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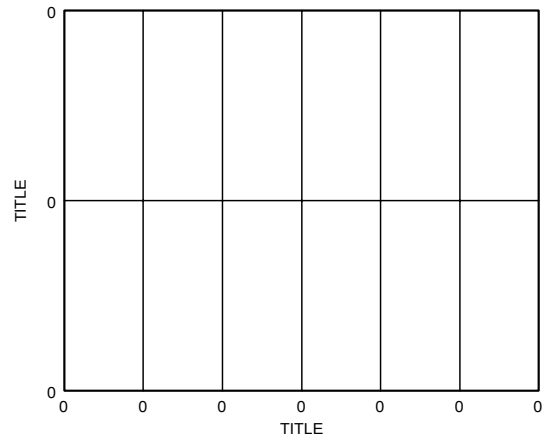
*TPC 19. DAC Full-Scale Error vs. V_{REF}* *TPC 20. DAC-to-DAC Crosstalk**TPC 21. ADC DNL**TPC 22. ADC INL**TPC 23. PSRR vs Supply Ripple Frequency**TPC 24. Temperature Error @ 3.3 V and 5 V*

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TPC 25. ADC Offset Error and Gain Error vs Temperature



TPC 26. ADC Offset Error and Gain Error vs V_{DD}

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ADT7516/17/18 OPERATION

Directly after the power-up calibration routine the ADT7516/17/18 goes into idle mode. In this mode the device is not performing any measurements and is fully powered up. All four DAC outputs are at 0V.

To begin monitoring, write to Control Configuration 1 (address = 18h) register and set bit C0 = 1. The ADT7516/17/18 goes into its power-up default measurement mode, which is Round Robin. The device proceeds to take measurements on the V_{DD} channel, internal temperature sensor channel, external temperature sensor channel or AIN1 and AIN2, AIN3 and finally AIN4. Once it finishes taking measurements on the AIN4 channel the device immediately loops back to start taking measurements on the V_{DD} channel and repeats the same cycle as before. This loop continues until the monitoring is stopped by resetting bit C0 of Control Configuration 1 register to 0. It is also possible to continue monitoring as well as switching to Single channel mode by writing to Control Configuration 2 register (address = 19h) and setting bit C4 = 1. Further explanation of the Single channel and Round Robin measurement modes are given in later sections. All measurement channels have averaging enabled on them on power-up. Averaging forces the device to take an average of 16 readings before giving a final measured result. To disable averaging and consequently decrease the conversion time by a factor of 16, set C5 = 1 in Control Configuration 2 register.

There are four single ended analog input channels on the ADT7516/17/18, AIN1 to AIN4. AIN1 and AIN2 are multiplexed with the external temperature sensors D+ and D- terminals. Bits C1 and C2 of Control Configuration 1 register (address = 18h) are used to select between AIN1/2 and external temperature sensor. The input range on the analog input channels is dependent on whether the ADC reference used is the internal V_{REF} or V_{DD} . To meet linearity specifications, it is recommended that the maximum V_{DD} value is 5 V. Bit C4 of Control Configuration 3 register is used to select between the internal reference or V_{DD} as the analog inputs ADC reference.

Controlling the DAC outputs can be done by writing to the DACs MSB and LSB registers (addresses 10h - 17h). The power-up default setting is to have a low going pulse on the LDAC pin (pin 9) controlling the updating of the DAC outputs from the DAC registers. You can configure the updating of the DAC outputs to be controlled by methods other than the LDAC pin by setting C3 = 1 of the Control Configuration 3 register (address = 1Ah). The DAC Configuration register (address = 1Bh) and the LDAC Configuration register (address = 1Ch) can now be used to control the DAC updating. These two registers also control the output range of the DACs and selecting between the internal or external reference. DAC A and DAC B outputs can be configured to give a voltage output proportional to the temperature of the internal and external temperature sensors respectively.

The dual serial interface defaults to the I²C protocol on power-up. To select and lock in the SPI protocol please follow the selection process as described in the Serial Interface Selection section. The I²C protocol cannot be

locked in, while the SPI protocol on selection is automatically locked in. The interface can only be switched back to be I²C when the device is powered off and on. When using I²C the $\overline{CS}$ pin should be tied to either V_{DD} or GND.

There are a number of different operating modes on the ADT7516/17/18 devices and all of them can be controlled by the configuration registers. These features consist of the INT/ $\overline{INT}$ pin, enabling and disabling interrupts, polarity of the INT/ $\overline{INT}$ pin, enabling and disabling the averaging on the measurement channels, SMBus timeout and software reset.

POWER-UP CALIBRATION

It is recommended that no communication to the part is initiated until approximately 5ms after V_{DD} has settled to within 10% of its final value. It is generally accepted that most systems take a maximum of 50ms to power-up. Power-up time is directly related to the amount of decoupling on the voltage supply line.

During this 5ms after V_{DD} has settled, the part is performing a calibration routine and any communication to the device will interrupt this routine and could cause erroneous temperature measurements. If it not possible to have V_{DD} at its nominal value by the time 50ms has elapsed or that communication to the device has started prior to V_{DD} settling then it is recommended that a measurement be taken on the V_{DD} channel before a temperature measurement is taken. The V_{DD} measurement is used to calibrate out any temperature measurement error due to different supply voltage values.

FUNCTIONAL DESCRIPTION - VOLTAGE OUTPUT**DAC**

The ADT7516/7517/7518 has four resistor-string DACs fabricated on a CMOS process with resolutions of 12, 10 and 8 bits respectively. They contain four output buffer amplifiers and is written to via I²C serial interface or SPI serial interface. See Serial Interface Selection section for more information.

The ADT7516/7517/7518 operates from a single supply of 2.7 V to 5.5 V and the output buffer amplifiers provide rail-to-rail output swing with a slew rate of 0.7 V/ μ s. All four DACs share a common reference input, namely V_{REFIN} . The reference input is buffered to draw virtually no current from the reference source as it offers the source a high impedance input. The devices have a power-down mode, in which all DACs may be turned off completely with a high-impedance output.

Each DAC output will not be updated until it receives the LDAC command. Therefore while the DAC registers would have been written to with a new value, this value will not be represented by a voltage output until the DACs have received the LDAC command. Reading back from any DAC register prior to issuing an LDAC command will result in the digital value that corresponds to the DAC output voltage. Thus the digital value written to the DAC register cannot be read back until after the LDAC command has been initiated. This LDAC command can

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be given by either pulling the $\overline{\text{LDAC}}$ pin low (falling edge loads DACs), setting up Bits D4 and D5 of DAC Configuration register (address = 1Bh) or using the LDAC register (address = 1Ch).

When using the $\overline{\text{LDAC}}$ pin to control DAC register loading, the low going pulse width should be 20ns minimum. The $\overline{\text{LDAC}}$ pin has to go high and low again before the DAC registers can be reloaded.

Digital-to-Analog Section

The architecture of one DAC channel consists of a resistor-string DAC followed by an output buffer amplifier. The voltage at the V_{REFIN} pin or the on-chip reference of 2.25 V provides the reference voltage for the corresponding DAC. Figure 7 shows a block diagram of the DAC architecture. Since the input coding to the DAC is straight binary, the ideal output voltage is given by:

$$V_{\text{OUT}} = \frac{V_{\text{REF}} * D}{2^N}$$

where D=decimal equivalent of the binary code which is loaded to the DAC register;

0-255 for ADT7518 (8-Bits)

0-1023 for ADT7517 (10-Bits)

0-4095 for ADT7516 (12-Bits)

N = DAC resolution.

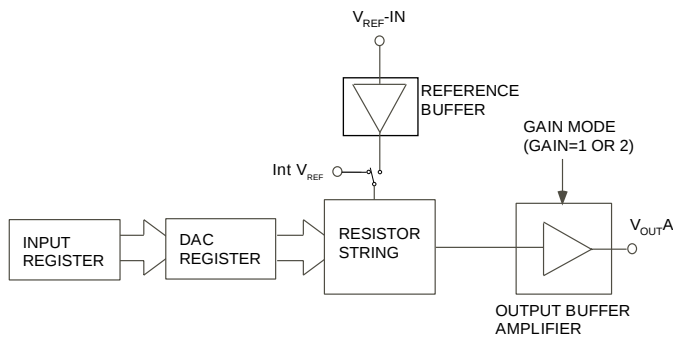


Figure 7. Single DAC channel architecture

Resistor String

The resistor string section is shown in Figure 8. It is simply a string of resistors, each of value 603Ω approximately. The digital code loaded to the DAC register determines at what node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

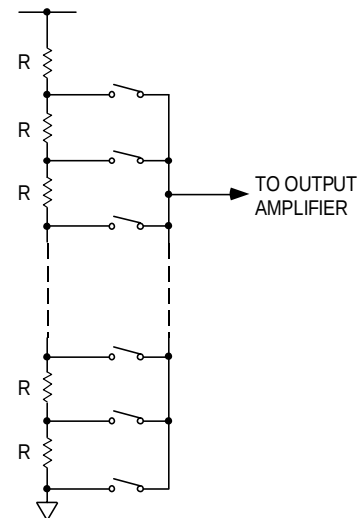


Figure 8. Resistor String

DAC Reference Inputs

There is an input reference pin for the DACs. This reference input is buffered.

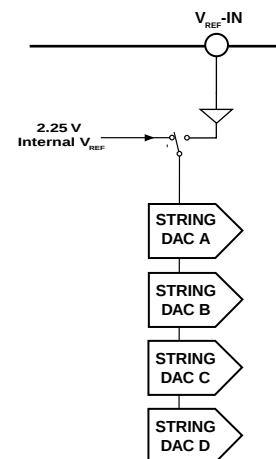


Figure 9. DAC Reference Buffer Circuit

The advantage with the buffered input is the high impedance it presents to the voltage source driving it. The user can have an external reference voltage as low as 1 V and as high as V_{DD} . The restriction of 1 V is due to the footroom of the reference buffer.

The LDAC Configuration register controls the option to select between internal and external voltage references. The default setting is for external reference selected.

Output Amplifier

The output buffer amplifier is capable of generating output voltages to within 1mV of either rail. Its actual range depends on the value of V_{REF} , GAIN and offset error. If a gain of 1 is selected (Bits 0-3 of DAC Configuration register = 0) the output range is 0.001 V to V_{REF} . If a gain of 2 is selected (Bits 0-3 of DAC Configuration register = 1) the output range is 0.001 V to $2V_{\text{REF}}$. However because of clamping the maximum output is limited to $V_{\text{DD}} - 0.001\text{V}$.

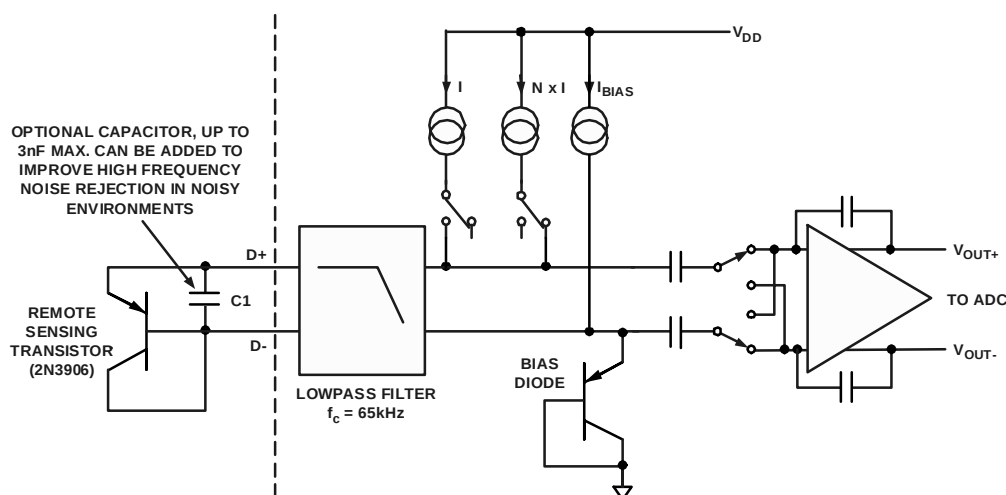


Figure 10. Signal Conditioning for External Diode Temperature Sensor

The output amplifier is capable of driving a load of $4k7\Omega$ to GND or V_{DD} , in parallel with $200pF$ to GND or V_{DD} . See Figure 4. The source and sink capabilities of the output amplifier can be seen in the plot in TPC 11.

The slew rate is $0.7V/\mu s$ with a half-scale settling time to ± 0.5 LSB (at 8 bits) of $6\mu s$.

THERMAL VOLTAGE OUTPUT

The ADT7516/17/18 has the capability of outputting a voltage that is proportional to temperature. DAC A output can be configured to represent the temperature of the internal sensor while DAC B output can be configured to represent the external temperature sensor. Bits C5 and C6 of Control Configuration 3 register select the temperature proportional output voltage. Each time a temperature measurement is taken the DAC output is updated. The output resolution for the ADT7518 is 8 bits with $1^\circ C$ change corresponding to one LSB change. The output resolution for the ADT7516 and ADT7517 is capable of 10 bits with $0.25^\circ C$ change corresponding to one LSB change. The default output resolution for the ADT7516 and ADT7517 is 8 bits. To increase this to 10 bits, set C1 = 1 of Control Configuration 3 register. The default output range is $0V-V_{REF}$ and this can be increased to $0V-2V_{REF}$. Increasing the output voltage span to $2V_{REF}$ can be done by setting D0 = 1 for DAC A (Internal Temperature Sensor) and D1 = 1 for DAC B (External Temperature Sensor) in DAC Configuration register (address 1Bh).

The output voltage is capable of tracking a max temperature range of $-128^\circ C$ to $+127^\circ C$ but the default setting is $-40^\circ C$ to $+127^\circ C$. If the output voltage range is $0V-V_{REF}$ ($V_{REF} = 2.25V$) then this corresponds to $0V$ representing $-40^\circ C$ and $1.48V$ representing $+127^\circ C$. This of course will give an upper deadband between $1.48V$ and V_{REF} .

The Internal and External Analog Temperature Offset registers can be used to vary this upper deadband and consequently the temperature that $0V$ corresponds to. Tables 2 and 3 give examples of how this is done using a DAC

output voltage span of V_{REF} and $2V_{REF}$ respectively. Simply write in the temperature value, in 2's complement format, that you want $0V$ to start at. For example, if you are using the DAC A output and you want $0V$ to start at $-40^\circ C$ then program D8h into the Internal Analog Temperature Offset register (address 21h). This is an 8-bit register and thus only has a temperature offset resolution of $1^\circ C$ for all device models. Use the following formulas to determine the value to program into the offset registers.

Negative temperatures : -

$$\text{Offset Register Code(d)}^* = (0V \text{ Temp}) + 128$$

*D7 of Offset Register Code is set to 1 for negative temperatures.

Example :

$$\begin{aligned} \text{Offset Register Code(d)} &= (-40) + 128 \\ &= 88d = 58h \end{aligned}$$

Since a negative temperature has been inputted into the equation, DB7 (MSB) of the Offset Register code is set to a 1. Therefore $58h$ becomes $D8h$.

$$58h + DB7(1) \Rightarrow D8h$$

Positive temperatures : -

$$\text{Offset Register Code(d)} = 0V \text{ Temp}$$

Example :

$$\text{Offset Register Code (d)} = 10d = 0Ah$$

Table 2. Thermal Voltage Output ($0V-V_{REF}$)

O/P Voltage	Default $^\circ C$	Max $^\circ C$	Sample $^\circ C$
0V	-40	-128	0
0.5V	+17	-71	+56
1V	+73	-15	+113
1.12V	+87	-1	+127

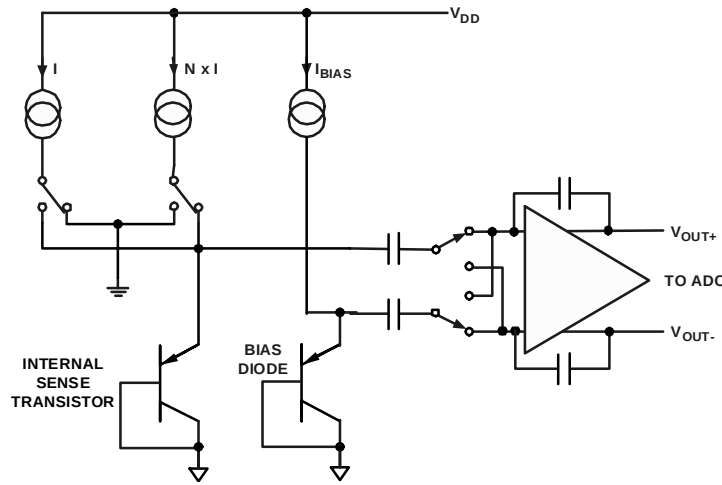


Figure 11. Top Level Structure of Internal Temperature Sensor

1.47V	+127	+39	UDB*
1.5V	UDB*	+42	UDB*
2V	UDB*	+99	UDB*
2.25V	UDB*	+127	UDB*

* Upper deadband has been reached. DAC output is not capable of increasing. Reference Figure 6.

Table 3. Thermal Voltage Output, (0V-2V_{REF})

O/P Voltage	Default °C	Max °C	Sample °C
0V	-40	-128	0
0.25V	-26	-114	14
0.5V	+12	-100	+28
0.75V	+3	-85	43
1V	+17	-71	+57
1.12V	+23	-65	+63
1.47V	+43	-45	+83
1.5V	+45	-43	+85
2V	+73	-15	+113
2.25V	+88	0	+127
2.5V	+102	+14	UDB*
2.75V	+116	+28	UDB*
3V	UDB*	+42	UDB*
3.25V	UDB*	+56	UDB*
3.5V	UDB*	+70	UDB*
3.75V	UDB*	+85	UDB*
4V	UDB*	+99	UDB*
4.25V	UDB*	+113	UDB*

4.5V	UDB*	+127	UDB*
------	------	------	------

* Upper deadband has been reached. DAC output is not capable of increasing. Reference Figure 6.

The following equation is used to work out the various temperatures for the corresponding 8-bit DAC output :-

$$8\text{-Bit Temp} = (\text{DAC O/P} \div 1 \text{ LSB}) + (0\text{V Temp})$$

For example, if the output is 1.5V, V_{REF} = 2.25 V, 8-bit DAC has an LSB size = 2.25V/256 = 8.79x10⁻³, and 0V Temp is at -128°C then the resultant temperature works out to be :-

$$(1.5 \div 8.79 \times 10^{-3}) + (-128) = +43^{\circ}\text{C}$$

The following equation is used to work out the various temperatures for the corresponding 10-bit DAC output :-

$$10\text{-Bit Temp} = ((\text{DAC O/P} \div 1 \text{ LSB}) \times 0.25) + (0\text{V Temp})$$

For example, if the output is 0.4991V, V_{REF} = 2.25 V, 10-bit DAC has an LSB size = 2.25V/1024 = 2.197x10⁻³, and 0V Temp is at -40°C then the resultant temperature works out to be :-

$$((0.4991 \div 2.197 \times 10^{-3}) \times 0.25) + (-40) = +16.75^{\circ}\text{C}$$

Figure 12 shows a graph of DAC output vs temperature for a V_{REF} = 2.25 V.

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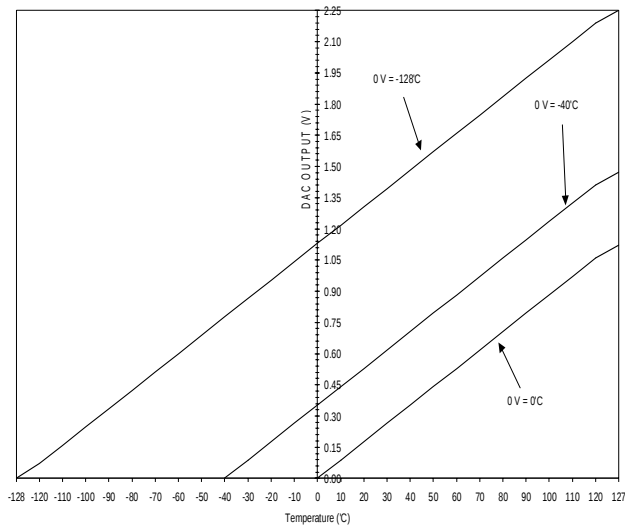


Figure 12. DAC Output vs Temperature, $V_{REF} = 2.25\text{ V}$

FUNCTIONAL DESCRIPTION - ANALOG INPUTS

SINGLE-ENDED INPUTS

The ADT7516/17/18 offers four single-ended analog input channels. The analog input range is between 0 V to 2.25 V or 0 V to V_{DD} . To maintain the linearity specification it is recommended that the maximum V_{DD} value be set at 5 V. Selection between the two input ranges is done by Bit C4 of Control Configuration 3 Register (Address = 1Ah). Setting this bit to 0 sets up the analog input ADC reference to be sourced from the internal voltage reference of 2.25 V. Setting the bit to 1 sets up the ADC reference to be sourced from V_{DD} .

The ADC resolution is 10 bits and is mostly suitable for DC input signals. Bits C1:2 of Control Configuration 1 register (Address = 18h) are used to set up pins 7 and 8 as AIN1 and AIN2. Figure 13 shows the overall view of the four channel analog input path.

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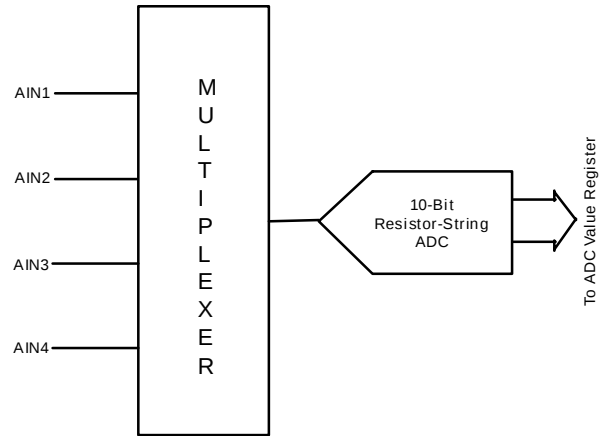


Figure 13. Quad Analog Input Path

CONVERTER OPERATION

The analog input channels use a successive approximation ADC based around a resistor-string DAC. Figures 14 and 15 show simplified schematics of the ADC. Figure 14 shows the ADC during acquisition phase. SW2 is closed and SW1 is in position A. The comparator is held in a balanced condition and the sampling capacitor acquires the signal on AIN.

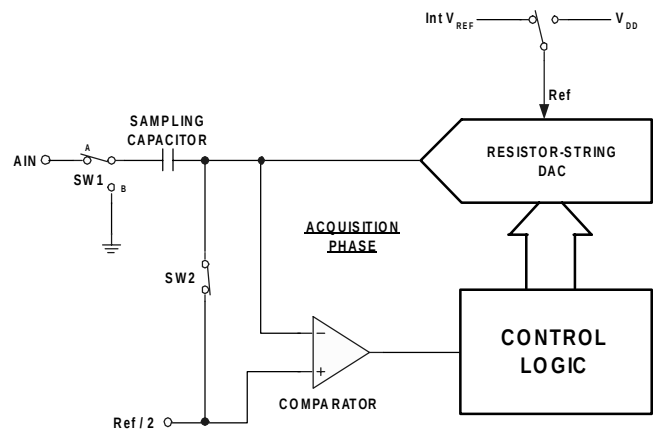


Figure 14. ADC Acquisition Phase

When the ADC eventually goes into conversion phase, see Figure 15, SW2 opens and SW1 moves to position B causing the comparator to become unbalanced. The control logic and the DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced the conversion is complete. The control logic generates the ADC output code. Figure 16 shows the ADC transfer function for the analog inputs.

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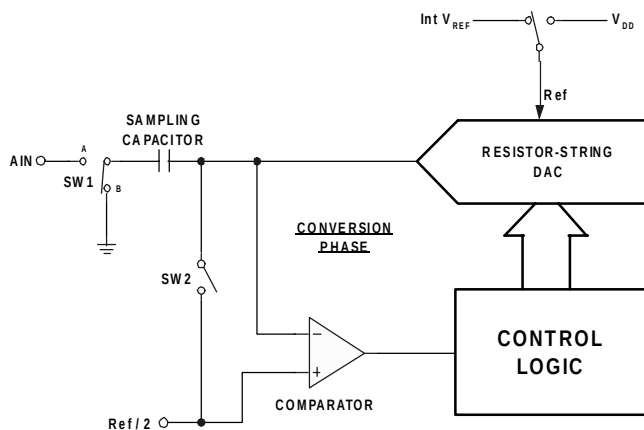


Figure 15. ADC Conversion Phase

ADC TRANSFER FUNCTION

The output coding of the ADT7516/17/18 analog inputs is straight binary. The designed code transitions occur midway between successive integer LSB values (i.e. 1/2LSB, 3/2LSB, etc.). The LSB is $V_{DD}/1024$ or $\text{Int } V_{REF}/1024$, $\text{Int } V_{REF} = 2.25 \text{ V}$. The ideal transfer characteristic is shown in figure 16 below.

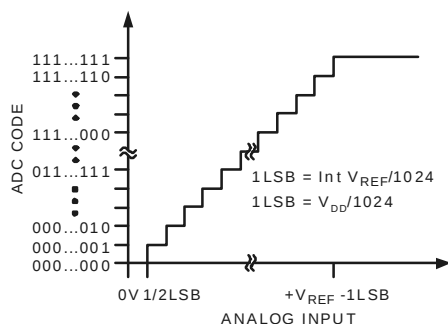


Figure 16. Single-Ended Transfer Function

To work out the voltage on any analog input channel, the following method can be used:

$$1 \text{ LSB} = \text{Reference (v)} / 1024$$

Convert value read back from AIN Value register into decimal.

$$\text{AIN Voltage} = \text{AIN Value (d)} \times \text{LSB size}$$

d = decimal

Example:

Internal Reference used. Therefore $V_{ref} = 2.25 \text{ V}$.

AIN Value = 512d

$$1 \text{ LSB size} = 2.25 \text{ V} / 1024 = 2.197 \times 10^{-3}$$

$$\begin{aligned} \text{AIN Voltage} &= 512 \times 2.197 \times 10^{-3} \\ &= 1.125 \text{ V} \end{aligned}$$

ANALOG INPUT ESD PROTECTION

Figure 17 shows the input structure on any on the analog input pins that provides ESD protection. The diode provides the main ESD protection for the analog inputs. Care

must be taken that the analog input signal never drops below the GND rail by more than 200mV. If this happens then the diode will become forward biased and start conducting current into the substrate. The 4pF capacitor is the typical pin capacitance and the resistor is a lumped component made up of the on-resistance of the multiplexer switch.

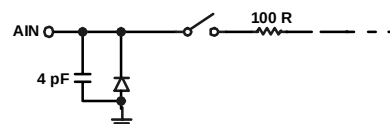


Figure 17. Equivalent Analog Input ESD Circuit

AIN INTERRUPTS

The measured results from the AIN inputs are compared with the AIN V_{HIGH} (greater than comparison) and V_{LOW} (less than and equal to comparison) limits. An interrupt occurs if the AIN inputs exceed or equal the limit registers. These voltage limits are stored in on-chip registers. Please note that the limit registers are 8 bits long while the AIN conversion result is 10 bits long. If the voltage limits are not masked out then any out of limit comparisons generate flags that are stored in Interrupt Status 1 Register (address = 00h) and one or more out-of limit results will cause the INT/INT pin to pull either high or low depending on the output polarity setting. It is good design practice to mask out interrupts for channels that are of no concern to the application.

Figure 18 shows the interrupt structure for the ADT7516/17/18. It gives a block diagram representation of how the various measurement channels affect the INT/INT pin.

FUNCTIONAL DESCRIPTION - MEASUREMENT**TEMPERATURE SENSOR**

The ADT7516/7517/7518 contains an A-D converter with special input signal conditioning to enable operation with external and on-chip diode temperature sensors. When the ADT7516/7517/7518 is operating in single channel mode, the A to D converter continually processes the measurement taken on one channel only. This channel is preselected by bits C0:C2 in Control Configuration 2 Register (address 19h). When in Round Robin mode the analog input multiplexer sequentially selects the V_{DD} input channel, the on-chip temperature sensor to measure its internal temperature, either the external temperature sensor or AIN1 and AIN2, AIN3 and then AIN4. These signals are digitized by the ADC and the results stored in the various Value Registers.

The measured results from the temperature sensors are compared with the Internal and External, T_{HIGH} , T_{LOW} limits. These temperature limits are stored in on-chip registers. If the temperature limits are not masked out then any out of limit comparisons generate flags that are stored in Interrupt Status 1 Register. One or more out-of

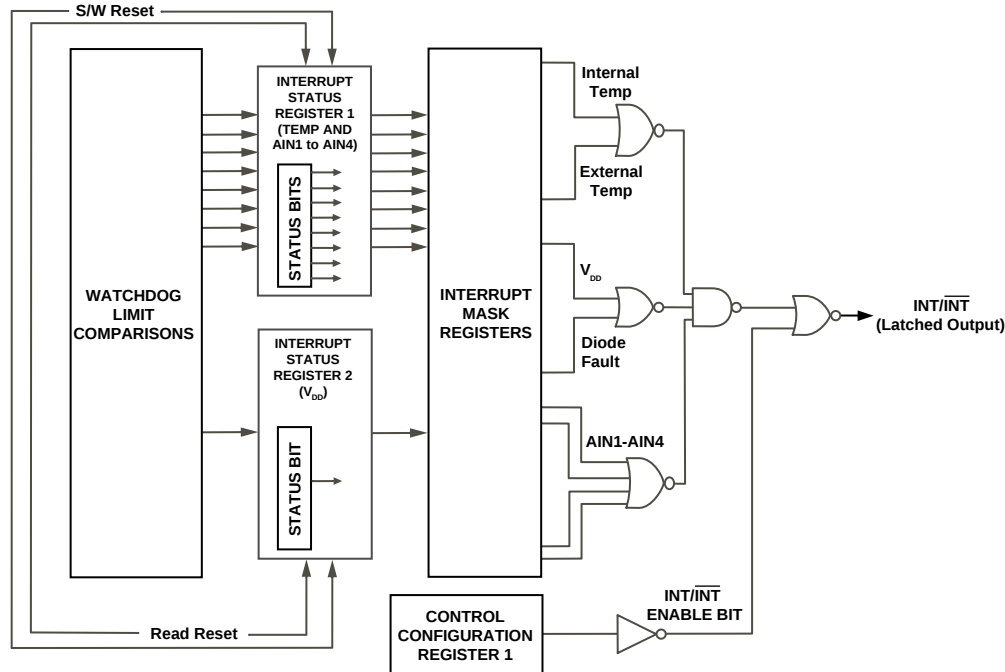


Figure 18. ADT7516/17/18 Interrupt Structure

limit results will cause the $\text{INT}/\overline{\text{INT}}$ output to pull either high or low depending on the output polarity setting.

Theoretically, the temperature sensor and ADC can measure temperatures from -128°C to $+127^{\circ}\text{C}$ with a resolution of 0.25°C . However, temperatures outside T_A are outside the guaranteed operating temperature range of the device. Temperature measurement from -128°C to $+127^{\circ}\text{C}$ is possible using an external sensor.

Temperature measurement is initiated by three methods. The first method is applicable when the part is in single channel measurement mode. The temperature is measured 16 times and internally averaged to reduce noise. The total time to measure a temperature channel is typically 25.92ms ($1.62\text{ms} \times 16$) for the internal temperature sensor and 16.8ms ($1.05\text{ms} \times 16$) for the external temperature sensor. The new temperature value is loaded into the Temperature Value Register and ready for reading by the I²C or SPI interface. The user has the option of disabling the averaging by setting a bit (Bit 5) in the Control Configuration Register 2 (address 19h). The ADT7516/7517/7518 defaults on power-up with the averaging enabled.

The second method is applicable when the part is in Round Robin measurement mode. The part measures both the internal and external temperature sensors as it cycles through all possible measurement channels. The two temperature channels are measured each time the part runs a round robin sequence. In round robin mode the part is continuously measuring all channels.

Temperature measurement is also initiated after every read or write to the part when the part is in either single channel measurement mode or Round Robin measurement mode. Once serial communication has started, any conversion in progress is stopped and the ADC reset. Conversion

will start again immediately after the serial communication has finished. The temperature measurement proceeds normally as described above.

V_{DD} MONITORING

The ADT7516/17/18 also has the capability of monitoring its own power supply. The part measures the voltage on its V_{DD} pin to a resolution of 10 bits. The resultant value is stored in two 8-bit registers, the two LSBs stored in register address 03h and the eight MSBs are stored in register address 06h. This allows the user to have the option of just doing a one byte read if 10-bit resolution is not important. The measured result is compared with V_{HIGH} and V_{LOW} limits. If the V_{DD} interrupt is not masked out then any out-of-limit comparison generates a flag in Interrupt Status 2 Register and one or more out-of-limit results will cause the $\text{INT}/\overline{\text{INT}}$ output to pull either high or low depending on the output polarity setting.

Measuring the voltage on the V_{DD} pin is regarded as monitoring a channel along with the Internal, External and AIN channels. You can select the V_{DD} channel for single channel measurement by setting Bit C4 = 1 and setting Bit C0 to Bit C2 to all 0's in Control Configuration 2 register.

When measuring the V_{DD} value the reference for the ADC is sourced from the Internal Reference. Table 4 shows the data format. As the max V_{CC} voltage measurable is 7 V, internal scaling is performed on the V_{CC} voltage to match the 2.25V internal reference value. Below is an example of how the transfer function works.

$$V_{DD} = 5 \text{ V}$$

$$\text{ADC Reference} = 2.25 \text{ V}$$

$$1 \text{ LSB} = \text{ADC Reference} / 2^{10}$$

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$$= 2.25 / 1024$$

$$= 2.197\text{mV}$$

$$\text{Scale Factor} = \text{Fullscale } V_{CC} / \text{ADC Reference}$$

$$= 7 / 2.25$$

$$= 3.11$$

$$\text{Conversion Result} = V_{DD} / ((7/\text{Scale Factor}) \times \text{LSB size})$$

$$= 5 / (3.11 \times 2.197\text{mV})$$

$$= 2\text{DBh}$$

TABLE 4. V_{DD} Data Format, $V_{REF} = 2.25\text{ V}$

V_{DD} Value	Digital Output	
	Binary	Hex
2.5 V	01 0110 1110	16E
3 V	01 1011 0111	1B7
3.5 V	10 0000 0000	200
4 V	10 0100 1001	249
4.5 V	10 1001 0010	292
5 V	10 1101 1011	2DB
5.5 V	11 0010 0100	324
6 V	11 0110 1101	36D
6.5 V	11 1011 0110	3B6
7 V	11 1111 1111	3FF

ON-CHIP REFERENCE

The ADT7516/17/18 has an on-chip 1.2 V band-gap reference which is gained up by a switched capacitor amplifier to give an output of 2.25 V. The amplifier is powered up for the duration of the device monitoring phase and is powered down once monitoring is disabled. This saves on current consumption. On power-up the default mode is to have the internal reference selected as the reference for the ADC. The ADC is used for measuring V_{DD} , internal temperature sensor, external temperature sensor and AIN inputs. The internal reference is always used when measuring V_{DD} , the internal and external temperature sensors. The external reference is the default power-up reference for the DACs.

ROUND ROBIN MEASUREMENT

On power-up the ADT7516/17/18 goes into Round Robin mode but monitoring is disabled. Setting Bit C0 of Configuration Register 1 to a 1 enables conversions. It sequences through all the available channels taking a measurement from each in the following order of V_{DD} , Internal temperature sensor, External temperature sensor/ (AIN1 and AIN2), AIN3 and AIN4. Pin 7 and pin 8 can be configured to be either external temperature sensor pins or stand alone analog input pins. Once conversion is completed on the AIN4 channel, the device loop around for another measurement cycle. This method of taking a measurement on all the channels in one cycle is called

Round Robin. Setting Bit 4 of Control Configuration 2 (address 19h) disables the Round Robin mode and in turn sets up the single channel mode. The single channel mode is where only one channel, eg. Internal temperature sensor, is measured in each conversion cycle.

The time taken to monitor all channels will normally not be of interest, as the most recently measured value can be read at any time.

For applications where the Round Robin time is important, it can be easily calculated.

As mentioned previously a conversion on the internal temperature channel takes 25.92 ms, on the external temperature channel it takes 16.8ms, on the V_{DD} and AIN channels it takes 712 us. These values are typical times and the channels have averaging on. This means that each channel is measured 16 times and internally averaged to reduce noise.

The total cycle time for V_{DD} , AIN1 to AIN4 and internal temperature is therefore nominally :

$$712\mu\text{s} + (4 \times 712\mu\text{s}) + 25.92\text{ms} = 29.48\text{ ms}$$

The total cycle time with averaging off is:

$$29.48\text{ ms} / 16 = 1.842\text{ ms}$$

The total cycle time for V_{DD} , AIN3, AIN4, internal temperature and external temperature is therefore nominally :

$$712\mu\text{s} + (2 \times 712\mu\text{s}) + 25.92\text{ms} + 16.8\text{ms} = 44.86\text{ ms}$$

The total cycle time with averaging off is:

$$44.86\text{ ms} / 16 = 2.8\text{ ms}$$

SINGLE CHANNEL MEASUREMENT

Setting C4 of Control Configuration 2 register enables the single channel mode and allows the ADT7516/17/18 to focus on one channel only. A channel is selected by writing to Bits C0:C2 in register Control Configuration 2 register. For example, to select the V_{DD} channel for monitoring write to the Control Configuration 2 register and set C4 to 1 (if not done so already), then write all 0's to bits C0 to C2. All subsequent conversions will be done on the V_{DD} channel only. To change the channel selection to the Internal temperature channel, write to the Control Configuration 2 register and set C0 = 1. When measuring in single channel mode, conversions on the channel selected occur directly after each other. Any communication to the ADT7516/17/18 stops the conversions but they are restarted once the read or write operation is completed.

MEASUREMENT METHOD**INTERNAL TEMPERATURE MEASUREMENT**

The ADT7516/7517/7518 contains an on-chip bandgap temperature sensor, whose output is digitized by the on-chip ADC. The temperature data is stored in the Internal Temperature Value Register. As both positive and negative temperatures can be measured, the temperature data is stored in two's complement format, as shown in Table 5. The thermal characteristics of the measurement sensor could change and therefore an offset is added to the measured value to enable the transfer function to match the

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thermal characteristics. This offset is added before the temperature data is stored. The offset value used is stored in the Internal Temperature Offset Register.

EXTERNAL TEMPERATURE MEASUREMENT

The ADT7516/7517/7518 can measure the temperature of one external diode sensor or diode-connected transistor.

The forward voltage of a diode or diode-connected transistor, operated at a constant current, exhibits a negative temperature coefficient of about $-2\text{mV}/^\circ\text{C}$. Unfortunately, the absolute value of V_{be} , varies from device to device, and individual calibration is required to null this out, so the technique is unsuitable for mass-production.

The time taken to measure the external temperature can be reduced by setting C0 of Control Config. 3 register (1Ah). This increases the ADC clock speed from 1.4KHz to 22KHz but the analog filters on the D+ and D- input pins are switched off to accommodate the higher clock speeds. Running at the slower ADC speed, the time taken to measure the external temperature is 16.8ms while on the fast ADC this time is reduced to 712 μs .

The technique used in the ADT7516/7517/7518 is to measure the change in V_{be} when the device is operated at two different currents.

This is given by:

$$\Delta V_{be} = KT/q \times \ln(N)$$

where:

K is Boltzmann's constant

q is charge on the carrier

T is absolute temperature in Kelvins

N is ratio of the two currents

Figure 10 shows the input signal conditioning used to measure the output of an external temperature sensor. This figure shows the external sensor as a substrate transistor, provided for temperature monitoring on some microprocessors, but it could equally well be a discrete transistor.

If a discrete transistor is used, the collector will not be grounded, and should be linked to the base. If a PNP transistor is used the base is connected to the D- input and the emitter to the D+ input. If an NPN transistor is used, the emitter is connected to the D- input and the base to the D+ input.

We recommend that a 2N3906 be used as the external transistor.

To prevent ground noise interfering with the measurement, the more negative terminal of the sensor is not referenced to ground, but is biased above ground by an internal diode at the D- input. As the sensor is operating in a noisy environment, C1 is provided as a noise filter. See the section on layout considerations for more information on C1.

To measure ΔV_{be} , the sensor is switched between operating currents of I and N x I. The resulting waveform is passed through a lowpass filter to remove noise, thence to a chopper-stabilized amplifier that performs the functions of amplification and rectification of the waveform to produce

a DC voltage proportional to ΔV_{be} . This voltage is measured by the ADC to give a temperature output in 10-bit two's complement format. To further reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles.

LAYOUT CONSIDERATIONS

Digital boards can be electrically noisy environments, and care must be taken to protect the analog inputs from noise, particularly when measuring the very small voltages from a remote diode sensor. The following precautions should be taken:

1. Place the ADT7516/17/18 as close as possible to the remote sensing diode. Provided that the worst noise sources such as clock generators, data/address buses and CRTs are avoided, this distance can be 4 to 8 inches.
2. Route the D+ and D- tracks close together, in parallel, with grounded guard tracks on each side. Provide a ground plane under the tracks if possible.
3. Use wide tracks to minimize inductance and reduce noise pickup. 10 mil track minimum width and spacing is recommended.



Figure 19. Arrangement of Signal Tracks

4. Try to minimize the number of copper/solder joints, which can cause thermocouple effects. Where copper/solder joints are used, make sure that they are in both the D+ and D- path and at the same temperature. Thermocouple effects should not be a major problem as 1°C corresponds to about $240\mu\text{V}$, and thermocouple voltages are about $3\mu\text{V}/^\circ\text{C}$ of temperature difference. Unless there are two thermocouples with a big temperature differential between them, thermocouple voltages should be much less than 200mV.
5. Place 0.1 μF bypass and 2200pF input filter capacitors close to the ADT7516/17/18.
6. If the distance to the remote sensor is more than 8 inches, the use of twisted pair cable is recommended. This will work up to about 6 to 12 feet.
7. For really long distances (up to 100 feet) use shielded twisted pair such as Belden #8451 microphone cable. Connect the twisted pair to D+ and D- and the shield to GND close to the ADT7516/17/18. Leave the remote end of the shield unconnected to avoid ground loops.

Because the measurement technique uses switched current sources, excessive cable and/or filter capacitance can affect

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the measurement. When using long cables, the filter capacitor may be reduced or removed.

Cable resistance can also introduce errors. 1Ω series resistance introduces about 0.5°C error.

TEMPERATURE VALUE FORMAT

One LSB of the ADC corresponds to 0.25°C. The ADC can theoretically measure a temperature span of 255 °C. The internal temperature sensor is guaranteed to a low value limit of -40 °C. It is possible to measure the full temperature span using the external temperature sensor. The temperature data format is shown in Tables 5.

The result of the internal or external temperature measurements is stored in the temperature value registers, and is compared with limits programmed into the Internal or External High and Low Registers.

TABLE 5. Temperature Data Format (Internal and External Temperature)

Temperature	Digital Output
-40 °C	11 0110 0000
-25 °C	11 1001 1100
-10 °C	11 1101 1000
-0.25 °C	11 1111 1111
0 °C	00 0000 0000
+0.25 °C	00 0000 0001
+10 °C	00 0010 1000
+25 °C	00 0110 0100
+50 °C	00 1100 1000
+75 °C	01 0010 1100
+100 °C	01 1001 0000
+105 °C	01 1010 0100
+125 °C	01 1111 0100

Temperature Conversion Formula:

1. Positive Temperature = ADC Code/4
2. Negative Temperature = (ADC Code* - 512)/4

*DB9 is removed from the ADC Code

INTERRUPTS

The measured results from the internal temperature sensor, external temperature sensor, V_{DD} pin and the AIN inputs are compared with the T_{HIGH}/V_{HIGH} (greater than comparison) and T_{LOW}/V_{LOW} (greater than or equal to comparison) limits. An interrupt occurs if the measurement exceeds or equals the limit registers. These limits are stored in on-chip registers. Please note that the limit registers are 8 bits long while the conversion results are 10

bits long. If the limits are not masked out then any out-of-limit comparisons generate flags that are stored in Interrupt Status 1 Register (address = 00h) and Interrupt Status 2 Register (address = 01h). One or more out-of-limit results will cause the $INT/\overline{INT}$ output to pull either high or low depending on the output polarity setting. It is good design practice to mask out interrupts for channels that are of no concern to the application.

Figure 18 shows the interrupt structure for the ADT7516/17/18. It gives a block diagram representation of how the various measurement channels affect the $INT/\overline{INT}$ pin.

ADT7516/7517/7518 REGISTERS

The ADT7516/17/18 contains registers that are used to store the results of external and internal temperature measurements, V_{DD} value measurements, analog input measurements, high and low temperature limits, supply voltage and analog input limits, set output DAC voltage levels, configure multipurpose pins and generally control the device. A description of these registers follows.

The register map is divided into registers of 8-bits long. Each register has it's own individual address but some consist of data that is linked with other registers. These registers hold the 10-bit conversion results of measurements taken on the Temperature, V_{DD} and AIN channels. For example, the 8 MSBs of the V_{DD} measurement are stored in register address 06h while the 2 LSBs are stored in register address 03h. The link involved between these types of registers is that when the LSB register is read first then the MSB registers associated with that LSB register are locked to prevent any updates. To unlock these MSB registers the user has only to read any one of them, which will have the affect of unlocking all previously locked MSB registers. So for the example given above if register 03h was read first then MSB registers 06h and 07h would be locked to prevent any updates to them. If register 06h was read then this register and register 07h would be subsequently unlocked.

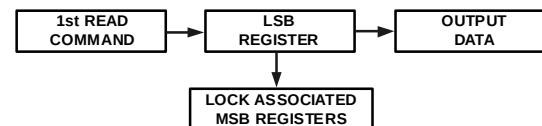


Figure 20. Phase 1 of 10-Bit Read

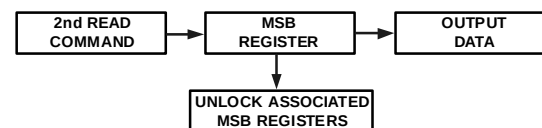


Figure 21. Phase 2 of 10-Bit Read

If an MSB register is read first, it's corresponding LSB register is not locked thus leaving the user with the option of just reading back 8 bits (MSB) of a 10-bit conversion result. Reading an MSB register first does not lock up other MSB registers and likewise reading an LSB register first does not lock up other LSB registers.

Table 6. List of ADT7516/7517/7518 Registers

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RD/WR Address	Name	Power-on Default
00h	Interrupt Status 1	00h
01h	Interrupt Status 2	00h
02h	RESERVED	
03h	Internal Temp & V _{DD} LSBs	00h
04h	External Temp & AIN 1-4 LSBs	00h
05h	RESERVED	00h
06h	V _{DD} MSBs	00h
07h	Internal Temperature MSBs	00h
08h	External Temp MSBs/ AIN 1 MSBs	00h
09h	AIN 2 MSBs	00h
0Ah	AIN 3 MSBs	00h
0Bh	AIN 4 MSBs	00h
0Ch-0Fh	RESERVED	00h
10h	DAC A LSBs (ADT7516/17 only)	00h
11h	DAC A MSBs	00h
12h	DAC B LSBs (ADT7516/17 only)	00h
13h	DAC B MSBs	00h
14h	DAC C LSBs (ADT7516/17 only)	00h
15h	DAC C MSBs	00h
16h	DAC D LSBs (ADT7516/17 only)	00h
17h	DAC D MSBs	00h
18h	Control CONFIG 1	00h
19h	Control CONFIG 2	00h
1Ah	Control CONFIG 3	00h
1Bh	DAC CONFIG	00h
1Ch	LDAC CONFIG	00h
1Dh	Interrupt Mask 1	00h
1Eh	Interrupt Mask 2	00h
1Fh	Internal Temp Offset	00h
20h	External Temp Offset	00h
21h	Internal Analog Temp Offset	D8h
22h	External Analog Temp Offset	D8h
23h	V _{DD} V _{HIGH} Limit	C7h
24h	V _{DD} V _{LOW} Limit	62h
25h	Internal T _{HIGH} Limit	64h
26h	Internal T _{LOW} Limit	C9h

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27h	External T _{HIGH} / AIN1 V _{HIGH} Limits	FFh
28h	External T _{LOW} / AIN1 V _{LOW} Limits	00h
29h-2Ah	RESERVED	
2Bh	AIN 2 V _{HIGH} Limit	FFh
2Ch	AIN 2 V _{LOW} Limit	00h
2Dh	AIN 3 V _{HIGH} Limit	FFh
2Eh	AIN 3 V _{LOW} Limit	00h
2Fh	AIN 4 V _{HIGH} Limit	FFh
30h	AIN 4 V _{LOW} Limit	00h
31h-4Ch	RESERVED	
4Dh	Device ID	03h/0Bh/07h
4Eh	Manufacturer's ID	41h
4Fh	Silicon Revision	00h
50h-7Eh	RESERVED	00h
7F	SPI Lock Status	00h
80-FFh	RESERVED	00h

Interrupt Status 1 Register (Read only) [Add. = 00h]

This 8-bit read only register reflects the status of some of the interrupts that can cause the INT/ $\overline{\text{INT}}$ pin to go active. This register is reset by a read operation provided that any out of limit event has been corrected. It is also reset by a software reset.

Table 7. Interrupt Status 1 Register

D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

Bit	Function
D0	1 when Internal Temp Value exceeds T _{HIGH} limit. Any internal temperature reading greater than the limit set will cause an out of limit event.
D1	1 when Internal Temp Value exceeds T _{LOW} limit. Any internal temperature reading less than or equal to the limit set will cause an out of limit event.
D2	This status bit is linked to the configuration of pins 7 and 8. If configured for External Temperature Sensor

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then this bit is 1 when External Temp Value exceeds T_{HIGH} limit. The default value for this limit register is -1°C so any external temperature reading greater than the limit set will cause an out of limit event.

If configured for AIN1 and AIN2 then this bit is 1 when AIN1 Input Voltage exceeds V_{HIGH} or V_{LOW} limits.

D3	1 when External Temp Value exceeds T_{LOW} limit. The default value for this limit register is 0°C so any external temperature reading less than or equal to the limit set will cause an out of limit event.
D4	1 indicates a fault (open or short) for the external temperature sensor.
D5	1 when AIN2 voltage is greater than corresponding V_{HIGH} limit. 1 when AIN2 voltage is less than or equal to corresponding V_{LOW} limit.
D6	1 when AIN3 voltage is greater than corresponding V_{HIGH} limit. 1 when AIN3 voltage is less than or equal to corresponding V_{LOW} limit.
D7	1 when AIN4 voltage is greater than corresponding V_{HIGH} limit. 1 when AIN4 voltage is less than or equal to corresponding V_{LOW} limit.

Interrupt Status 2 Register (Read only) [Add. = 01h]

This 8-bit read only register reflects the status of the V_{DD} interrupt that can cause the $\text{INT}/\overline{\text{INT}}$ pin to go active. This register is reset by a read operation provided that any out of limit event has been corrected. It is also reset by a software reset.

Table 8. Interrupt Status 2 Register

D7	D6	D5	D4	D3	D2	D1	D0
N/A	N/A	N/A	0*	N/A	N/A	N/A	N/A

*Default settings at Power-up.

Bit	Function
D4	1 when V_{DD} value is greater than corresponding V_{HIGH} limit. 1 when V_{DD} is less than or equal to corresponding V_{LOW} limit.

INTERNAL TEMPERATURE VALUE/ V_{DD} VALUE REGISTER LSBs (Read only) [Add. = 03h]

This Internal Temperature Value and V_{DD} Value Register is a 8-bit read-only register. It stores the two LSBs of the 10-bit temperature reading from the internal temperature sensor and also the two LSBs of the 10-bit supply voltage reading.

Table 9. Internal Temp/ V_{DD} LSBs

D7	D6	D5	D4	D3	D2	D1	D0
N/A	N/A	N/A	N/A	V1	LSB	T1	LSB
N/A	N/A	N/A	N/A	0*	0*	0*	0*

*Default settings at Power-up.

Bit	Function
D0	LSB of Internal Temperature Value
D1	B1 of Internal Temperature Value
D2	LSB of V_{DD} Value
D3	B1 of V_{DD} Value

EXTERNAL TEMPERATURE VALUE and ANALOG INPUTS 1-4 REGISTER LSBs (Read only) [Add. = 04h]

This is a 8-bit read-only register. Bits D2 - D7 store the two LSBs of the analog inputs AIN2 - AIN4. Bits D0 and D1 are used to store the two LSBs of either the External Temperature Value or AIN1 input value. The type of input for D0 and D1 is selected by Bits C1:C2 of Control Configuration 1.

Table 10. External Temperature & AIN 1-4 LSBs

D7	D6	D5	D4	D3	D2	D1	D0
A4	A4 _{LSB}	A3	A3 _{LSB}	A2	A2 _{LSB}	T/A	T/A _{LSB}
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

Bit	Function
D0	LSB of External Temperature Value or AIN 1 Value
D1	Bit 1 of External Temperature Value or AIN 1 Value
D2	LSB of AIN 2 Value
D3	Bit 1 of AIN 2 Value
D4	LSB of AIN 3 Value
D5	Bit 1 of AIN 3 Value
D6	LSB of AIN 4 Value
D7	Bit 1 of AIN 4 Value

 V_{DD} VALUE REGISTER MSBs (Read only) [Add. = 06h]

This 8-bit read only register stores the supply voltage value. The 8 MSBs of the 10-bit value are stored in this register.

Table 11. V_{DD} Value MSBs

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

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V9	V8	V7	V6	V5	V4	V3	V2
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

INTERNAL TEMPERATURE VALUE REGISTER MSBS (Read only) [Add. = 07h]

This 8-bit read only register stores the Internal Temperature value from the internal temperature sensor in twos complement format. The 8 MSBs of the 10-bit value are stored in this register.

Table 12. Internal Temperature Value MSBs

D7	D6	D5	D4	D3	D2	D1	D0
T9	T8	T7	T6	T5	T4	T3	T2
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

EXTERNAL TEMPERATURE VALUE OR ANALOG INPUT AIN 1 REGISTER MSBS (Read only) [Add. = 08h]

This 8-bit read only register stores, if selected, the External Temperature value or the Analog Input AIN 1 value. Selection is done in Control Configuration 1 register. The external temperature value is stored in twos complement format. The 8 MSBs of the 10-bit value are stored in this register.

Table 13. External Temperature Value/Analog Inputs MSBs

D7	D6	D5	D4	D3	D2	D1	D0
T/A9	T/A8	T/A7	T/A6	T/A5	T/A4	T/A3	T/A2
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

AIN 2 REGISTER MSBS (Read) [Add. = 09h]

This 8-bit read register contains the 8 MSBs of the AIN 2 analog input voltage word. The value in this register is combined with bits D2:3 of the External Temperature Value and Analog Inputs 1-4 Register LSBs, address 04h, to give the full 10-bit conversion result of the analog value on the AIN 2 pin.

Table 14. AIN 2 MSBs

D7	D6	D5	D4	D3	D2	D1	D0
MSB	A8	A7	A6	A5	A4	A3	A2
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

AIN 3 REGISTER MSBS (Read) [Add. = 0Ah]

This 8-bit read register contains the 8 MSBs of the AIN 3 analog input voltage word. The value in this register is combined with bits D4:5 of the External Temperature Value and Analog Inputs 1-4 Register LSBs, address 04h,

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to give the full 10-bit conversion result of the analog value on the AIN 3 pin.

Table 15. AIN 3 MSBs

D7	D6	D5	D4	D3	D2	D1	D0
MSB	A8	A7	A6	A5	A4	A3	A2
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

AIN 4 REGISTER MSBS (Read) [Add. = 0Bh]

This 8-bit read register contains the 8 MSBs of the AIN 4 analog input voltage word. The value in this register is combined with bits D6:7 of the External Temperature Value and Analog Inputs 1-4 Register LSBs, address 04h, to give the full 10-bit conversion result of the analog value on the AIN 4 pin.

Table 16. AIN 4 MSBs

D7	D6	D5	D4	D3	D2	D1	D0
MSB	A8	A7	A6	A5	A4	A3	A2
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

DAC A REGISTER LSBs (Read/Write) [Add. = 10h]

This 8-bit read/write register contains the 4/2 LSBs of the ADT7516/7517 DAC A word respectively. The value in this register is combined with the value in the DAC A Register MSBs and converted to an analog voltage on the V_{OUTA} pin. On power-up the voltage output on the V_{OUTA} pin is 0 V.

Table 17. DAC A (ADT7516) LSBs

D7	D6	D5	D4	D3	D2	D1	D0
B3	B2	B1	LSB	N/A	N/A	N/A	N/A
0*	0*	0*	0*	N/A	N/A	N/A	N/A

*Default settings at Power-up.

Table 18. DAC A (ADT7517) LSBs

D7	D6	D5	D4	D3	D2	D1	D0
B1	LSB	N/A	N/A	N/A	N/A	N/A	N/A
0*	0*	N/A	N/A	N/A	N/A	N/A	N/A

*Default settings at Power-up.

DAC A REGISTER MSBS (Read/Write) [Add. = 11h]

This 8-bit read/write register contains the 8 MSBs of the DAC A word. The value in this register is combined with the value in the DAC A Register LSBs and converted to an analog voltage on the V_{OUTA} pin. On power-up the voltage output on the V_{OUTA} pin is 0 V.

Table 19. DAC A MSBs

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

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MSB	B8	B7	B6	B5	B4	B3	B2
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

DAC B REGISTER LSBs (Read/Write) [Add. = 12h]

This 8-bit read/write register contains the 4/2 LSBs of the ADT7516/7517 DAC B word respectively. The value in this register is combined with the value in the DAC B Register MSBs and converted to an analog voltage on the V_{OUTB} pin. On power-up the voltage output on the V_{OUTB} pin is 0 V.

Table 20. DAC B (ADT7516) LSBs

D7	D6	D5	D4	D3	D2	D1	D0
B3	B2	B1	LSB	N/A	N/A	N/A	N/A
0*	0*	0*	0*	N/A	N/A	N/A	N/A

*Default settings at Power-up.

Table 21. DAC B (ADT7517) LSBs

D7	D6	D5	D4	D3	D2	D1	D0
B1	LSB	N/A	N/A	N/A	N/A	N/A	N/A
0*	0*	N/A	N/A	N/A	N/A	N/A	N/A

*Default settings at Power-up.

DAC B REGISTER MSBs (Read/Write) [Add. = 13h]

This 8-bit read/write register contains the 8 MSBs of the DAC B word. The value in this register is combined with the value in the DAC B Register LSBs and converted to an analog voltage on the V_{OUTB} pin. On power-up the voltage output on the V_{OUTB} pin is 0 V.

Table 22. DAC B MSBs

D7	D6	D5	D4	D3	D2	D1	D0
MSB	B8	B7	B6	B5	B4	B3	B2
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

DAC C REGISTER LSBs (Read/Write) [Add. = 14h]

This 8-bit read/write register contains the 4/2 LSBs of the ADT7516/7517 DAC C word respectively. The value in this register is combined with the value in the DAC C Register MSBs and converted to an analog voltage on the V_{OUTC} pin. On power-up the voltage output on the V_{OUTC} pin is 0 V.

Table 23. DAC C (ADT7516) LSBs

D7	D6	D5	D4	D3	D2	D1	D0
B3	B2	B1	LSB	N/A	N/A	N/A	N/A
0*	0*	0*	0*	N/A	N/A	N/A	N/A

*Default settings at Power-up.

Table 24. DAC C (ADT7517) LSBs

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D7	D6	D5	D4	D3	D2	D1	D0
B1	LSB	N/A	N/A	N/A	N/A	N/A	N/A
0*	0*	N/A	N/A	N/A	N/A	N/A	N/A

*Default settings at Power-up.

DAC C REGISTER MSBs (Read/Write) [Add. = 15h]

This 8-bit read/write register contains the 8 MSBs of the DAC C word. The value in this register is combined with the value in the DAC C Register LSBs and converted to an analog voltage on the V_{OUTC} pin. On power-up the voltage output on the V_{OUTC} pin is 0 V.

Table 25. DAC C MSBs

D7	D6	D5	D4	D3	D2	D1	D0
MSB	B8	B7	B6	B5	B4	B3	B2
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

DAC D REGISTER LSBs (Read/Write) [Add. = 16h]

This 8-bit read/write register contains the 4/2 LSBs of the ADT7516/7517 DAC D word respectively. The value in this register is combined with the value in the DAC D Register MSBs and converted to an analog voltage on the V_{OUTD} pin. On power-up the voltage output on the V_{OUTD} pin is 0 V.

Table 26. DAC D (ADT7516) LSBs

D7	D6	D5	D4	D3	D2	D1	D0
B3	B2	B1	LSB	N/A	N/A	N/A	N/A
0*	0*	0*	0*	N/A	N/A	N/A	N/A

*Default settings at Power-up.

Table 27. DAC D (ADT7517) LSBs

D7	D6	D5	D4	D3	D2	D1	D0
B1	LSB	N/A	N/A	N/A	N/A	N/A	N/A
0*	0*	N/A	N/A	N/A	N/A	N/A	N/A

*Default settings at Power-up.

DAC D REGISTER MSBs (Read/Write) [Add. = 17h]

This 8-bit read/write register contains the 8 MSBs of the DAC D word. The value in this register is combined with the value in the DAC D Register LSBs and converted to an analog voltage on the V_{OUTD} pin. On power-up the voltage output on the V_{OUTD} pin is 0 V.

Table 28. DAC D MSBs

D7	D6	D5	D4	D3	D2	D1	D0
MSB	B8	B7	B6	B5	B4	B3	B2
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

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CONTROL CONFIGURATION 1 REGISTER (Read/Write) [Add. = 18h]

This configuration register is an 8-bit read/write register that is used to setup some of the operating modes of the ADT7516/17/18.

Table 29. Control Configuration 1

D7	D6	D5	D4	D3	D2	D1	D0
PD	C6	C5	C4	C3	C2	C1	C0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

Bit	Function
C0	This bit enables/disables conversions in Round Robin and Single Channel mode. ADT7516/17/18 powers up in Round Robin mode but monitoring is not initiated until this bit is set. Default = 0. 0 = Stop monitoring. 1 = Start monitoring.
C2:C1	Selects between the two different analog inputs on pins 7 and 8. ADT7516/17/18 powers up with AIN1 and AIN2 selected. 00 AIN1 and AIN2 selected. 01 Undefined. 10 External TDM selected. 11 Undefined.
C3	Selects between digital (LDAC) and analog inputs (AIN3) on pin 9. When AIN3 is selected, Bit C3 of Control Configuration 3 register is masked out and has no affect until LDAC is selected as the input on pin 9. 0 LDAC selected. 1 AIN3 selected.
C4	RESERVED. Write 0 only.
C5	0 Enable $\text{INT}/\overline{\text{INT}}$ Output 1 Disable $\text{INT}/\overline{\text{INT}}$ Output
C6	Configures $\text{INT}/\overline{\text{INT}}$ output polarity. 0 = Active low 1 = Active High
PD	Power-down Bit. Setting this bit to 1 puts the ADT7516/17/18 into standby mode. In this mode both ADC and DACs are fully powered down, but serial interface is still operational. To power up the part again just write 0 to this bit.

CONTROL CONFIGURATION 2 REGISTER (Read/Write) [Add. = 19h]

This configuration register is an 8-bit read/write register that is used to setup some of the operating modes of the ADT7516/17/18.

Table 30. Control Configuration 2

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

C7	C6	C5	C4	C3	C2	C1	C0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

Bit	Function
C2:0	In single channel mode these bits select between V_{DD} , the internal temperature sensor, external temperature sensor/AIN1, AIN2, AIN3 and AIN4 for conversion. Default is V_{DD} . 000 = V_{DD} 001 = Internal Temperature Sensor. 010 = External Temperature Sensor/AIN1 (Bits C1:C2 of Control Configuration 1 affect this selection) 011 = AIN2 100 = AIN3 101 = AIN4 110 - 111 = RESERVED
C3	RESERVED
C4	Selects between single channel and Round Robin conversion cycle. Default is Round Robin. 0 = Round Robin. 1 = Single Channel.
C5	Default condition is to average every measurement on all channels 16 times. This bit disables this averaging. Channels affected are temperature, analog inputs and V_{DD} . 0 = Enable averaging. 1 = Disable averaging.
C6	SMBus timeout on the serial clock puts a 25ms limit on the pulse width of the clock. Ensures that a fault on the master SCL does not lock up the SDA line. 0 = Disable SMBus Timeout. 1 = Enable SMBus Timeout.
C7	Software Reset. Setting this bit to a 1 causes a software reset. All registers and DAC outputs will reset to their default settings.

CONTROL CONFIGURATION 3 REGISTER (Read/Write) [Add. = 1Ah]

This configuration register is an 8-bit read/write register that is used to setup some of the operating modes of the ADT7516/17/18.

Table 31. Control Configuration 3

D7	D6	D5	D4	D3	D2	D1	D0
C7	C6	C5	C4	C3	C2	C1	C0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

Bit	Function
C0	Selects between fast and normal ADC conversion speeds.

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0 = ADC clock at 1.4 KHz.
 1 = ADC clock at 22.5 KHz. Analog filters are disabled.

C1	On the ADT7516 and ADT7517, this bit selects between 8 bits and 10 bits DAC output resolution on the Thermal Voltage Output feature. Default = 8 bits. This bit has no affect on the ADT7518 output as this part has only an 8-bit DAC. In the ADT7518 case, write 0 to this bit. 0 = 8 bits resolution. 1 = 10 bits resolution.
C2	RESERVED. Only write 0.
C3	0 = $\overline{\text{LDAC}}$ pin controls updating of DAC outputs. 1 = DAC Configuration register and LDAC Configuration register control updating of DAC outputs.
C4	Selects the ADC reference to be either Internal V_{REF} or V_{DD} for analog inputs. 0 = Int V_{REF} 1 = V_{DD}
C5	Setting this bit selects DAC A voltage output to be proportional to the internal temperature measurement.
C6	Setting this bit selects DAC B voltage output to be proportional to the external temperature measurement.
C7	RESERVED. Write 0 only.

DAC CONFIGURATION REGISTER (Read/Write)**[Add. = 1Bh]**

This configuration register is an 8-bit read/write register that is used to control the output ranges of all four DACs and also to control the loading of the DAC registers if the $\overline{\text{LDAC}}$ pin is disabled (bit C3 = 1, Control Configuration 3 register).

Table 32. DAC Configuration

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

Bit	Function
D0	Selects the output range of DAC A. 0 = 0 V to V_{REF} . 1 = 0 V to $2V_{\text{REF}}$.
D1	Selects the output range of DAC B. 0 = 0 V to V_{REF} . 1 = 0 V to $2V_{\text{REF}}$.
D2	Selects the output range of DAC C. 0 = 0 V to V_{REF} . 1 = 0 V to $2V_{\text{REF}}$.

D3 Selects the output range of DAC D.
 0 = 0 V to V_{REF} .
 1 = 0 V to $2V_{\text{REF}}$.

D5:D4	00	MSB write to any DAC register generates LDAC command which updates that DAC only.
	01	MSB write to DAC B or DAC D register generates LDAC command which updates DACs A, B or DACs C, D respectively.
	10	MSB write to DAC D register generates LDAC command which updates all 4 DACs.
	11	LDAC command generated from LDAC register.

D6:D7 RESERVED. Write 0's only.

LDAC CONFIGURATION REGISTER (Write only)**[Add. = 1Ch]**

This configuration register is an 8-bit write register that is used to control the updating of the quad DAC outputs if the $\overline{\text{LDAC}}$ pin is disabled and Bits D4 and D5 of DAC Configuration register are both set to 1. Also selects either the internal or external V_{REF} for all four DACs. Bits D0-D3 in this register are self clearing i.e. reading back from this register will always give 0's for these bits.

Table 33. LDAC Configuration

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

Bit	Function
D0	Writing a 1 to this bit will generate the LDAC command to update DAC A output only.
D1	Writing a 1 to this bit will generate the LDAC command to update DAC B output only.
D2	Writing a 1 to this bit will generate the LDAC command to update DAC C output only.
D3	Writing a 1 to this bit will generate the LDAC command to update DAC D output only.
D4	Selects either internal V_{REF} or external V_{REF} for DACs A and B. 0 = External V_{REF} 1 = Internal V_{REF}
D5	Selects either internal V_{REF} or external V_{REF} for DACs C and D. 0 = External V_{REF} 1 = Internal V_{REF}
D6:D7	RESERVED. Only write 0's.

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INTERRUPT MASK 1 REGISTER (Read/Write) [Add. = 1Dh]

This mask register is an 8-bit read/write register that can be used to mask out any interrupts that can cause the INT/ $\overline{\text{INT}}$ pin to go active.

Table 34. Interrupt Mask 1

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

Bit	Function
D0	0 = Enable internal T_{HIGH} interrupt. 1 = Disable internal T_{HIGH} interrupt.
D1	0 = Enable internal T_{LOW} interrupt. 1 = Disable internal T_{LOW} interrupt.
D2	0 = Enable external T_{HIGH} interrupt or AIN1 interrupt. 1 = Disable external T_{HIGH} interrupt or AIN1 interrupt.
D3	0 = Enable external T_{LOW} interrupt. 1 = Disable external T_{LOW} interrupt.
D4	0 = Enable external temperature fault interrupt. 1 = Disable external temperature fault interrupt.
D5	0 = Enable AIN2 interrupt. 1 = Disable AIN2 interrupt.
D6	0 = Enable AIN3 interrupt. 1 = Disable AIN3 interrupt.
D7	0 = Enable AIN4 interrupt. 1 = Disable AIN4 interrupt.

INTERRUPT MASK 2 REGISTER (Read/Write) [Add. = 1Eh]

This mask register is an 8-bit read/write register that can be used to mask out any interrupts that can cause the INT/ $\overline{\text{INT}}$ pin to go active.

Table 35. Interrupt Mask 2

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

Bit	Function
D0:D3	RESERVED. Only write 0's.
D4	0 = Enable V_{DD} interrupts. 1 = Disable V_{DD} interrupts.
D5:D7	RESERVED. Only write 0's.

INTERNAL TEMPERATURE OFFSET REGISTER (Read/Write) [Add. = 1Fh]

This register contains the Offset Value for the Internal Temperature Channel. A 2's complement number can be written to this register which is then 'added' to the measured result before it is stored or compared to limits. In this way a sort of one-point calibration can be done whereby the whole transfer function of the channel can be moved up or down. From a software point of view this may be a very simple method to vary the characteristics of the measurement channel if the thermal characteristics change. As it is an 8-bit register the temperature resolution is 1°C.

Table 36. Internal Temperature Offset

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

EXTERNAL TEMPERATURE OFFSET REGISTER (Read/Write) [Add. = 20h]

This register contains the Offset Value for the Internal Temperature Channel. A 2's complement number can be written to this register which is then 'added' to the measured result before it is stored or compared to limits. In this way a sort of one-point calibration can be done whereby the whole transfer function of the channel can be moved up or down. From a software point of view this may be a very simple method to vary the characteristics of the measurement channel if the thermal characteristics change. As it is an 8-bit register the temperature resolution is 1°C.

Table 37. External Temperature Offset

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

INTERNAL ANALOG TEMPERATURE OFFSET REGISTER (Read/Write) [Add. = 21h]

This register contains the Offset Value for the Internal Thermal Voltage output. A 2's complement number can be written to this register which is then 'added' to the measured result before it is converted by DAC A. Varying the value in this register has the affect of varying the temperature span. For example, the output voltage can represent a temperature span of -128°C to +127°C or even 0°C to +127°C. In essence this register changes the position of 0V on the temperature scale. Anything other than -128°C to +127°C will produce an upper deadband on the DAC A output. As it is an 8-bit register the temperature resolution is 1°C. Default value is -40°C.

Table 38. Internal Analog Temperature Offset

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

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D7	D6	D5	D4	D3	D2	D1	D0
1*	1*	0*	1*	1*	0*	0*	0*

*Default settings at Power-up.

EXTERNAL ANALOG TEMPERATURE OFFSET REGISTER (Read/Write) [Add. = 22h]

This register contains the Offset Value for the External Thermal Voltage output. A 2's complement number can be written to this register which is then 'added' to the measured result before it is converted by DAC B. Varying the value in this register has the affect of varying the temperature span. For example, the output voltage can represent a temperature span of -128°C to +127°C or even 0°C to +127°C. In essence this register changes the position of 0V on the temperature scale. Anything other than -128°C to +127°C will produce an upper deadband on the DAC B output. As it is an 8-bit register the temperature resolution is 1°C. Default value is -40°C.

Table 39. External Analog Temperature Offset

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1*	1*	0*	1*	1*	0*	0*	0*

*Default settings at Power-up.

V_{DD} V_{HIGH} LIMIT REGISTER (Read/Write) [Add. = 23h]

This limit register is an 8-bit read/write register which stores the V_{DD} upper limit that will cause an interrupt and activate the INT/ $\overline{\text{INT}}$ output (if enabled). For this to happen the measured V_{DD} value has to be greater than the value in this register. Default value is 5.46 V.

Table 40. V_{DD} V_{HIGH} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1*	1*	0*	0*	0*	1*	1*	1*

*Default settings at Power-up.

V_{DD} V_{LOW} LIMIT REGISTER (Read/Write) [Add. = 24h]

This limit register is an 8-bit read/write register which stores the V_{DD} lower limit that will cause an interrupt and activate the INT/ $\overline{\text{INT}}$ output (if enabled). For this to happen the measured V_{DD} value has to be less than or equal to the value in this register. Default value is 2.7 V.

Table 41. V_{DD} V_{HIGH} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	1*	1*	0*	0*	0*	1*	0*

*Default settings at Power-up.

INTERNAL T_{HIGH} LIMIT REGISTER (Read/Write) [Add. = 25h]

This limit register is an 8-bit read/write register which stores the 2's complement of the internal temperature

upper limit that will cause an interrupt and activate the INT/ $\overline{\text{INT}}$ output (if enabled). For this to happen the measured Internal Temperature Value has to be greater than the value in this register. As it is an 8-bit register the temperature resolution is 1°C. Default value is +100°C.

Table 42. Internal T_{HIGH} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	1*	1*	0*	0*	1*	0*	0*

*Default settings at Power-up.

INTERNAL T_{LOW} LIMIT REGISTER (Read/Write) [Add. = 26h]

This limit register is an 8-bit read/write register which stores the 2's complement of the internal temperature lower limit that will cause an interrupt and activate the INT/ $\overline{\text{INT}}$ output (if enabled). For this to happen the measured Internal Temperature Value has to be more negative than or equal to the value in this register. As it is an 8-bit register the temperature resolution is 1°C. Default value is -55°C.

Table 43. Internal T_{LOW} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1*	1*	0*	0*	1*	0*	0*	1*

*Default settings at Power-up.

EXTERNAL T_{HIGH} / AIN1 V_{HIGH} LIMIT REGISTER (Read/Write) [Add. = 27h]

If pins 7 and 8 are configured for the external temperature sensor then this limit register is an 8-bit read/write register which stores the 2's complement of the external temperature upper limit that will cause an interrupt and activate the INT/ $\overline{\text{INT}}$ output (if enabled). For this to happen the measured External Temperature Value has to be greater than the value in this register. As it is an 8-bit register the temperature resolution is 1°C. Default value is -1°C.

If pins 7 and 8 are configured for AIN1 and AIN2 inputs then this limit register is an 8-bit read/write register which stores the AIN1 input upper limit that will cause an interrupt and activate the INT/ $\overline{\text{INT}}$ output (if enabled). For this to happen the measured AIN1 value has to be greater than the value in this register. As it is an 8-bit register the resolution is four times less than the resolution of the 10-Bit ADC. As the power-up default settings for pins 7 and 8 is AIN1 and AIN2 inputs then the default value for this limit register is fullscale voltage.

Table 44. AIN1 V_{HIGH} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1*	1*	1*	1*	1*	1*	1*	1*

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*Default settings at Power-up.

EXTERNAL T_{LOW} / AIN1 V_{LOW} LIMIT REGISTER (Read/Write) [Add. = 28h]

If pins 7 and 8 are configured for the external temperature sensor then this limit register is an 8-bit read/write register which stores the 2's complement of the external temperature lower limit that will cause an interrupt and activate the INT/ $\overline{\text{INT}}$ output (if enabled). For this to happen the measured External Temperature Value has to be more negative than or equal to the value in this register. As it is an 8-bit register the temperature resolution is 1°C. Default value = 0°C.

If pins 7 and 8 are configured for AIN1 and AIN2 inputs then this limit register is an 8-bit read/write register which stores the AIN1 input lower limit that will cause an interrupt and activate the INT/ $\overline{\text{INT}}$ output (if enabled). For this to happen the measured AIN1 value has to be less than or equal to the value in this register. As it is an 8-bit register the resolution is four times less than the resolution of the 10-Bit ADC. As the power-up default settings for pins 7 and 8 is AIN1 and AIN2 inputs then the default value for this limit register is 0 V.

Table 45. AIN1 V_{LOW} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

AIN2 V_{HIGH} LIMIT REGISTER (Read/Write) [Add. = 2Bh]

This limit register is an 8-bit read/write register which stores the AIN2 input upper limit that will cause an interrupt and activate the INT/ $\overline{\text{INT}}$ output (if enabled). For this to happen the measured AIN2 value has to be greater than the value in this register. As it is an 8-bit register the resolution is four times less than the resolution of the 10-Bit ADC. Default value is fullscale voltage.

Table 46. AIN2 V_{HIGH} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1*	1*	1*	1*	1*	1*	1*	1*

*Default settings at Power-up.

AIN2 V_{LOW} LIMIT REGISTER (Read/Write) [Add. = 2Ch]

This limit register is an 8-bit read/write register which stores the AIN2 input lower limit that will cause an interrupt and activate the INT/ $\overline{\text{INT}}$ output (if enabled). For this to happen the measured AIN2 value has to be less than or equal to the value in this register. As it is an 8-bit register the resolution is four times less than the resolution of the 10-Bit ADC. Default value is 0 V.

Table 47. AIN2 V_{LOW} Limit

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D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

AIN3 V_{HIGH} LIMIT REGISTER (Read/Write) [Add. = 2Dh]

This limit register is an 8-bit read/write register which stores the AIN3 input upper limit that will cause an interrupt and activate the INT/ $\overline{\text{INT}}$ output (if enabled). For this to happen the measured AIN3 value has to be greater than the value in this register. As it is an 8-bit register the resolution is four times less than the resolution of the 10-Bit ADC. Default value is fullscale voltage.

Table 48. AIN3 V_{HIGH} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1*	1*	1*	1*	1*	1*	1*	1*

*Default settings at Power-up.

AIN3 V_{LOW} LIMIT REGISTER (Read/Write) [Add. = 2Eh]

This limit register is an 8-bit read/write register which stores the AIN3 input lower limit that will cause an interrupt and activate the INT/ $\overline{\text{INT}}$ output (if enabled). For this to happen the measured AIN3 value has to be less than or equal to the value in this register. As it is an 8-bit register the resolution is four times less than the resolution of the 10-Bit ADC. Default value is 0 V.

Table 49. AIN3 V_{LOW} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

AIN4 V_{HIGH} LIMIT REGISTER (Read/Write) [Add. = 2Fh]

This limit register is an 8-bit read/write register which stores the AIN4 input upper limit that will cause an interrupt and activate the INT/ $\overline{\text{INT}}$ output (if enabled). For this to happen the measured AIN4 value has to be greater than the value in this register. As it is an 8-bit register the resolution is four times less than the resolution of the 10-Bit ADC. Default value is fullscale voltage.

Table 50. AIN4 V_{HIGH} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1*	1*	1*	1*	1*	1*	1*	1*

*Default settings at Power-up.

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AIN4 V_{LOW} LIMIT REGISTER (Read/Write) [Add. = 30h]

This limit register is an 8-bit read/write register which stores the AIN4 input lower limit that will cause an interrupt and activate the INT/ $\overline{\text{INT}}$ output (if enabled). For this to happen the measured AIN4 value has to be less than or equal to the value in this register. As it is an 8-bit register the resolution is four times less than the resolution of the 10-Bit ADC. Default value is 0 V.

Table 51. AIN4 V_{LOW} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

DEVICE ID REGISTER (Read only) [Add. = 4Dh]

This 8-bit read only register indicates which part the device is in the model range. ADT7516 = 03h, ADT7517 = 07h and ADT7518 = 0Bh.

MANUFACTURER'S ID REGISTER (Read only) [Add. = 4Eh]

This register contains the manufacturers identification number. ADI's is 41h.

SILICON REVISION REGISTER (Read only) [Add. = 4Fh]

This register is divided into the four lsbs representing the Stepping and the four msbs representing the Version. The

Stepping contains the manufacturers code for minor revisions or steppings to the silicon. The Version is the ADT7516/17/18 version number. The ADT7516/17/18's version number is 0100b (4h).

SPI LOCK STATUS REGISTER (Read only) [Add. = 7Fh]

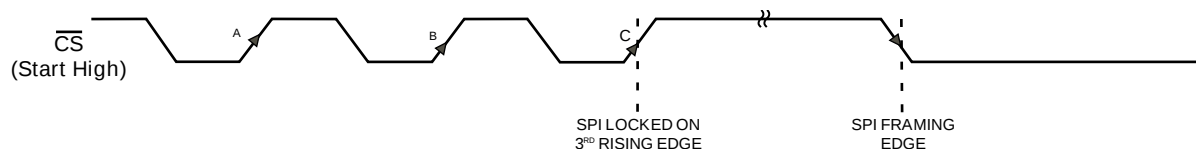
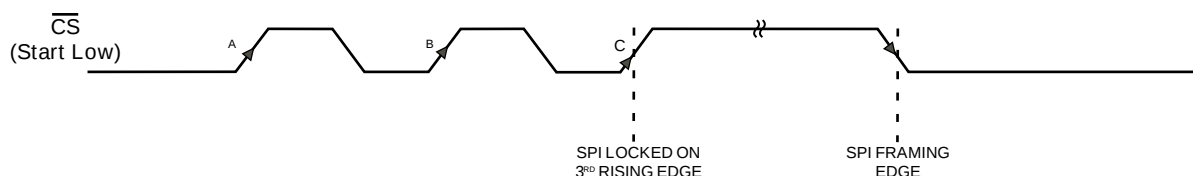
Bit D0 (LSB) of this read only register indicates whether the SPI interface is locked or not. Writing to this register will cause the device to malfunction. Default value is 00h.
0 = I²C interface
1 = SPI interface selected and locked.

ADT7516/7517/7518 SERIAL INTERFACE

There are two serial interfaces that can be used on this part, I²C and SPI. The device will power up with the serial interface in I²C mode but it is not locked into this mode. To stay in I²C mode it is recommended that the user ties the $\overline{\text{CS}}$ line to either V_{CC} or GND. It is not possible to lock the I²C mode but it is possible to select and lock the SPI mode.

To select and lock the interface into the SPI mode, a number of pulses must be sent down the $\overline{\text{CS}}$ (pin 4) line. The following section describes how this is done.

Once the SPI communication protocol has been locked in, it cannot be unlocked while the device is still powered up. Bit D0 of SPI Lock Status register (address = 7Fh) is set to 1 when a successful SPI interface lock has been accomplished. To reset the serial interface the user must

**Figure 22(a). Serial Interface - Selecting and Locking SPI Protocol****Figure 22(b). Serial Interface - Selecting and Locking SPI Protocol**

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power down the part and power up again. A software reset does not reset the serial interface.

SERIAL INTERFACE SELECTION

The $\overline{CS}$ line controls the selection between I²C and SPI. Figure 22 shows the selection process necessary to lock the SPI interface mode.

If the user wants to communicate to the ADT7516/17/18 using the SPI protocol, send three pulses down the $\overline{CS}$ line as shown in figure 22(a) and 22(b). On the third rising edge (marked as C in figure 22) the part selects and locks the SPI interface. The user is now limited to communicating to the device using the SPI protocol.

As per most SPI standards, the $\overline{CS}$ line must be low during every SPI communication to the ADT7516/17/18 and high all other times. Typical examples of how to connect up the dual interface as I²C or SPI is shown in figures 23(a) and 23(b).

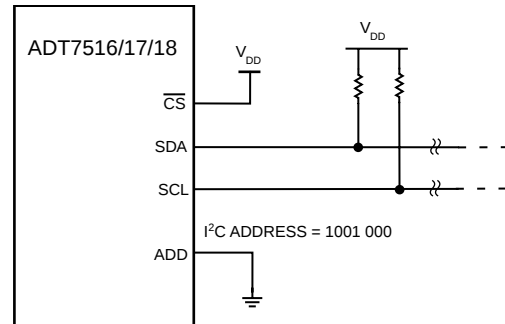


Figure 23(a). Typical I²C Interface Connection

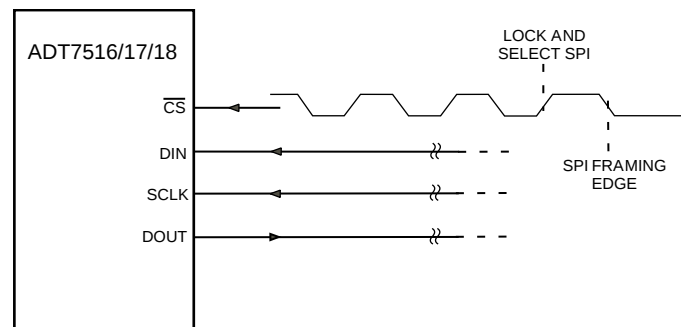


Figure 23(b). Typical SPI Interface Connection

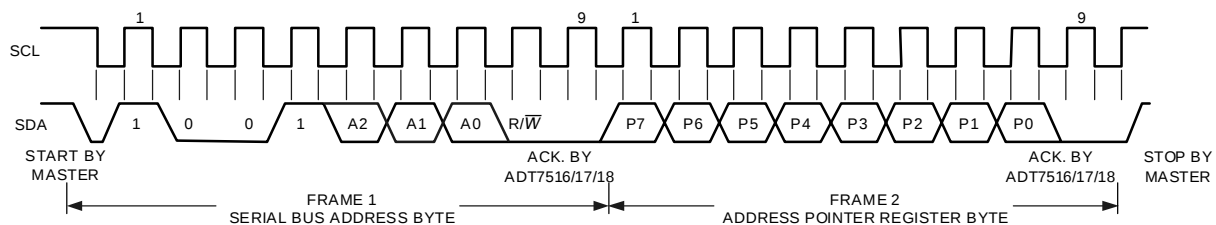


Figure 24. I²C - Writing to the Address Pointer Register to select a register for a subsequent Read operation

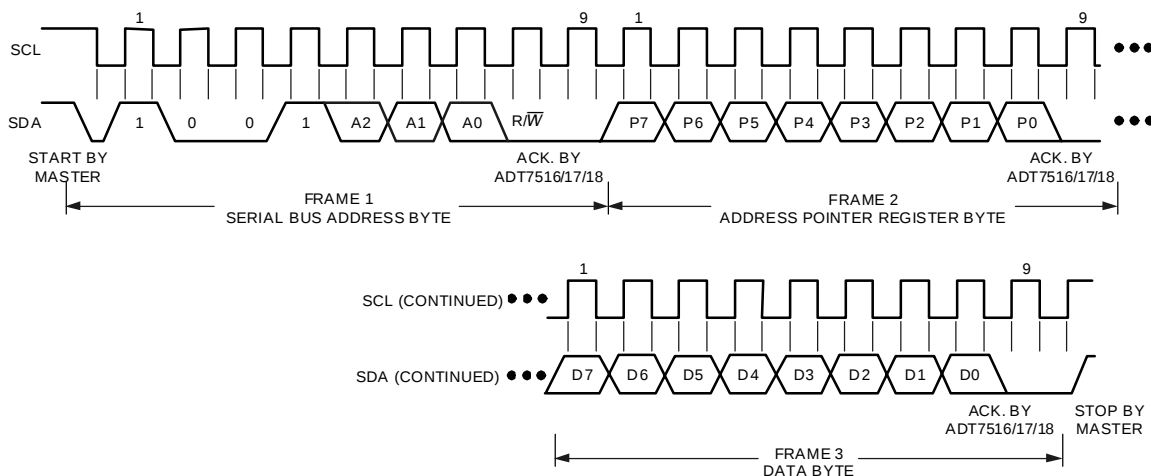


Figure 25. I²C - Writing to the Address Pointer Register followed by a single byte of data to the selected register

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The following sections describe in detail how to use the I²C and SPI protocols associated with the ADT7516/17/18.

I²C SERIAL INTERFACE

Like all I²C-compatible devices, the ADT7516/7517/7518 has an 7-bit serial address. The four MSBs of this address for the ADT7516/7517/7518 are set to 1001. The three LSBs are set by pin 11, ADD. The ADD pin can be configured three ways to give three different address options; low, floating and high. Setting the ADD pin low gives a serial bus address of 1001 000, leaving it floating gives the address 1001 010 and setting it high gives the address 1001 011.

There is an enable/disable bit for the SMBus timeout. When this is enabled the SMBus will timeout after 25 ms of no activity. To enable it, set Bit 6 of Control Configuration 2 register. The power-on default is with the SMBus timeout disabled.

The ADT7516/17/18 supports SMBus Packet Error Checking (PEC) and it's use is optional. It is triggered by supplying the extra clocks for the PEC byte. The PEC is calculated using CRC-8. The Frame Clock Sequence (FCS) conforms to CRC-8 by the polynomial :

$$C(x) = x^8 + x^2 + x^1 + 1$$

Consult SMBus specification (www.smbus.org) for more information.

The serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, defined as a high to low transition on the serial data line SDA whilst the serial clock line SCL remains high. This indicates that an address/data stream will follow. All slave peripherals connected to the serial bus respond to the START condition, and shift in the next 8 bits, consisting of a 7-bit address (MSB first) plus a R/ $\overline{W}$ bit, which determines the direction of the data transfer, i.e. whether data will be written to or read from the slave device.

The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the Acknowledge Bit. All other devices on the bus now remain idle whilst the selected device waits for data to be read from or written to it. If the R/ $\overline{W}$ bit is a 0 then the master will write to the slave device. If the R/ $\overline{W}$ bit is a 1 the master will read from the slave device.

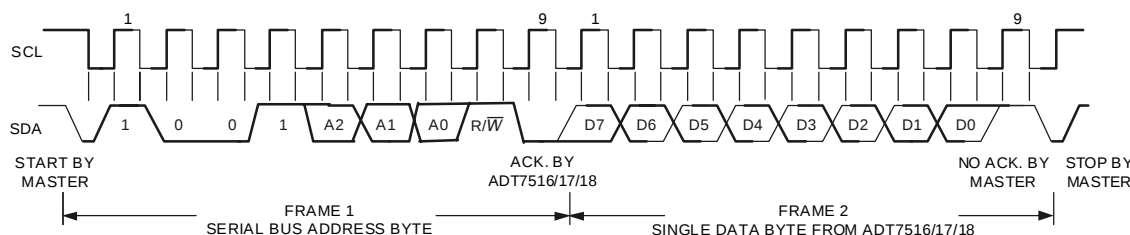


Figure 26. I²C - Reading a single byte of data from a selected register

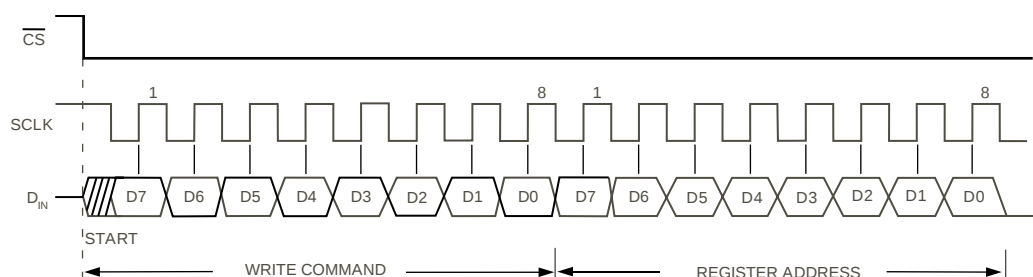


Figure 27. SPI - Writing to the Address Pointer Register followed by a single byte of data to the selected register

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2. Data is sent over the serial bus in sequences of 9 clock pulses, 8 bits of data followed by an Acknowledge Bit from the receiver of data. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, as a low to high transition when the clock is high may be interpreted as a STOP signal.
3. When all data bytes have been read or written, stop conditions are established. In WRITE mode, the master will pull the data line high during the 10th clock pulse to assert a STOP condition. In READ mode, the master device will pull the data line high during the low period before the 9th clock pulse. This is known as No Acknowledge. The master will then take the data line low during the low period before the 10th clock pulse, then high during the 10th clock pulse to assert a STOP condition.

Any number of bytes of data may be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation, because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

The I²C address set up by the ADD pin is not latched by the device until after this address has been sent twice. On the 8th SCL cycle of the second valid communication, the serial bus address is latched in. This is the SCL cycle

directly after the device has seen it's own I²C serial bus address. Any subsequent changes on this pin will have no affect on the I²C serial bus address.

WRITING TO THE ADT7516/7517/7518

Depending on the register being written to, there are two different writes for the ADT7516/7517/7518. It is not possible to do a block write to this part i.e no I²C auto-increment.

Writing to the Address Pointer Register for a subsequent read.

In order to read data from a particular register, the Address Pointer Register must contain the address of that register. If it does not, the correct address must be written to the Address Pointer Register by performing a single-byte write operation, as shown in Figure 24. The write operation consists of the serial bus address followed by the address pointer byte. No data is written to any of the data registers. A read operation is then performed to read the register.

Writing data to a Register.

All registers are 8-bit registers so only one byte of data can be written to each register. Writing a single byte of data to one of these Read/Write registers consists of the serial bus address, the data register address written to the Address Pointer Register, followed by the data byte written

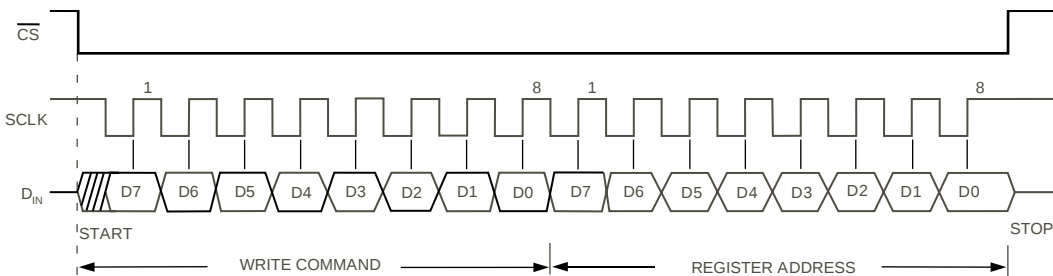


Figure 28. SPI - Writing to the Address Pointer Register to select a register for a subsequent read operation

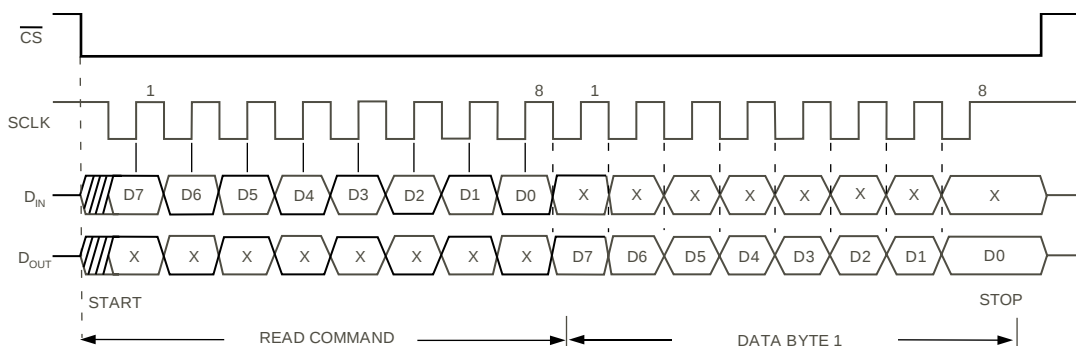


Figure 29. SPI - Reading a single byte of data from a selected register

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to the selected data register. This is illustrated in Figure 25. To write to a different register, another START or repeated START is required. If more than one byte of data is sent in one communication operation, the addressed register will be repeatedly loaded until the last data byte has been sent.

READING DATA FROM THE ADT7516/7517/7518

Reading data from the ADT7516/7517/7518 is done in a one byte operation. Reading back the contents of a register is shown in Figure 26. The register address previously having been set up by a single byte write operation to the Address Pointer Register. If you want to read from another register then you will have to write to the Address Pointer Register again to set up the relevant register address. Thus block reads are not possible i.e. no I²C auto-increment.

SPI SERIAL INTERFACE

The SPI serial interface of the ADT7516/7517/7518 consists of four wires, $\overline{CS}$, SCLK, DIN and DOUT. The $\overline{CS}$ is used to select the device when more than one device is connected to the serial clock and data lines. The $\overline{CS}$ is also used to distinguish between any two separate serial communications, reference Figure 31 for graphical explanation. The SCLK is used to clock data in and out of the part. The DIN line is used to write to the registers and the DOUT line is used to read data back from the registers.

The part operates in a slave mode and requires an externally applied serial clock to the SCLK input. The serial interface is designed to allow the part to be interfaced to systems that provide a serial clock that is synchronized to the serial data.

There are two types of serial operations, a read and a write. Command words are used to distinguish between a read and a write operation. These command words are

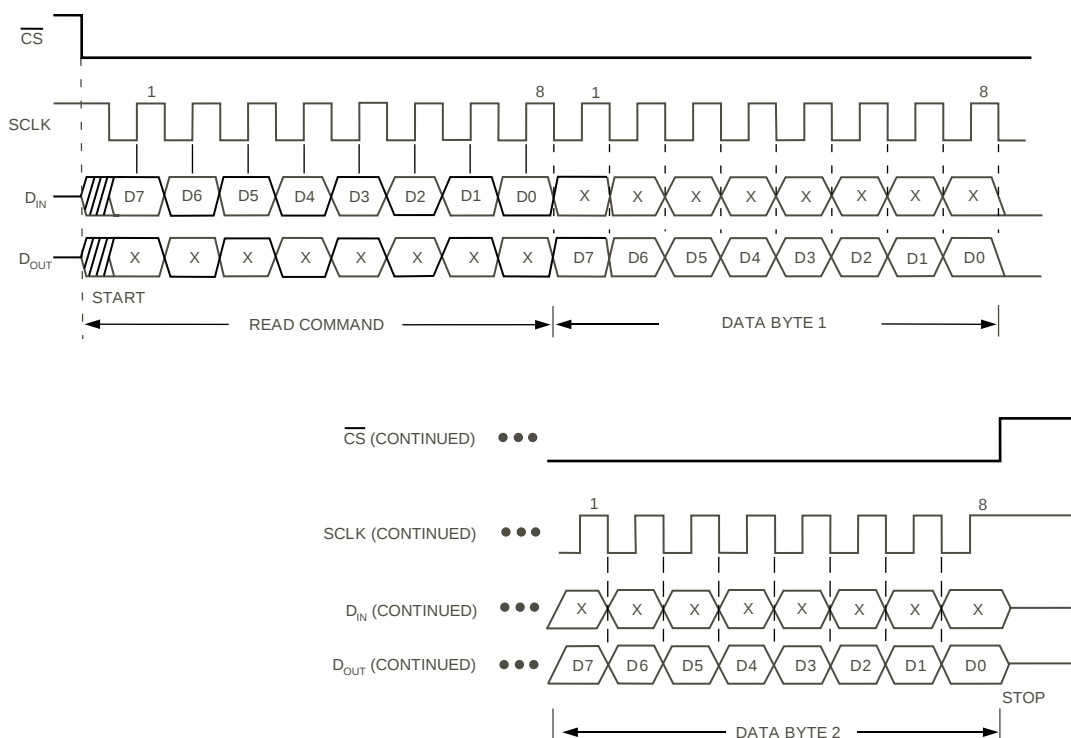


Figure 30. SPI - Reading a two bytes of data from two sequential registers

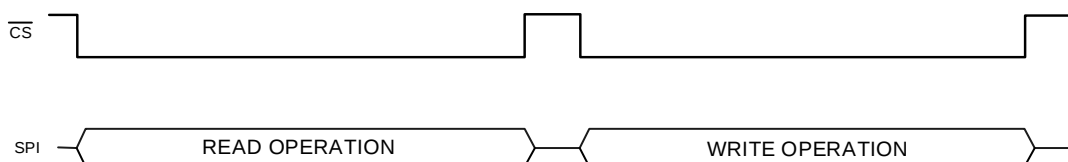


Figure 31. SPI - Correct use of $\overline{CS}$ during SPI communication

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given in Table 52. Address auto-increment is possible in SPI mode.

Table 52. SPI COMMAND WORDS

WRITE	READ
90h (1001 0000)	91h (1001 0001)

Write Operation

Figure 27 shows the timing diagram for a write operation to the ADT7516/7517/7518. Data is clocked into the registers on the rising edge of SCLK. When the $\overline{CS}$ line is high the DIN and DOUT lines are in three-state mode. Only when the $\overline{CS}$ goes from a high to a low does the part accept any data on the DIN line. In SPI mode the Address Pointer Register is capable of auto-incrementing to the next register in the register map without having to load the Address Pointer register each time. In Figure 27 the register address portion of the diagram gives the first register that will be written to. Subsequent data bytes will be written into sequential writable registers. Thus after each data byte has been written into a register, the Address Pointer Register auto increments its value to the next available register. The Address Pointer Register will auto-increment from 00h to 3Fh and will loop back to start all over again at 00h when it reaches 3Fh.

Read Operation

Figures 28 to 30 show the timing diagrams necessary to accomplish correct read operations. To read back from a register you first have to write to the Address Pointer Register with the address of the register you wish to read from. This operation is shown in Figure 28. Figure 29 shows the procedure for reading back a single byte of data. The read command is first sent to the part during the first 8 clock cycles, during the following 8 clock cycles the data contained in the register selected by the Address Pointer register is outputted onto the DOUT line. Data is outputted onto the DOUT line on the falling edge of SCLK. Figure 30 shows the procedure when reading data from two sequential registers. Multiple data reads are possible in SPI interface mode as the Address Pointer Register is auto-incremental. The Address Pointer Register will auto-increment from 00h to 3Fh and will loop back to start all over again at 00h when it reaches 3Fh.

SMBUS/SPI INT/ $\overline{INT}$

The ADT7516/17/18 INT/ $\overline{INT}$ output is an interrupt line for devices that want to trade their ability to master for an extra pin. The ADT7516/17/18 is a slave only device and uses the SMBus/SPI INT/ $\overline{INT}$ to signal the host device that it wants to talk. The SMBus/SPI INT/ $\overline{INT}$ on the ADT7516/17/18 is used as an over/under limit indicator.

The INT/ $\overline{INT}$ pin has an open-drain configuration which allows the outputs of several devices to be wired-AND together when the INT/ $\overline{INT}$ pin is active low. Use C6 of the Control Configuration 1 Register to set the active polarity of the INT/ $\overline{INT}$ output. The power-up default is active low. The INT/ $\overline{INT}$ output can be disabled or enabled by setting C5 of Control Configuration 1 Register to a 1 or 0 respectively.

The INT/ $\overline{INT}$ output becomes active when either the Internal Temperature Value, the External Temperature Value, V_{DD} Value or any of the AIN input values exceed the values in their corresponding T_{HIGH}/V_{HIGH} or T_{LOW}/V_{LOW} Registers. The INT/ $\overline{INT}$ output goes inactive again when a conversion result has the measured value back within the trip limits. The two Interrupt Status registers show which event caused the INT/ $\overline{INT}$ pin to go active.

The INT/ $\overline{INT}$ output requires an external pull-up resistor. This can be connected to a voltage different from V_{DD} provided the maximum voltage rating of the INT/ $\overline{INT}$ output pin is not exceeded. The value of the pull-up resistor depends on the application, but should be as large enough to avoid excessive sink currents at the INT/ $\overline{INT}$ output, which can heat the chip and affect the temperature reading.

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Outline Dimensions
 (Dimensions shown in inches and mm)
16-Lead QSOP Package
(RQ-16)

