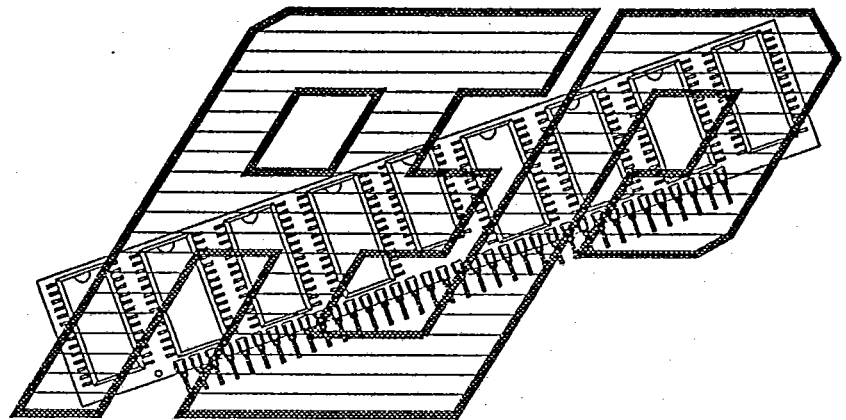


July 30, 1990

AEPSX128K8
STATIC RAM MODULE

T-46-23-14

- >> 131,072 x 8 Organization
- >> Double sided to maximize bit density
- >> On board 1-of-16 Decoder
- >> Completely Static operation
- >> TTL compatible
- >> Low power, battery back-up operation capability
- >> Uses single +5V power supply
- >> Super Low Power version available



128 KILOBYTE STATIC RAM MODULE

DESCRIPTION:

The AEPSx128K8 is a high density 128 Kilo-word by 8 bit static random access memory module in a 36 pin single-inline-package format. Physically it consists of an FR4 PC material substrate mounted with sixteen 8K x 8 SOP (small outline package) ICs, the 1-of-16 decoder, four 0.1 microfarad decoupling capacitors, and 36 edge-clip I/O pins.

The module can use any of the 8K x 8 SRAMs made by any of a large number of manufacturers in both Mix-MOS and CMOS technologies. A wide range of access speeds are available. The decoder normally used is the 74HCT154. Other decoder choices available are the 74F154, the 74HC154, and the fully CMOS version 74F154.

Performance specifications and electrical characteristics are determined by the IC devices used. A typical memory component on the module will draw 100uA (max.) in standby and 70mA (max.) during access (for standard low power devices, super low power use 2uA and 8mA typically).

Mechanical dimensions are 0.88 in. high by 4.79 in. long by 0.28 in. wide. The module is available with either vertical or 90 degree (horizontal) lead pins. The latter allows the module to be mounted on its side which gives a low 0.315 stand-off height.

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ADVANCED ELECTRONIC PKG

AEP SX128K8
STATIC RAM MODULE

T-46-23-14

PART NUMBERING CHART

High Speed 128K x 8	Vertical lead pins	Horizontal lead pins
30ns SRAM ICs	AEPSS128K8-30	AEP SH128K8-30
35ns SRAM ICs	AEPSS128K8-35	AEP SH128K8-35
45ns SRAM ICs	AEPSS128K8-45	AEP SH128K8-45
55ns SRAM ICs	AEPSS128K8-55	AEP SH128K8-55
70ns SRAM ICs	AEPSS128K8-70	AEP SH128K8-70
Standard 128K x 8		
100ns SRAM ICs	AEPSS128K8-10SL	AEP SH128K8-10SL
120ns SRAM ICs	AEPSS128K8-12SL	AEP SH128K8-12SL

Decoder notes:

The standard decoder used with 100ns and slower SRAMs is the HCT154. AEP may substitute the F154 or the LS154 if these are more readily available. The F154 decoder is standard with SRAMs faster than 100ns. On Super Low Power versions of the module the CMOS compatible HC154 is standard. Specific decoders may be ordered with any speed or version of the module by adding -HCT, -HC, -F, or -LS to the end of the part number.

The decoder does effect the memory access speed of the module. The HCT154 can add 35ns in worst case. The F154 adds only 10ns worst case but draws more power. Consult the Signetics data book for details.

Memory notes:

Memory access speeds specified in the part numbers are maximums for the SRAM ICs used. AEP reserves the right to use faster rated devices unless requested not to. As an example, 100ns parts may be substituted for 120ns parts depending on stocks on hand.

Due to the rapidly progressing nature of SRAM development, devices with access speeds other than those listed are likely to be available also. Check with AEP.

Vendor notes:

The IC device specification information which may be included is typical and does not limit AEP to that vendor. The actual devices used will be equivalent depending on price, availability, and customer requirements. AEP will gladly use or exclude particular manufacturers upon request. However, this may affect module price.

Disclaimers:

The Information in this document has been carefully checked and is believed to be reliable. However, Advanced Electronic Packaging Inc. assumes no responsibility for inaccuracies. AEP also reserves the right to change products or specifications without notice.


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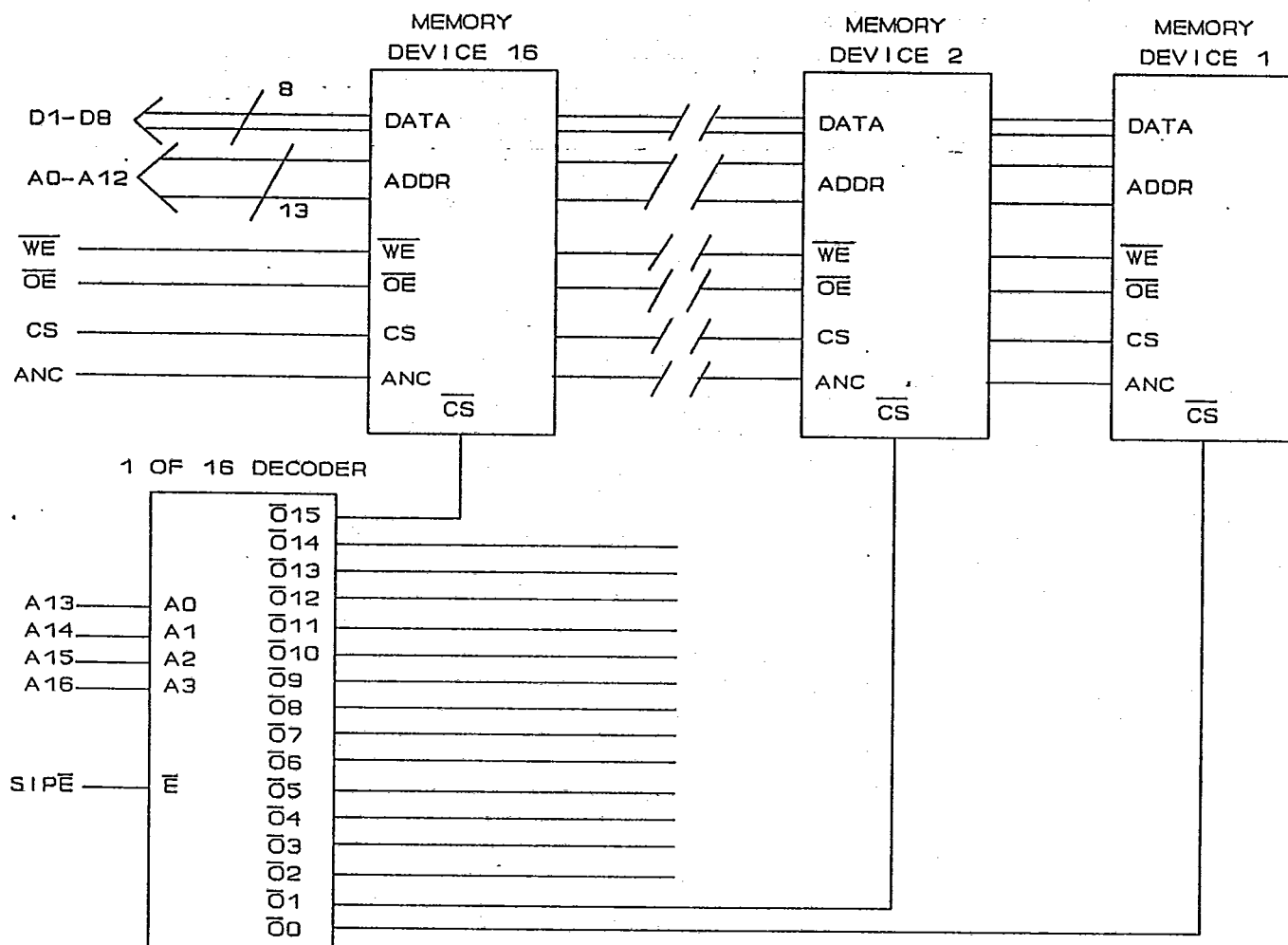
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AEPSX128K8
STATIC RAM MODULE

ADVANCED ELECTRONIC PKG

T-46-23-14

128K x 8 STATIC RAM MODULE FUNCTIONAL DIAGRAM



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AEPSX128K8
STATIC RAM MODULE

T-46-23-14

128K x 8 STATIC RAM MODULE SIP PIN-OUT CONFIGURATION

1	N/C		
2	Vcc		
3	WE	$A_0 - A_{16}$	ADDRESS INPUTS
4	I/O ₃	$I/O_1 - I/O_8$	DATA LINES
5	I/O ₄		
6	I/O ₁		
7	A ₁	WE	WRITE ENABLE*
8	A ₂		
9	A ₃	SIP E	SIP ENABLE*
10	A ₄		
11	Vss	OE	OUTPUT ENABLE*
12	I/O ₆		
13	A ₁₀	Vcc	POWER (+5V)
14	A ₁₁		
15	A ₅	Vss	GROUND
16	A ₁₃		
17	A ₁₄	CS	CHIP SELECT*
18	N/C		
19	SIP E	N/C	NO CONNECT
20	A ₁₅		
21	A ₁₆	AN/C	NO CONNECT
22	A ₁₂		
23	ANC		
24	A ₆		
25	I/O ₂		
26	Vss		
27	A ₀		
28	A ₇		
29	A ₈		
30	A ₉		
31	I/O ₈		
32	I/O ₅		
33	I/O ₇		
34	CS		
35	Vcc		
36	OE		

*ACTIVE LOW

High address notes:

Address inputs A13 to A16 are connected to the decoder on both the 128K and the 512K versions. If compatibility between the two versions is not a concern, then it is recommended making these the highest order address lines when using the 512K module exclusively.



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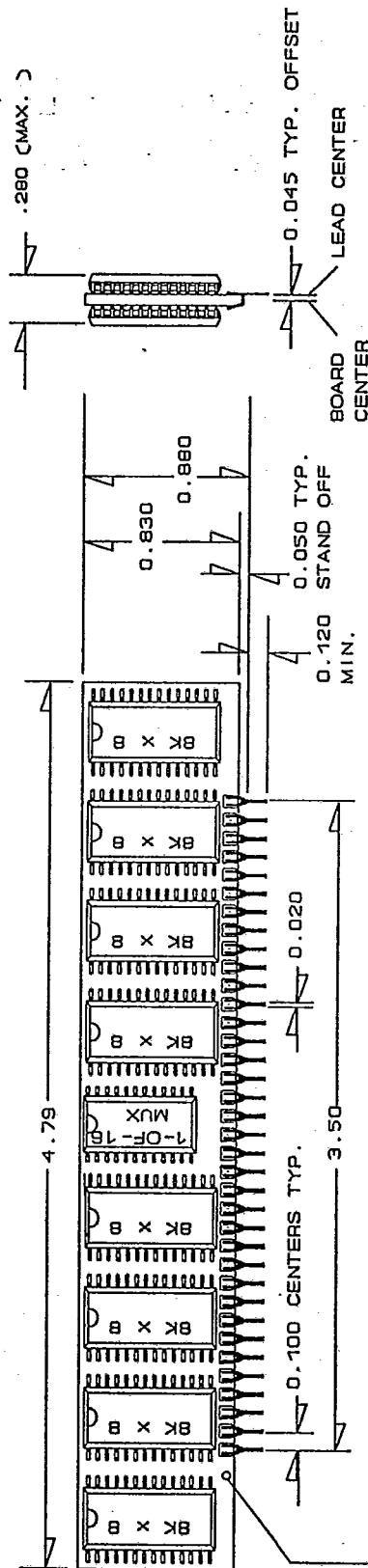
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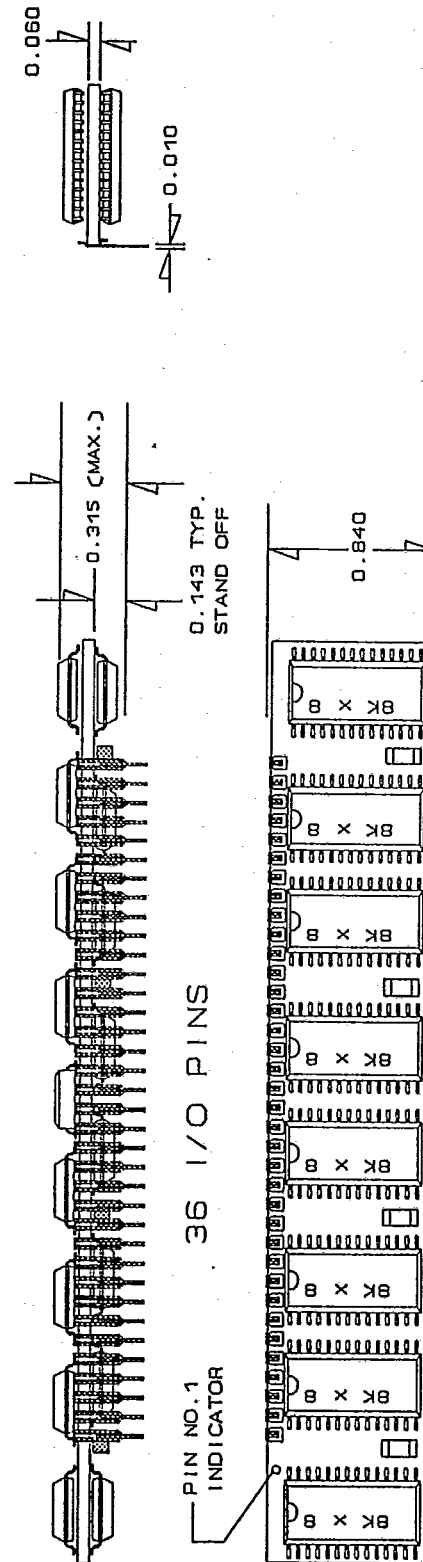
T-46-23-14

ADVANCED ELECTRONIC PACKAGING AEPSX128K8 STATIC RAM MODULE

DIMENSIONS IN INCHES, TOLERANCE: ± 0.010 UNLESS SPECIFIED.



FRONT AND SIDE VIEWS
(SHOWING VERTICAL MOUNTING LEADS OPTION)



BOTTOM, REAR, AND SIDE VIEWS
(SHOWING HORIZONTAL MOUNTING LEADS OPTION)



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