

CD54/74HC03

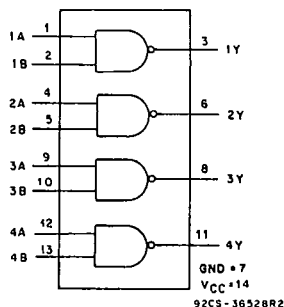
CD54/74HCT03

File Number 1832

HARRIS SEMICONDUCTOR

27E D 4302271 0017463 9 HAS

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Quad 2-Input NAND Gate With Open Drain

Type Features:

- Buffered inputs
- Typical propagation delay = 8 ns @ $V_{CC} = 5\text{ V}$, $C_L = 15\text{ pF}$, $T_A = 25^\circ\text{C}$
- Output pull-up to 10 V

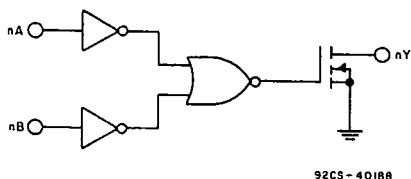
The RCA-CD54/74HC03 and CD54/74HCT03 logic gates utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The 54HCT/74HCT logic family is functionally as well as pin compatible with the standard 54LS/74LS logic family.

These open-drain NAND gates can drive into resistive loads to output voltages as high as 10 V. Minimum values of R_L required vs. load voltage are shown in Fig. 2.

The CD54HC03 and CD54HCT03 are supplied in 14-lead dual-in-line frit-seal ceramic packages (F suffix). The CD74HC03 and CD74HCT03 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- Fanout (over temperature range):
Standard outputs - 10 LSTTL loads
Bus driver outputs - 15 LSTTL loads
- Wide operating temperature range:
CD74HC/HCT: -40 to $+85^\circ\text{C}$
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL logic ICs
- Alternate source is Philips/Signetics
- CD54HC/CD74HC Types:
2 to 6 V Operation
High noise immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} , @ $V_{CC} = 5\text{ V}$
- CD54HCT/CD74HCT Types:
4.5 to 5.5 V Operation
Direct LSTTL input logic compatibility
 $V_{IL} = 0.8\text{ V max.}$, $V_{IH} = 2\text{ V Min.}$
CMOS input compatibility
 $I_I \leq 1\text{ }\mu\text{A}$ @ V_{OL} , V_{OH}



LOGIC DIAGRAM

TRUTH TABLE

A	B	Y	
L	L	Z #	H *
H	L	Z #	H *
L	H	Z #	H *
H	H	L	

* Requires pull-up (R_L to V_L)

Without pull-up (high impedance)

HARRIS SEMICONDUCTOR 27E D 430227J 0017464 0 HAS

T-43-21

Technical Data

CD54/74HC03

CD54/74HCT03

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE, (V _{cc}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I _{IK} (FOR V _I < -0.5 V OR V _I > V _{cc} + 0.5 V)	±20 mA
DC OUTPUT DIODE CURRENT, I _{OK} (FOR V _O < -0.5 V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I _O) (FOR -0.5 V < V _O)	-25 mA
DC V _{cc} OR GROUND CURRENT (I _{cc})	±50 mA
POWER DISSIPATION PER PACKAGE (P _D):	
For T _A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T _A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T _A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T _A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T _A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T _A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T _A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T _{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

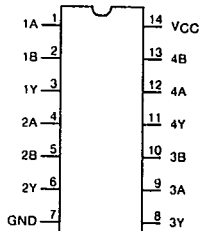
RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T _A = Full Package-Temperature Range) V _{cc} : *			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input Voltage V _I	0	V _{cc}	V
DC Load Voltage V _L	0	10 #	V
Operating Temperature T _A :			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t _r , t _f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

* Unless otherwise specified, all voltages are referenced to Ground.

With pull-up resistor whose value limits output current to 25 mA.



9LCS-38303

TERMINAL ASSIGNMENT

CD54/74HC03

CD54/74HCT03

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC03/CD54HC03											CD74HCT03/CD54HCT03											UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES					
	V _I V	I _O mA	V _{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V _I V	V _{CC} V	+25°C			-40/ +85°C		-55/ +125°C					
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max				
High-Level Input Voltage	V _{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V		
Low-Level Input Voltage	V _{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V		
Low-Level Output Voltage	V _{OL}	V _{IL} or V _{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	—	V _{IL} or V _{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V	
CMOS Loads				4	4.5	—	0.1	—	0.1	—	0.1	—											
TTL Loads		V _{IL} or V _{IH}	5.2	6	—	—	0.26	—	0.33	—	0.4	—	V _{IL} or V _{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V	
Input Leakage Current	I _I	V _{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	—	Any Voltage Between V _{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA	
Quiescent Device Current	I _{CC}	V _{CC} or Gnd	0	6	—	—	2	—	20	—	40	—	V _{CC} or Gnd	5.5	—	—	2	—	20	—	40	μA	
Additional Quiescent Device Current per Input pin: 1 unit load	ΔI _{CC} *												V _{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA	
Output Leakage Current	I _{OZ}	V _{IL}	V _O = 10 V thru 1 KΩ	6	—	—	0.5	—	5	—	10	—	V _I = V _{IL} V _O = 10 V thru 1 KΩ	5.5	—	—	0.5	—	5	—	10	μA	

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS *
nA, nB	1

* Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC03

CD54/74HCT03

SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, Input t_r , $t_f = 6\text{ ns}$)

CHARACTERISTIC	C _L (pF)	TYPICAL VALUES		UNITS	
		HC	HCT		
Propagation Delay, (Fig. 1)	t _{PZL} , t _{PLZ}	15	8	9	ns
Power Dissipation Capacitance *	C _{PD}	—	6.4	9	pF

* C_{PD} is used to determine the dynamic power consumption, per gate.

$$P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_o) + \sum (V_L^2 / R_L) \text{ (Duty Factor "Low")}$$

where f_i = input frequency

f_o = output frequency

C_L = output load capacitance

V_{CC} = supply voltage

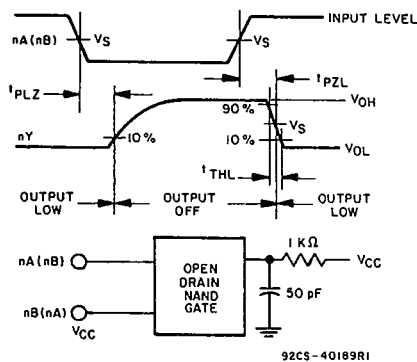
Duty factor "low" = percent of time output is "low"

V_L = output voltage

R_L = pull-up resistor

SWITCHING CHARACTERISTICS ($C_L = 50\text{ pF}$, Input t_r , $t_f = 6\text{ ns}$)

CHARACTERISTIC	TEST CONDITIONS V _{CC} V	LIMITS												UNITS
		25° C				-40° C to +85° C				-55° C to +125° C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay t _{PLZ} Output Low to High Impedance and High Impedance to Output Low	2 4.5 6	— — —	100 20 17	— — —	— 24 —	— — —	125 25 21	— — —	— 30 —	— — —	150 30 26	— — —	— 36 —	ns
Transition Times t _{THL} (Figure 1)	2 4.5 6	— — —	75 15 13	— — —	— 15 —	— — —	95 19 16	— — —	— 19 —	— — —	110 22 19	— — —	— 22 —	ns
Input Capacitance C _I		—	10	—	10	—	10	—	10	—	10	—	10	pF



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 1 - Transition times, propagation delay times, and test circuit.

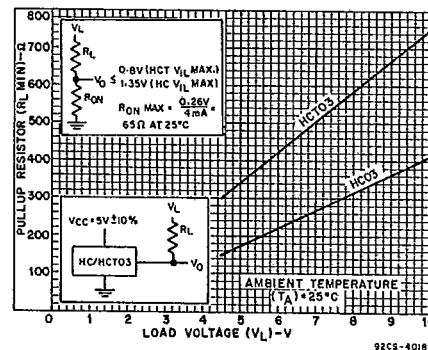


Fig. 2 - Minimum resistive load vs load voltage.