CY2SSTU32864

1.8V, 25-bit (1:1) or 14-bit (1:2) JEDEC-Compliant Data Register

Features

- **Operating frequency: DC to 333 MHz**
- **Supports DDRII SDRAM**
- **Two operations modes: 25 bit (1:1) and 14 bit (1:2)**
- **1.8V operation**
- **Fully JEDEC-compliant**
- **96-ball LFBGA**

Description

All clock and data inputs are compatible with the JEDEC standard for SSTL_18. The control inputs are LVCMOS. All outputs are 1.8-V CMOS drivers that have been optimized to drive the DDR-II DIMM load. The SSTU32864 operates from a differential clock (CK and CK#). Data are registered at the crossing of CK going high, and CK# going low.

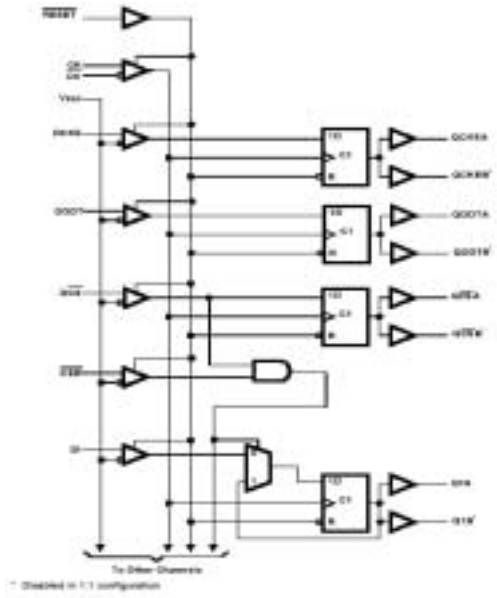
The C0 input controls the pinout configuration of the 1:2 pinout from A configuration (when low) to B configuration (when high). The C1 input controls the pinout configuration from 25-bit 1:1 (when low) to 14-bit 1:2 (when high). C0 = 1 and C1 = 0 is not allowed and should default to the C0 = C1 = 0 state.

The device monitors both DCS# and CSR# inputs and will gate the Qn outputs from changing states when both DCS# and CSR# inputs are high. If either DCS# or CSR# input is low, the Qn outputs will function normally. The RESET input has priority over the DCS# and CSR# control and will force the outputs low. If the DCS#-control functionality is not desired, the CSR# input can be hardwired to ground, in which case the set-up time requirement for DCS# would be the same as for the other D data inputs.

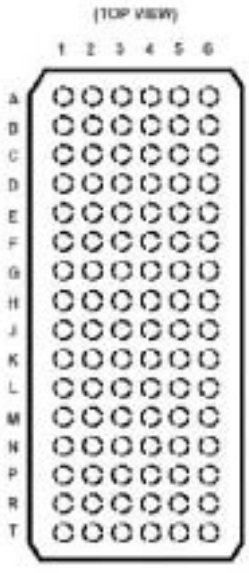
The device supports low-power standby operation. When the reset input (RESET#) is low, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage (VREF) inputs are allowed. In addition, when RESET# is low, all registers are reset and all outputs are forced low. The LVCMOS RESET# and Cn inputs must always be held at a valid logic high or low level. To ensure defined outputs from the register before a stable clock has been supplied, RESET# must be held in the low state during power-up.

In the DDR-II RDIMM application, RESET# is specified to be completely asynchronous with respect to CK and CK#. Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the outputs will be driven low quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers.

Block Diagram



Pin Configuration



Document History Page

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**	129199	09/09/03	RGL	New Data Sheet