



**CYDM256B16**  
**CYDM128B16**  
**CYDM064B16**

## 1.8V 4K/8K/16K x 16 MoBL<sup>®</sup> Dual-Port Static RAM

### Features

- True dual-ported memory cells that allow simultaneous access of the same memory location
- 4/8/16K x 16 organization
- High-speed access: 40 ns
- Ultra Low operating power
  - Active:  $I_{CC} = 15 \text{ mA}$  (typical) at 55 ns
  - Active:  $I_{CC} = 25 \text{ mA}$  (typical) at 40 ns
  - Standby:  $I_{SB3} = 2 \mu\text{A}$  (typical)
- Small footprint: Available in a 6x6 mm 100-pin Lead(Pb)-free vFBGA
- Port-independent 1.8V, 2.5V, and 3.0V I/Os
- Full asynchronous operation
- Automatic power-down
- Pin select for Master or Slave
- Expandable data bus to 32 bits with Master/Slave chip select when using more than one device
- On-chip arbitration logic
- Semaphores included to permit software handshaking between ports
- Input Read Registers and Output Drive Registers
- INT flag for port-to-port communication
- Separate upper-byte and lower-byte control
- Industrial temperature ranges

### Selection Guide for $V_{CC} = 1.8\text{V}$

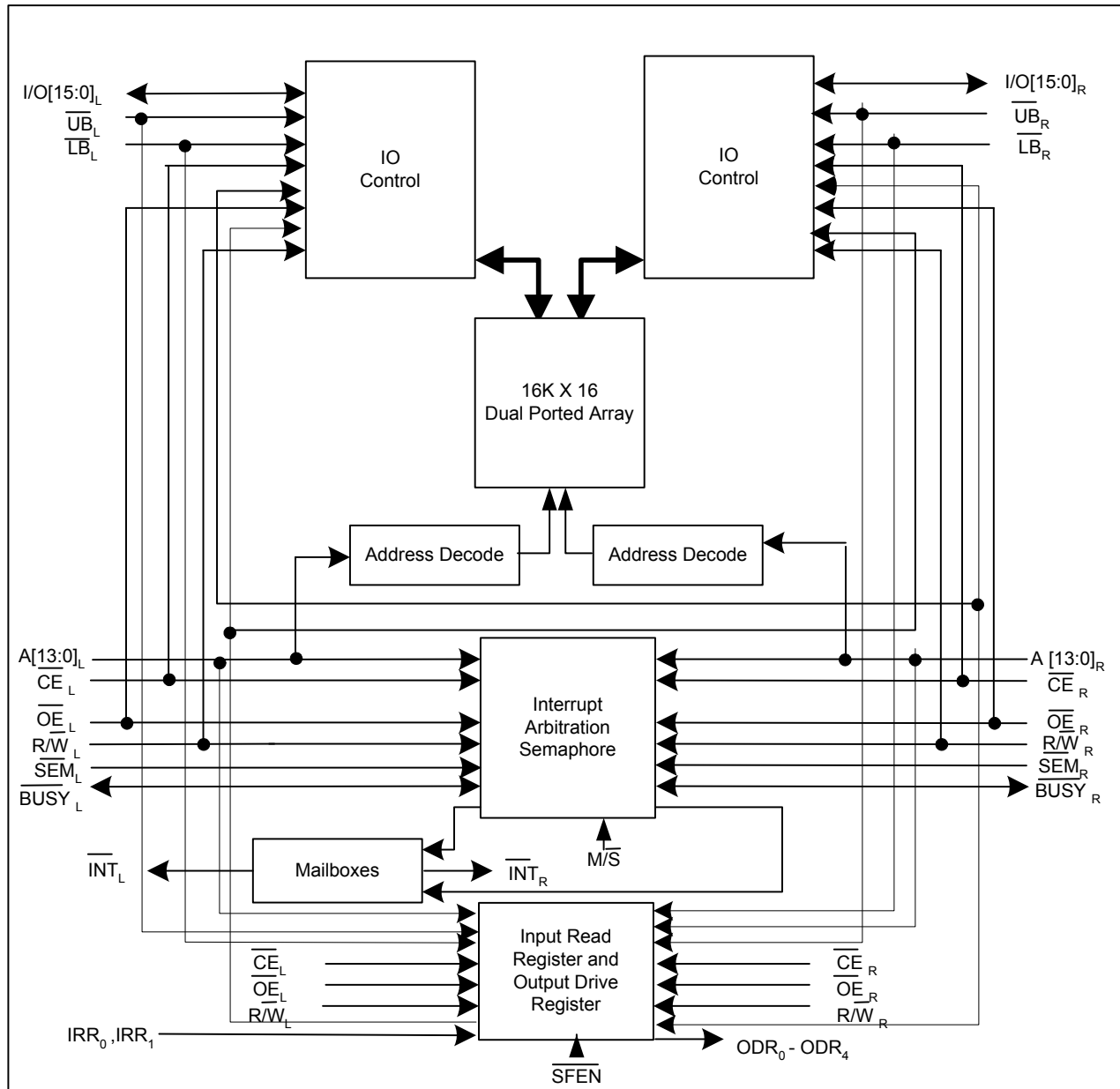
	CYDM256B16, CYDM128B16, CYDM064B16 -40	CYDM256B16, CYDM128B16, CYDM064B16 -55	Unit
Port I/O Voltages (P1-P2)	1.8V-1.8V	1.8V-1.8V	
Maximum Access Time	40	55	ns
Typical Operating Current	25	15	mA
Typical Standby Current for $I_{SB1}$	2	2	$\mu\text{A}$
Typical Standby Current for $I_{SB3}$	2	2	$\mu\text{A}$

### Selection Guide for $V_{CC} = 2.5\text{V}$

	CYDM256B16, CYDM128B16, CYDM064B16 -40	CYDM256B16, CYDM128B16, CYDM064B16 -55	Unit
Port I/O Voltages (P1-P2)	2.5V-2.5V	2.5V-2.5V	
Maximum Access Time	40	55	ns
Typical Operating Current	39	28	mA
Typical Standby Current for $I_{SB1}$	6	6	$\mu\text{A}$
Typical Standby Current for $I_{SB3}$	4	4	$\mu\text{A}$

### Selection Guide for $V_{CC} = 3.0\text{V}$

	CYDM256B16, CYDM128B16, CYDM064B16 -40	CYDM256B16, CYDM128B16, CYDM064B16 -55	Unit
Port I/O Voltages (P1-P2)	3.0V-3.0V	3.0V-3.0V	
Maximum Access Time	40	55	ns
Typical Operating Current	49	42	mA
Typical Standby Current for $I_{SB1}$	7	7	$\mu\text{A}$
Typical Standby Current for $I_{SB3}$	6	6	$\mu\text{A}$



**Figure 1. Top Level Block Diagram**<sup>[1, 2]</sup>

**Notes:**

1.  $A_0$ - $A_{11}$  for 4K devices;  $A_0$ - $A_{12}$  for 8K devices;  $A_0$ - $A_{13}$  for 16K devices.
2. BUSY is an output in master mode and an input in slave mode.

**Pin Configurations** [3, 4, 5, 6, 7]

**100-Ball 0.5-mm Pitch BGA**  
**Top View**  
**CYDM064B16/CYDM128B16/CYDM256B16**

	1	2	3	4	5	6	7	8	9	10
A	A <sub>5R</sub>	A <sub>8R</sub>	A <sub>11R</sub>	$\overline{UB}_R$	V <sub>SS</sub>	$\overline{SEM}_R$	I/O <sub>15R</sub>	I/O <sub>12R</sub>	I/O <sub>10R</sub>	V <sub>SS</sub>
B	A <sub>3R</sub>	A <sub>4R</sub>	A <sub>7R</sub>	A <sub>9R</sub>	$\overline{CE}_R$	R/ $\overline{W}_R$	$\overline{OE}_R$	V <sub>DDIOR</sub>	I/O <sub>9R</sub>	I/O <sub>6R</sub>
C	A <sub>0R</sub>	A <sub>1R</sub>	A <sub>2R</sub>	A <sub>6R</sub>	$\overline{LB}_R$	IRR1 <sup>[6]</sup>	I/O <sub>14R</sub>	I/O <sub>11R</sub>	I/O <sub>7R</sub>	V <sub>SS</sub>
D	ODR4	ODR2	$\overline{BUSY}_R$	$\overline{INT}_R$	A <sub>10R</sub>	A <sub>12R</sub> <sup>[3]</sup>	I/O <sub>13R</sub>	I/O <sub>8R</sub>	I/O <sub>5R</sub>	I/O <sub>2R</sub>
E	V <sub>SS</sub>	$\overline{M/S}$	ODR3	$\overline{INT}_L$	V <sub>SS</sub>	V <sub>SS</sub>	I/O <sub>4R</sub>	V <sub>DDIOR</sub>	I/O <sub>1R</sub>	V <sub>SS</sub>
F	$\overline{SFEN}$	ODR1	$\overline{BUSY}_L$	A <sub>1L</sub>	V <sub>CC</sub>	V <sub>SS</sub>	I/O <sub>3R</sub>	I/O <sub>0R</sub>	I/O <sub>15L</sub>	V <sub>DDIOL</sub>
G	ODR0	A <sub>2L</sub>	A <sub>5L</sub>	A <sub>12L</sub> <sup>[3]</sup>	$\overline{OE}_L$	I/O <sub>3L</sub>	I/O <sub>11L</sub>	I/O <sub>12L</sub>	I/O <sub>14L</sub>	I/O <sub>13L</sub>
H	A <sub>0L</sub>	A <sub>4L</sub>	A <sub>9L</sub>	$\overline{LB}_L$	$\overline{CE}_L$	I/O <sub>1L</sub>	V <sub>DDIOL</sub>	NC <sup>[7]</sup>	NC <sup>[7]</sup>	I/O <sub>10L</sub>
J	A <sub>3L</sub>	A <sub>7L</sub>	A <sub>10L</sub>	IRR0 <sup>[5]</sup>	V <sub>CC</sub>	V <sub>SS</sub>	I/O <sub>4L</sub>	I/O <sub>6L</sub>	I/O <sub>8L</sub>	I/O <sub>9L</sub>
K	A <sub>6L</sub>	A <sub>8L</sub>	A <sub>11L</sub>	$\overline{UB}_L$	$\overline{SEM}_L$	R/ $\overline{W}_L$	I/O <sub>0L</sub>	I/O <sub>2L</sub>	I/O <sub>5L</sub>	I/O <sub>7L</sub>
	1	2	3	4	5	6	7	8	9	10

**Notes:**

3. A12L and A12R are NC pins for CYDM064B16.
4. IRR functionality is not supported for the CYDM256B16 device.
5. This pin is A13L for CYDM256B16 device.
6. This pin is A13R for CYDM256B16 device.
7. Leave this pin unconnected. No trace or power component can be connected to this pin.

## Pin Definitions

Left Port	Right Port	Description
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$\overline{R/W}_L$	$\overline{R/W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L}-A_{13L}$	$A_{0R}-A_{13R}$	Address ( $A_0-A_{11}$ for 4K devices; $A_0-A_{12}$ for 8K devices; $A_0-A_{13}$ for 16K devices).
$I/O_{0L}-I/O_{15L}$	$I/O_{0R}-I/O_{15R}$	Data Bus Input/Output for x16 devices
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select ( $I/O_8-I/O_{15}$ ).
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select ( $I/O_0-I/O_7$ ).
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
IRR0, IRR1		Input Read Register for CYDM064B16, CYDM128B16. A13L, A13R for CYDM256B16.
ODR0-ODR4		Output Drive Register; These outputs are Open Drain.
$\overline{SFEN}$		Special Function Enable
$\overline{M/S}$		Master or Slave Select
$V_{CC}$		Core Power
GND		Ground
$V_{DDIOL}$		Left Port I/O Voltage
$V_{DDIOR}$		Right Port I/O Voltage
NC		No Connect. Leave this pin Unconnected.

## Functional Description

The CYDM256B16, CYDM128B16, CYDM064B16 are low-power CMOS 4K, 8K, 16K x 16 dual-port static RAMs. Arbitration schemes are included on the devices to handle situations when multiple processors access the same piece of data. Two ports are provided, permitting independent, asynchronous access for reads and writes to any location in memory. The devices can be utilized as standalone 16-bit dual-port static RAMs or multiple devices can be combined in order to function as a 32-bit or wider master/slave dual-port static RAM. An M/S pin is provided for implementing 32-bit or wider memory applications without the need for separate master and slave devices or additional discrete logic. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: Chip Enable ( $\overline{CE}$ ), Read or Write Enable (R/W), and Output Enable ( $\overline{OE}$ ). Two flags are provided on each port (BUSY and INT). BUSY signals that the port is trying to access the same location currently being accessed by the other port. The Interrupt flag (INT) permits communication between ports or systems by means of a mail box. The semaphores are used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power-down feature is controlled independently on each port by a Chip Enable (CE) pin.

The CYDM256B16, CYDM128B16, CYDM064B16 are available in 100-ball 0.5-mm pitch Ball Grid Array (BGA) packages.

### Power Supply

The core voltage ( $V_{CC}$ ) can be 1.8V, 2.5V or 3.0V, as long as it is lower than or equal to the I/O voltage.

Each port can operate on independent I/O voltages. This is determined by what is connected to the  $V_{DDIOL}$  and  $V_{DDIOR}$  pins. The supported I/O standards are 1.8V/2.5V LVCMOS and 3.0V LVTTTL.

### Write Operation

Data must be set up for a duration of  $t_{SD}$  before the rising edge of R/W in order to guarantee a valid write. A write operation is controlled by either the R/W pin (see Write Cycle No. 1 waveform) or the  $\overline{CE}$  pin (see Write Cycle No. 2 waveform). Required inputs for non-contention operations are summarized in Table 1.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must occur before the data is read on the output; otherwise the data read is not deterministic. Data will be valid on the port  $t_{DD}$  after the data is presented on the other port.

### Read Operation

When reading the device, the user must assert both the  $\overline{OE}$  and CE pins. Data will be available  $t_{ACE}$  after CE or  $t_{DOE}$  after  $\overline{OE}$  is asserted. If the user wishes to access a semaphore flag,

then the  $\overline{\text{SEM}}$  pin must be asserted instead of the  $\overline{\text{CE}}$  pin, and OE must also be asserted.

### Interrupts

The upper two memory locations may be used for message passing. The highest memory location (FFF for the CYDM064B16, 1FFF for the CYDM128B16, 3FFF for the CYDM256B16) is the mailbox for the right port and the second-highest memory location (FFE for the CYDM064B16, 1FFE for the CYDM128B16, 3FFE for the CYDM256B16) is the mailbox for the left port. When one port writes to the other port's mailbox, an interrupt is generated to the owner. The interrupt is reset when the owner reads the contents of the mailbox. The message is user-defined.

Each port can read the other port's mailbox without resetting the interrupt. The active state of the busy signal (to a port) prevents the port from setting the interrupt to the winning port. Also, an active busy to a port prevents that port from reading its own mailbox and, thus, resetting the interrupt to it.

If an application does not require message passing, do not connect the interrupt pin to the processor's interrupt request input pin. On power up, an initialization program should be run and the interrupts for both ports must be read to reset them.

The operation of the interrupts and their interaction with Busy are summarized in *Table 2*.

### Busy

The CYDM256B16, CYDM128B16, CYDM064B16 provide on-chip arbitration to resolve simultaneous memory location access (contention). If both ports'  $\overline{\text{CE}}$ s are asserted and an address match occurs within  $t_{\text{PS}}$  of each other, the busy logic will determine which port has access. If  $t_{\text{PS}}$  is violated, one port will definitely gain permission to the location, but it is not predictable which port will get that permission. BUSY will be asserted  $t_{\text{BLA}}$  after an address match or  $t_{\text{BLC}}$  after  $\overline{\text{CE}}$  is taken LOW.

### Master/Slave

A  $\overline{\text{M/S}}$  pin is provided in order to expand the word width by configuring the device as either a master or a slave. The BUSY output of the master is connected to the BUSY input of the slave. This will allow the device to interface to a master device with no external components. Writing to slave devices must be delayed until after the BUSY input has settled ( $t_{\text{BLC}}$  or  $t_{\text{BLA}}$ ), otherwise, the slave chip may begin a write cycle during a contention situation. When tied HIGH, the  $\overline{\text{M/S}}$  pin allows the device to be used as a master and, therefore, the BUSY line is an output. BUSY can then be used to send the arbitration outcome to a slave.

### Input Read Register

The Input Read Register (IRR) captures the status of two external input devices that are connected to the Input Read pins.

The contents of the IRR read from address x0000 from either port. During reads from the IRR, DQ0 and DQ1 are valid bits and DQ<15:2> are don't care. Writes to address x0000 are not allowed from either port.

Address x0000 is not available for standard memory accesses when  $\text{SFEN} = V_{\text{IL}}$ . When  $\text{SFEN} = V_{\text{IH}}$ , address x0000 is available for memory accesses.

The inputs will be 1.8V/2.5V LVCMOS or 3.0V LVTTL, depending on the core voltage supply ( $V_{\text{CC}}$ ). Refer to *Table 3* for Input Read Register operation.

IRR is not available in the CYDM256B16, as the IRR pins are used as extra address pins  $A_{13L}$  and  $A_{13R}$ .

### Output Drive Register

The Output Drive Register (ODR) determines the state of up to five external binary state devices by providing a path to  $V_{\text{SS}}$  for the external circuit. These outputs are Open Drain.

The five external devices can operate at different voltages ( $1.5V \leq V_{\text{DDIO}} \leq 3.5V$ ) but the combined current cannot exceed 40 mA (8 mA max for each external device). The status of the ODR bits are set using standard write accesses from either port to address x0001 with a "1" corresponding to on and "0" corresponding to off.

The status of the ODR bits can be read with a standard read access to address x0001. When  $\text{SFEN} = V_{\text{IL}}$ , the ODR is active and address x0001 is not available for memory accesses. When  $\text{SFEN} = V_{\text{IH}}$ , the ODR is inactive and address x0001 can be used for standard accesses.

During reads and writes to ODR DQ<4:0> are valid and DQ<15:5> are don't care. Refer to *Table 4* for Output Drive Register operation.

### Semaphore Operation

The CYDM256B16, CYDM128B16, CYDM064B16 provide eight semaphore latches, which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a zero to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore,  $\overline{\text{SEM}}$  or  $\overline{\text{OE}}$  must be deasserted for  $t_{\text{SOP}}$  before attempting to read the semaphore. The semaphore value will be available  $t_{\text{SWRD}} + t_{\text{DOE}}$  after the rising edge of the semaphore write. If the left port was successful (reads a zero), it assumes control of the shared resource, otherwise (reads a one) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a one), the left side will succeed in gaining control of the semaphore. If the left side no longer requires the semaphore, a one is written to cancel its request.

Semaphores are accessed by asserting  $\overline{\text{SEM}}$  LOW. The  $\overline{\text{SEM}}$  pin functions as a chip select for the semaphore latches ( $\overline{\text{CE}}$  must remain HIGH during  $\overline{\text{SEM}}$  LOW).  $A_{0-2}$  represents the semaphore address.  $\overline{\text{OE}}$  and R/W are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O<sub>0</sub> is used. If a zero is written to the left port of an available semaphore, a one will appear at the same semaphore address on the right port. That semaphore can now only be modified by the side showing zero (the left port in this case). If the left port now relinquishes control by writing a one to the semaphore, the semaphore will be set to one for both sides. However, if the right port had requested the semaphore (written a zero) while the left port had control, the right port would immediately own the semaphore as soon as the left port released it. *Table 5* shows sample semaphore operations.



When reading a semaphore, all sixteen data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within  $t_{SPS}$  of each other, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore. On power-up, both ports should write "1" to all eight semaphores.

### Architecture

The CYDM256B16, CYDM128B16, CYDM064B16 consist of an array of 4K, 8K, or 16K words of 16 dual-port RAM cells,

I/O and address lines, and control signals ( $\overline{CE}$ ,  $\overline{OE}$ ,  $R/\overline{W}$ ). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a BUSY pin is provided on each port. Two Interrupt (INT) pins can be utilized for port-to-port communication. Two Semaphore (SEM) control pins are used for allocating shared resources. With the M/S pin, the devices can function as a master (BUSY pins are outputs) or as a slave (BUSY pins are inputs). The devices also have an automatic power-down feature controlled by  $\overline{CE}$ . Each port is provided with its own output enable control (OE), which allows data to be read from the device.

**Table 1. Non-Contending Read/Write**

Inputs						Outputs		Operation
CE	R/W	OE	UB	LB	SEM	I/O <sub>8</sub> -I/O <sub>15</sub>	I/O <sub>0</sub> -I/O <sub>7</sub>	
H	X	X	X	X	H	High Z	High Z	Deselected: Power-down
X	X	X	H	H	H	High Z	High Z	Deselected: Power-down
L	L	X	L	H	H	Data In	High Z	Write to Upper Byte Only
L	L	X	H	L	H	High Z	Data In	Write to Lower Byte Only
L	L	X	L	L	H	Data In	Data In	Write to Both Bytes
L	H	L	L	H	H	Data Out	High Z	Read Upper Byte Only
L	H	L	H	L	H	High Z	Data Out	Read Lower Byte Only
L	H	L	L	L	H	Data Out	Data Out	Read Both Bytes
X	X	H	X	X	X	High Z	High Z	Outputs Disabled
H	H	L	X	X	L	Data Out	Data Out	Read Data in Semaphore Flag
X	H	L	H	H	L	Data Out	Data Out	Read Data in Semaphore Flag
H		X	X	X	L	Data In	Data In	Write D <sub>IN0</sub> into Semaphore Flag
X		X	H	H	L	Data In	Data In	Write D <sub>IN0</sub> into Semaphore Flag
L	X	X	L	X	L			Not Allowed
L	X	X	X	L	L			Not Allowed

**Table 2. Interrupt Operation Example (Assumes  $\overline{BUSY}_L = \overline{BUSY}_R = \text{HIGH}$ )<sup>[8]</sup>**

Function	Left Port					Right Port				
	R/W <sub>L</sub>	CE <sub>L</sub>	OE <sub>L</sub>	A <sub>0L-13L</sub>	INT <sub>L</sub>	R/W <sub>R</sub>	CE <sub>R</sub>	OE <sub>R</sub>	A <sub>0R-13R</sub>	INT <sub>R</sub>
Set Right $\overline{INT}_R$ Flag	L	L	X	3FFF <sup>[11]</sup>	X	X	X	X	X	L <sup>[10]</sup>
Reset Right $\overline{INT}_R$ Flag	X	X	X	X	X	X	L	L	3FFF <sup>[11]</sup>	H <sup>[9]</sup>
Set Left $\overline{INT}_L$ Flag	X	X	X	X	L <sup>[9]</sup>	L	L	X	3FFE <sup>[11]</sup>	X
Reset Left $\overline{INT}_L$ Flag	X	L	L	3FFE <sup>[11]</sup>	H <sup>[10]</sup>	X	X	X	X	X

**Notes:**

- 8. See Interrupts Functional Description for specific highest memory locations by device.
- 9. If  $\overline{BUSY}_R = L$ , then no change.
- 10. If  $\overline{BUSY}_L = L$ , then no change.
- 11. See Functional Description for specific addresses by device.

**Table 3. Input Read Register Operation**<sup>[12, 15]</sup>

SFEN	CE	R/W	OE	UB	LB	ADDR	I/O <sub>0</sub> -I/O <sub>4</sub>	I/O <sub>5</sub> -I/O <sub>15</sub>	Mode
H	L	H	L	L	L	x0000-Max	VALID <sup>[13]</sup>	VALID <sup>[13]</sup>	Standard Memory Access
L	L	H	L	X	L	x0000	VALID <sup>[14]</sup>	X	IRR Read

**Table 4. Output Drive Register**<sup>[16]</sup>

SFEN	CE	R/W	OE	UB	LB	ADDR	I/O <sub>0</sub> -I/O <sub>4</sub>	I/O <sub>5</sub> -I/O <sub>15</sub>	Mode
H	L	H	X <sup>[17]</sup>	L <sup>[13]</sup>	L <sup>[13]</sup>	x0000-Max	VALID <sup>[13]</sup>	VALID <sup>[13]</sup>	Standard Memory Access
L	L	L	X	X	L	x0001	VALID <sup>[14]</sup>	X	ODR Write <sup>[16, 18]</sup>
L	L	H	L	X	L	x0001	VALID <sup>[14]</sup>	X	ODR Read <sup>[16]</sup>

**Table 5. Semaphore Operation Example**

Function	I/O <sub>0</sub> -I/O <sub>15</sub> Left	I/O <sub>0</sub> -I/O <sub>15</sub> Right	Status
No action	1	1	Semaphore-free
Left port writes 0 to semaphore	0	1	Left Port has semaphore token
Right port writes 0 to semaphore	0	1	No change. Right side has no write access to semaphore
Left port writes 1 to semaphore	1	0	Right port obtains semaphore token
Left port writes 0 to semaphore	1	0	No change. Left port has no write access to semaphore
Right port writes 1 to semaphore	0	1	Left port obtains semaphore token
Left port writes 1 to semaphore	1	1	Semaphore-free
Right port writes 0 to semaphore	1	0	Right port has semaphore token
Right port writes 1 to semaphore	1	1	Semaphore free
Left port writes 0 to semaphore	0	1	Left port has semaphore token
Left port writes 1 to semaphore	1	1	Semaphore-free

**Notes:**

12. SFEN = V<sub>IL</sub> for IRR reads
13. UB or LB = V<sub>IL</sub>. If LB = V<sub>IL</sub>, then DQ<7:0> are valid. If UB = V<sub>IL</sub> then DQ<15:8> are valid.
14. LB must be active (LB = V<sub>IL</sub>) for these bits to be valid.
15. SFEN active when either CE<sub>L</sub> = V<sub>IL</sub> or CE<sub>R</sub> = V<sub>IL</sub>. It is inactive when CE<sub>L</sub> = CE<sub>R</sub> = V<sub>IH</sub>.
16. SFEN = V<sub>IL</sub> for ODR reads and writes.
17. Output enable must be low (OE = V<sub>IL</sub>) during reads for valid data to be output.
18. During ODR writes data will also be written to the memory.



**Maximum Ratings**<sup>[19]</sup>

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature .....-65°C to +150°C
- Ambient Temperature with Power Applied.....-55°C to +125°C
- Supply Voltage to Ground Potential ..... -0.5V to +3.3V
- DC Voltage Applied to Outputs in High-Z State.....-0.5V to V<sub>CC</sub> + 0.5V
- DC Input Voltage<sup>[20]</sup> .....-0.5V to V<sub>CC</sub> + 0.5V

- Output Current into Outputs (LOW)..... 90 mA
- Static Discharge Voltage..... > 2000V
- Latch-up Current..... > 200 mA

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	1.8V ± 100 mV 2.5V ± 100 mV 3.0V ± 300 mV
Industrial	-40°C to +85°C	1.8V ± 100 mV 2.5V ± 100 mV 3.0V ± 300 mV

**Electrical Characteristics for V<sub>CC</sub> = 1.8V** Over the Operating Range

Parameter	Description			CYDM256B16, CYDM128B16, CYDM064B16			CYDM256B16, CYDM128B16, CYDM064B16			Unit
		P1 I/O Voltage	P2 I/O Voltage	-40			-55			
				Min.	Typ.	Max.	Min.	Typ.	Max.	
V <sub>OH</sub>	Output HIGH Voltage (I <sub>OH</sub> = -100 μA)	1.8V (any port)		V <sub>DDIO</sub> - 0.2			V <sub>DDIO</sub> - 0.2			V
	Output HIGH Voltage (I <sub>OH</sub> = -2 mA)	2.5V (any port)		2.0			2.0			V
	Output HIGH Voltage (I <sub>OH</sub> = -2 mA)	3.0V (any port)		2.1			2.1			V
V <sub>OL</sub>	Output LOW Voltage (I <sub>OL</sub> = 100 μA)	1.8V (any port)				0.2			0.2	V
	Output HIGH Voltage (I <sub>OL</sub> = 2 mA)	2.5V (any port)				0.4			0.4	V
	Output HIGH Voltage (I <sub>OL</sub> = 2 mA)	3.0V (any port)				0.4			0.4	V
V <sub>OL ODR</sub>	ODR Output LOW Voltage (I <sub>OL</sub> = 8 mA)	1.8V (any port)				0.2			0.2	V
		2.5V (any port)				0.2			0.2	V
		3.0V (any port)				0.2			0.2	V
V <sub>IH</sub>	Input HIGH Voltage	1.8V (any port)		1.2		V <sub>DDIO</sub> + 0.2	1.2		V <sub>DDIO</sub> + 0.2	V
		2.5V (any port)		1.7		V <sub>DDIO</sub> + 0.3	1.7		V <sub>DDIO</sub> + 0.3	V
		3.0V (any port)		2.0		V <sub>DDIO</sub> + 0.2	2.0		V <sub>DDIO</sub> + 0.2	V
V <sub>IL</sub>	Input LOW Voltage	1.8V (any port)		-0.2		0.4	-0.2		0.4	V
		2.5V (any port)		-0.3		0.6	-0.3		0.6	V
		3.0V (any port)		-0.2		0.7	-0.2		0.7	V
I <sub>OZ</sub>	Output Leakage Current	1.8V	1.8V	-1		1	-1		1	μA
		2.5V	2.5V	-1		1	-1		1	μA
		3.0V	3.0V	-1		1	-1		1	μA
I <sub>CEX ODR</sub>	ODR Output Leakage Current. V <sub>OUT</sub> = V <sub>DDIO</sub>	1.8V	1.8V	-1		1	-1		1	μA
		2.5V	2.5V	-1		1	-1		1	μA
		3.0V	3.0V	-1		1	-1		1	μA

**Notes:**

- 19. The voltage on any input or I/O pin can not exceed the power pin during power-up.
- 20. Pulse width < 20 ns.



**Electrical Characteristics for  $V_{CC} = 1.8V$**  (continued) Over the Operating Range

Parameter	Description		CYDM256B16, CYDM128B16, CYDM064B16			CYDM256B16, CYDM128B16, CYDM064B16			Unit		
			P1 I/O Voltage	P2 I/O Voltage	-40			-55			
					Min.	Typ.	Max.	Min.		Typ.	Max.
$I_{IX}$	Input Leakage Current		1.8V	1.8V	-1		1	-1		1	$\mu A$
			2.5V	2.5V	-1		1	-1		1	$\mu A$
			3.0V	3.0V	-1		1	-1		1	$\mu A$
$I_{CC}$	Operating Current ( $V_{CC} = \text{Max.}$ , $I_{OUT} = 0 \text{ mA}$ ) Outputs Disabled	Ind.	1.8V	1.8V		25	40		15	25	mA
$I_{SB1}$	Standby Current (Both Ports TTL Level) $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC} - 0.2$ , $SEM_L = SEM_R = V_{CC} - 0.2$ , $f = f_{MAX}$	Ind.	1.8V	1.8V		2	6		2	6	$\mu A$
$I_{SB2}$	Standby Current (One Port TTL Level) $\overline{CE}_L$   $\overline{CE}_R \geq V_{IH}$ , $f = f_{MAX}$	Ind.	1.8V	1.8V		8.5	18		8.5	14	mA
$I_{SB3}$	Standby Current (Both Ports CMOS Level) $\overline{CE}_L$ & $\overline{CE}_R \geq$ $V_{CC} - 0.2V$ , $SEM_L$ and $SEM_R >$ $V_{CC} - 0.2V$ , $f = 0$	Ind.	1.8V	1.8V		2	6		2	6	$\mu A$
$I_{SB4}$	Standby Current (One Port CMOS Level) $\overline{CE}_L$   $\overline{CE}_R \geq V_{IH}$ , $f = f_{MAX}$ <sup>[21]</sup>	Ind.	1.8V	1.8V		8.5	18		8.5	14	mA

**Notes:**

21.  $f_{MAX} = 1/t_{RC}$  = All inputs cycling at  $f = 1/t_{RC}$  (except output enable).  $f = 0$  means no address or control lines change. This applies only to inputs at CMOS level standby  $I_{SB3}$ .

**Electrical Characteristics for  $V_{CC} = 2.5V$  Over the Operating Range**

Parameter	Description			CYDM256B16, CYDM128B16, CYDM064B16			CYDM256B16, CYDM128B16, CYDM064B16			Unit	
		P1 I/O Voltage	P2 I/O Voltage	-40			-55				
				Min.	Typ.	Max.	Min.	Typ.	Max.		
V <sub>OH</sub>	Output HIGH Voltage ( $I_{OH} = -2$ mA)	2.5V (any port)		2.0			2.0			V	
		3.0V (any port)		2.1			2.1			V	
V <sub>OL</sub>	Output LOW Voltage ( $I_{OL} = 2$ mA)	2.5V (any port)				0.4			0.4	V	
		3.0V (any port)				0.4			0.4	V	
V <sub>OL ODR</sub>	ODR Output LOW Voltage ( $I_{OL} = 8$ mA)	2.5V (any port)				0.2			0.2	V	
		3.0V (any port)				0.2			0.2	V	
V <sub>IH</sub>	Input HIGH Voltage	2.5V (any port)		1.7		V <sub>DDIO</sub> + 0.3	1.7		V <sub>DDIO</sub> + 0.3	V	
		3.0V (any port)		2.0		V <sub>DDIO</sub> + 0.2	2.0		V <sub>DDIO</sub> + 0.2	V	
V <sub>IL</sub>	Input LOW Voltage	2.5V (any port)		-0.3		0.6	-0.3		0.6	V	
		3.0V (any port)		-0.2		0.7	-0.2		0.7	V	
I <sub>OZ</sub>	Output Leakage Current	2.5V	2.5V	-1		1	-1		1	μA	
		3.0V	3.0V	-1		1	-1		1	μA	
I <sub>CEX ODR</sub>	ODR Output Leakage Current. V <sub>OUT</sub> = V <sub>CC</sub>	2.5V	2.5V	-1		1	-1		1	μA	
		3.0V	3.0V	-1		1	-1		1	μA	
I <sub>IX</sub>	Input Leakage Current	2.5V	2.5V	-1		1	-1		1	μA	
		3.0V	3.0V	-1		1	-1		1	μA	
I <sub>CC</sub>	Operating Current ( $V_{CC} = \text{Max.}$ , $I_{OUT} = 0$ mA) Outputs Disabled	Ind.	2.5V	2.5V		39	55		28	40	mA
I <sub>SB1</sub>	Standby Current (Both Ports TTL Level) $CE_L$ and $CE_R \geq V_{CC} - 0.2$ , $SEM_L = SEM_R = V_{CC} - 0.2$ , $f = f_{MAX}$	Ind.	2.5V	2.5V		6	8		6	8	μA
I <sub>SB2</sub>	Standby Current (One Port TTL Level) $CE_L$   $CE_R \geq V_{IH}$ , $f = f_{MAX}$	Ind.	2.5V	2.5V		21	30		18	25	mA
I <sub>SB3</sub>	Standby Current (Both Ports CMOS Level) $CE_L$ & $CE_R \geq$ $V_{CC} - 0.2V$ , $SEM_L$ and $SEM_R >$ $V_{CC} - 0.2V$ , $f = 0$	Ind.	2.5V	2.5V		4	6		4	6	μA
I <sub>SB4</sub>	Standby Current (One Port CMOS Level) $CE_L$   $CE_R \geq V_{IH}$ , $f = f_{MAX}$ <sup>[21]</sup>	Ind.	2.5V	2.5V		21	30		18	25	mA

**Electrical Characteristics for 3.0V** Over the Operating Range

Parameter	Description			CYDM256B16, CYDM128B16, CYDM064B16			CYDM256B16, CYDM128B16, CYDM064B16			Unit	
		P1 I/O Voltage	P2 I/O Voltage	-40			-55				
				Min.	Typ.	Max.	Min.	Typ.	Max.		
V <sub>OH</sub>	Output HIGH Voltage (I <sub>OH</sub> = -2 mA)	3.0V (any port)		2.1			2.1			V	
V <sub>OL</sub>	Output LOW Voltage (I <sub>OL</sub> = 2 mA)	3.0V (any port)				0.4			0.4	V	
V <sub>OL ODR</sub>	ODR Output LOW Voltage (I <sub>OL</sub> = 8 mA)	3.0V (any port)				0.2			0.2	V	
V <sub>IH</sub>	Input HIGH Voltage	3.0V (any port)		2.0		V <sub>DDIO</sub> + 0.2	2.0		V <sub>DDIO</sub> + 0.2	V	
V <sub>IL</sub>	Input LOW Voltage	3.0V (any port)		-0.2		0.7	-0.2		0.7	V	
I <sub>OZ</sub>	Output Leakage Current	3.0V	3.0V	-1		1	-1		1	μA	
I <sub>CEX ODR</sub>	ODR Output Leakage Current. V <sub>OUT</sub> = V <sub>CC</sub>	3.0V	3.0V	-1		1	-1		1	μA	
I <sub>IX</sub>	Input Leakage Current	3.0V	3.0V	-1		1	-1		1	μA	
I <sub>CC</sub>	Operating Current (V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA) Outputs Disabled	Ind.	3.0V	3.0V		49	70		42	60	mA
I <sub>SB1</sub>	Standby Current (Both Ports TTL Level) CE <sub>L</sub> and CE <sub>R</sub> ≥ V <sub>CC</sub> - 0.2, SEM <sub>L</sub> = SEM <sub>R</sub> = V <sub>CC</sub> - 0.2, f = f <sub>MAX</sub>	Ind.	3.0V	3.0V		7	10		7	10	μA
I <sub>SB2</sub>	Standby Current (One Port TTL Level) CE <sub>L</sub>   CE <sub>R</sub> ≥ V <sub>IH</sub> , f = f <sub>MAX</sub>	Ind.	3.0V	3.0V		28	40		25	35	mA
I <sub>SB3</sub>	Standby Current (Both Ports CMOS Level) CE <sub>L</sub> & CE <sub>R</sub> ≥ V <sub>CC</sub> - 0.2V, SEM <sub>L</sub> and SEM <sub>R</sub> > V <sub>CC</sub> - 0.2V, f = 0	Ind.	3.0V	3.0V		6	8		6	8	μA
I <sub>SB4</sub>	Standby Current (One Port CMOS Level) CE <sub>L</sub>   CE <sub>R</sub> ≥ V <sub>IH</sub> , f = f <sub>MAX</sub> <sup>[21]</sup>	Ind.	3.0V	3.0V		28	40		25	35	mA

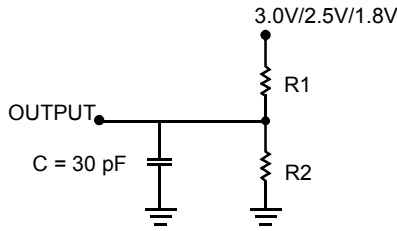
**Capacitance<sup>[22]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 3.0V	9	pF
C <sub>OUT</sub>	Output Capacitance		10	pF

**Note:**

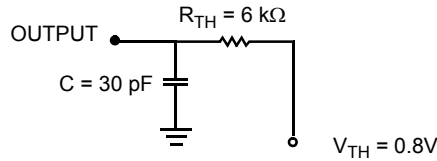
22. Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms



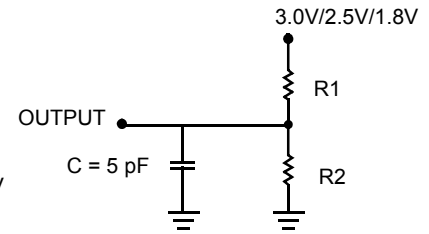
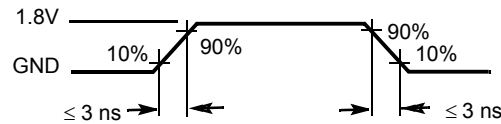
(a) Normal Load

	3.0V/2.5V	1.8V
R1	1022Ω	13500Ω
R2	792Ω	10800Ω



(b) Thévenin Equivalent (Load 1)

ALL INPUT PULSES



(c) Three-State Delay (Load 2)

(Used for  $t_{LZ}$ ,  $t_{HZ}$ ,  $t_{HZWE}$ , and  $t_{LZWE}$  including scope and jig)

## Switching Characteristics for $V_{CC} = 1.8V$ Over the Operating Range<sup>[23]</sup>

Parameter	Description	CYDM256B16, CYDM128B16, CYDM064B16		CYDM256B16, CYDM128B16, CYDM064B16		Unit
		-40		-55		
		Min.	Max.	Min.	Max.	
<b>Read Cycle</b>						
$t_{RC}$	Read Cycle Time	40		55		ns
$t_{AA}$	Address to Data Valid		40		55	ns
$t_{OHA}$	Output Hold From Address Change	5		5		ns
$t_{ACE}^{[24]}$	$\overline{CE}$ LOW to Data Valid		40		55	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		25		30	ns
$t_{LZOE}^{[25, 26, 27]}$	$\overline{OE}$ Low to Low Z	5		5		ns
$t_{HZOE}^{[25, 26, 27]}$	$\overline{OE}$ HIGH to High Z		15		25	ns
$t_{LZCE}^{[25, 26, 27]}$	$\overline{CE}$ LOW to Low Z	5		5		ns
$t_{HZCE}^{[25, 26, 27]}$	$\overline{CE}$ HIGH to High Z		15		25	ns
$t_{PU}^{[27]}$	$\overline{CE}$ LOW to Power-Up	0		0		ns
$t_{PD}^{[27]}$	$\overline{CE}$ HIGH to Power-Down		40		55	ns
$t_{ABE}^{[24]}$	Byte Enable Access Time		40		55	ns
<b>Write Cycle</b>						
$t_{WC}$	Write Cycle Time	40		55		ns
$t_{SCE}^{[24]}$	$\overline{CE}$ LOW to Write End	30		45		ns
$t_{AW}$	Address Valid to Write End	30		45		ns
$t_{HA}$	Address Hold From Write End	0		0		ns

### Notes:

23. Test conditions assume signal transition time of 3 ns or less, timing reference levels of  $V_{CC}/2$ , input pulse levels of 0 to  $V_{CC}$ , and output loading of the specified  $I_{OH}/I_{OH}$  and 30-pF load capacitance.

24. To access RAM,  $\overline{CE} = L$ ,  $UB = L$ ,  $SEM = H$ . To access semaphore,  $\overline{CE} = H$  and  $SEM = L$ . Either condition must be valid for the entire  $t_{SCE}$  time.

25. At any given temperature and voltage condition for any given device,  $t_{HZCE}$  is less than  $t_{LZCE}$  and  $t_{HZOE}$  is less than  $t_{LZOE}$ .

26. Test conditions used are Load 3.

27. This parameter is guaranteed but not tested. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Read Timing with Busy waveform

**Switching Characteristics for  $V_{CC} = 1.8V$  Over the Operating Range<sup>[23]</sup> (continued)**

Parameter	Description	CYDM256B16, CYDM128B16, CYDM064B16		CYDM256B16, CYDM128B16, CYDM064B16		Unit
		-40		-55		
		Min.	Max.	Min.	Max.	
$t_{SA}^{[24]}$	Address Set-up to Write Start	0		0		ns
$t_{PWE}$	Write Pulse Width	25		40		ns
$t_{SD}$	Data Set-up to Write End	20		30		ns
$t_{HD}$	Data Hold From Write End	0		0		ns
$t_{HZWE}^{[26, 27]}$	R/W LOW to High Z		15		25	ns
$t_{LZWE}^{[26, 27]}$	R/W HIGH to Low Z	0		0		ns
$t_{WDD}^{[28]}$	Write Pulse to Data Delay		55		80	ns
$t_{DDD}^{[28]}$	Write Data Valid to Read Data Valid		55		80	ns
<b>Busy Timing<sup>[29]</sup></b>						
$t_{BLA}$	BUSY LOW from Address Match		30		45	ns
$t_{BHA}$	BUSY HIGH from Address Mismatch		30		45	ns
$t_{BLC}$	BUSY LOW from $\overline{CE}$ LOW		30		45	ns
$t_{BHC}$	BUSY HIGH from $\overline{CE}$ HIGH		30		45	ns
$t_{PS}^{[30]}$	Port Set-up for Priority	5		5		ns
$t_{WB}$	R/W HIGH after BUSY (Slave)	0		0		ns
$t_{WH}$	R/W HIGH after BUSY HIGH (Slave)	20		35		ns
$t_{BDD}^{[31]}$	BUSY HIGH to Data Valid		30		40	ns
<b>Interrupt Timing<sup>[29]</sup></b>						
$t_{INS}$	INT Set Time		35		45	ns
$t_{INR}$	INT Reset Time		35		45	ns
<b>Semaphore Timing</b>						
$t_{SOP}$	SEM Flag Update Pulse ( $\overline{OE}$ or $\overline{SEM}$ )	10		15		ns
$t_{SWRD}$	SEM Flag Write to Read Time	10		10		ns
$t_{SPS}$	SEM Flag Contention Window	10		10		ns
$t_{SAA}$	SEM Address Access Time		40		55	ns

**Notes:**

28. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Read Timing with Busy waveform.

29. Test conditions used are Load 2.

30. Add 2ns to this parameter if  $V_{CC}$  and  $V_{DDIOR}$  are  $<1.8V$ , and  $V_{DDIOL}$  is  $>2.5V$  at temperature  $<0^{\circ}C$ .

31.  $t_{BDD}$  is a calculated parameter and is the greater of  $t_{WDD} - t_{PWE}$  (actual) or  $t_{DDD} - t_{SD}$  (actual).

**Switching Characteristics for  $V_{CC} = 2.5V$  Over the Operating Range**

Parameter	Description	CYDM256B16, CYDM128B16, CYDM064B16		CYDM256B16, CYDM128B16, CYDM064B16		Unit
		-40		-55		
		Min.	Max.	Min.	Max.	
<b>Read Cycle</b>						
$t_{RC}$	Read Cycle Time	40		55		ns
$t_{AA}$	Address to Data Valid		40		55	ns
$t_{OHA}$	Output Hold From Address Change	5		5		ns
$t_{ACE}^{[24]}$	$\overline{CE}$ LOW to Data Valid		40		55	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		25		30	ns
$t_{LZOE}^{[25, 26, 27]}$	$\overline{OE}$ Low to Low Z	2		2		ns
$t_{HZOE}^{[25, 26, 27]}$	$\overline{OE}$ HIGH to High Z		15		25	ns
$t_{LZCE}^{[25, 26, 27]}$	$\overline{CE}$ LOW to Low Z	2		2		ns
$t_{HZCE}^{[25, 26, 27]}$	$\overline{CE}$ HIGH to High Z		15		25	ns
$t_{PU}^{[27]}$	$\overline{CE}$ LOW to Power-Up	0		0		ns
$t_{PD}^{[27]}$	$\overline{CE}$ HIGH to Power-Down		40		55	ns
$t_{ABE}^{[24]}$	Byte Enable Access Time		40		55	ns
<b>Write Cycle</b>						
$t_{WC}$	Write Cycle Time	40		55		ns
$t_{SCE}^{[24]}$	$\overline{CE}$ LOW to Write End	30		45		ns
$t_{AW}$	Address Valid to Write End	30		45		ns
$t_{HA}$	Address Hold From Write End	0		0		ns
$t_{SA}^{[24]}$	Address Set-up to Write Start	0		0		ns
$t_{PWE}$	Write Pulse Width	25		40		ns
$t_{SD}$	Data Set-up to Write End	20		30		ns
$t_{HD}$	Data Hold From Write End	0		0		ns
$t_{HZWE}^{[26, 27]}$	R/W LOW to High Z		15		25	ns
$t_{LZWE}^{[26, 27]}$	R/W HIGH to Low Z	0		0		ns
$t_{WDD}^{[28]}$	Write Pulse to Data Delay		55		80	ns
$t_{DDD}^{[28]}$	Write Data Valid to Read Data Valid		55		80	ns
<b>Busy Timing<sup>[29]</sup></b>						
$t_{BLA}$	$\overline{BUSY}$ LOW from Address Match		30		45	ns
$t_{BHA}$	$\overline{BUSY}$ HIGH from Address Mismatch		30		45	ns
$t_{BLC}$	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		30		45	ns
$t_{BHC}$	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH		30		45	ns
$t_{PS}^{[30]}$	Port Set-up for Priority	5		5		ns
$t_{WB}$	R/W HIGH after $\overline{BUSY}$ (Slave)	0		0		ns
$t_{WH}$	R/W HIGH after $\overline{BUSY}$ HIGH (Slave)	20		35		ns
$t_{BDD}^{[31]}$	$\overline{BUSY}$ HIGH to Data Valid		30		40	ns
<b>Interrupt Timing<sup>[29]</sup></b>						
$t_{INS}$	$\overline{INT}$ Set Time		35		45	ns
$t_{INR}$	$\overline{INT}$ Reset Time		35		45	ns

**Switching Characteristics for  $V_{CC} = 2.5V$  Over the Operating Range (continued)**

Parameter	Description	CYDM256B16, CYDM128B16, CYDM064B16		CYDM256B16, CYDM128B16, CYDM064B16		Unit
		-40		-55		
		Min.	Max.	Min.	Max.	
<b>Semaphore Timing</b>						
$t_{SOP}$	SEM Flag Update Pulse ( $\overline{OE}$ or $\overline{SEM}$ )	10		15		ns
$t_{SWRD}$	SEM Flag Write to Read Time	10		10		ns
$t_{SPS}$	SEM Flag Contention Window	10		10		ns
$t_{SAA}$	SEM Address Access Time		40		55	ns

**Switching Characteristics for  $V_{CC} = 3.0V$  Over the Operating Range**

Parameter	Description	CYDM256B16, CYDM128B16, CYDM064B16		CYDM256B16, CYDM128B16, CYDM064B16		Unit
		-40		-55		
		Min.	Max.	Min.	Max.	
<b>Read Cycle</b>						
$t_{RC}$	Read Cycle Time	40		55		ns
$t_{AA}$	Address to Data Valid		40		55	ns
$t_{OHA}$	Output Hold From Address Change	5		5		ns
$t_{ACE}^{[24]}$	$\overline{CE}$ LOW to Data Valid		40		55	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		25		30	ns
$t_{LZOE}^{[25, 26, 27]}$	$\overline{OE}$ Low to Low Z	1		1		ns
$t_{HZOE}^{[25, 26, 27]}$	$\overline{OE}$ HIGH to High Z		15		25	ns
$t_{LZCE}^{[25, 26, 27]}$	$\overline{CE}$ LOW to Low Z	1		1		ns
$t_{HZCE}^{[25, 26, 27]}$	$\overline{CE}$ HIGH to High Z		15		25	ns
$t_{PU}^{[27]}$	$\overline{CE}$ LOW to Power-Up	0		0		ns
$t_{PD}^{[27]}$	$\overline{CE}$ HIGH to Power-Down		40		55	ns
$t_{ABE}^{[24]}$	Byte Enable Access Time		40		55	ns
<b>Write Cycle</b>						
$t_{WC}$	Write Cycle Time	40		55		ns
$t_{SCE}^{[24]}$	$\overline{CE}$ LOW to Write End	30		45		ns
$t_{AW}$	Address Valid to Write End	30		45		ns
$t_{HA}$	Address Hold From Write End	0		0		ns
$t_{SA}^{[24]}$	Address Set-up to Write Start	0		0		ns
$t_{PWE}$	Write Pulse Width	25		40		ns
$t_{SD}$	Data Set-up to Write End	20		30		ns
$t_{HD}$	Data Hold From Write End	0		0		ns
$t_{HZWE}^{[26, 27]}$	$R/\overline{W}$ LOW to High Z		15		25	ns
$t_{LZWE}^{[26, 27]}$	$R/\overline{W}$ HIGH to Low Z	0		0		ns
$t_{WDD}^{[28]}$	Write Pulse to Data Delay		55		80	ns
$t_{DDD}^{[28]}$	Write Data Valid to Read Data Valid		55		80	ns



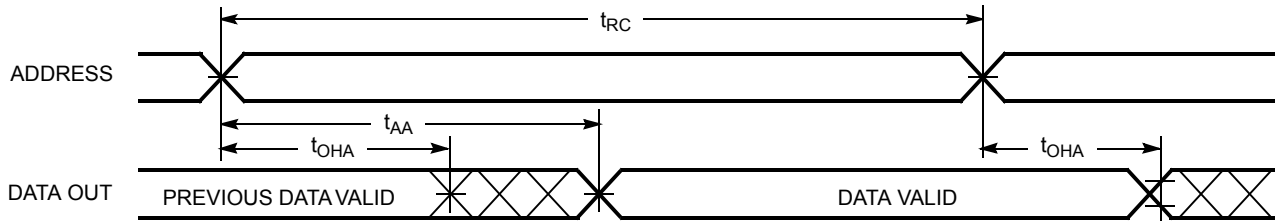
**Switching Characteristics for  $V_{CC} = 3.0V$  Over the Operating Range (continued)**

Parameter	Description	CYDM256B16, CYDM128B16, CYDM064B16		CYDM256B16, CYDM128B16, CYDM064B16		Unit
		-40		-55		
		Min.	Max.	Min.	Max.	
<b>Busy Timing<sup>[29]</sup></b>						
$t_{BLA}$	$\overline{BUSY}$ LOW from Address Match		30		45	ns
$t_{BHA}$	$\overline{BUSY}$ HIGH from Address Mismatch		30		45	ns
$t_{BLC}$	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		30		45	ns
$t_{BHC}$	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH		30		45	ns
$t_{PS}^{[30]}$	Port Set-up for Priority	5		5		ns
$t_{WB}$	$R/\overline{W}$ HIGH after $\overline{BUSY}$ (Slave)	0		0		ns
$t_{WH}$	$R/\overline{W}$ HIGH after $\overline{BUSY}$ HIGH (Slave)	20		35		ns
$t_{BDD}^{[31]}$	$\overline{BUSY}$ HIGH to Data Valid		30		40	ns
<b>Interrupt Timing<sup>[29]</sup></b>						
$t_{INS}$	$\overline{INT}$ Set Time		35		45	ns
$t_{INR}$	$\overline{INT}$ Reset Time		35		45	ns
<b>Semaphore Timing</b>						
$t_{SOP}$	SEM Flag Update Pulse ( $\overline{OE}$ or $\overline{SEM}$ )	10		15		ns
$t_{SWRD}$	SEM Flag Write to Read Time	10		10		ns
$t_{SPS}$	SEM Flag Contention Window	10		10		ns
$t_{SAA}$	SEM Address Access Time		40		55	ns

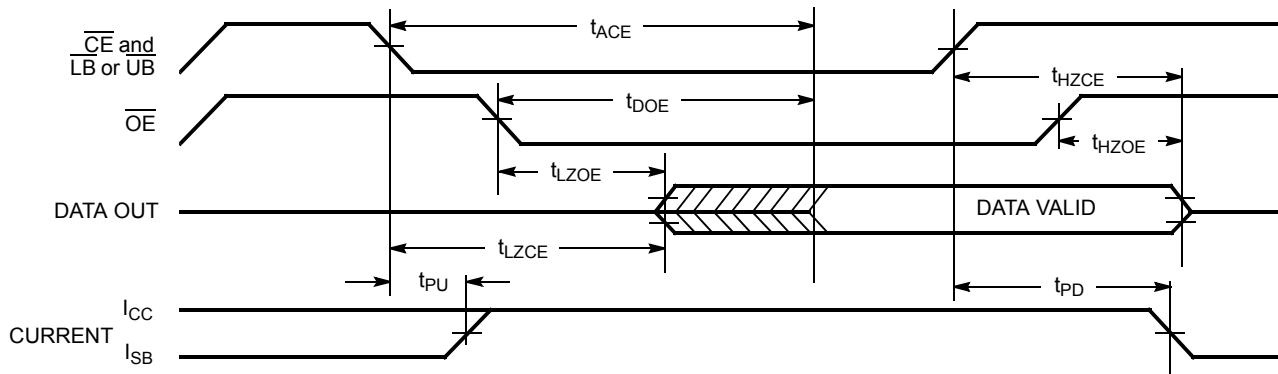


## Switching Waveforms

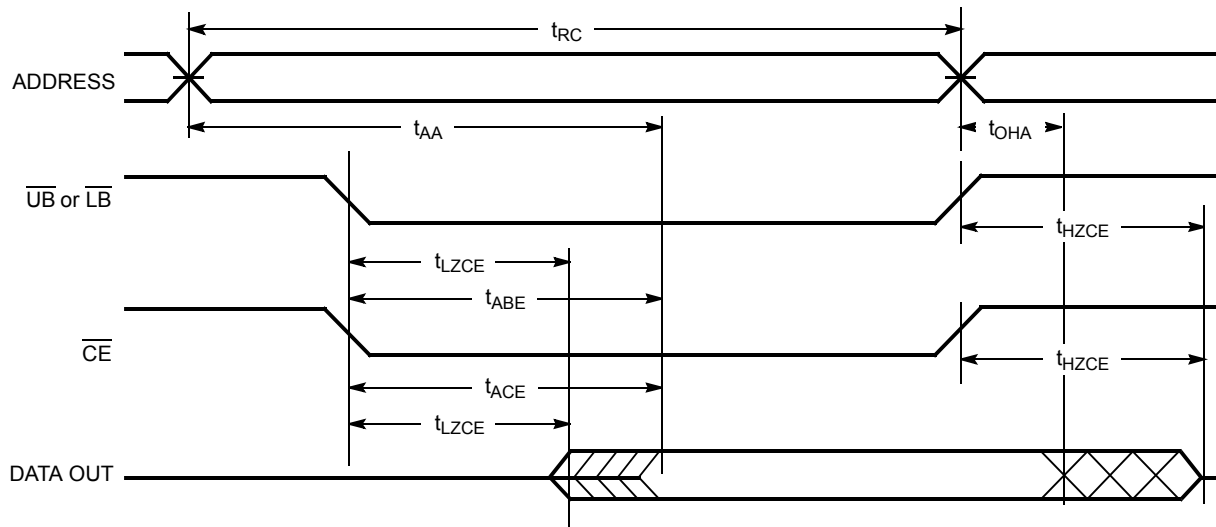
### Read Cycle No.1 (Either Port Address Access)<sup>[32, 33, 34]</sup>



### Read Cycle No.2 (Either Port $\overline{\text{CE}}/\overline{\text{OE}}$ Access)<sup>[32, 35, 36]</sup>



### Read Cycle No. 3 (Either Port)<sup>[32, 34, 37, 38]</sup>

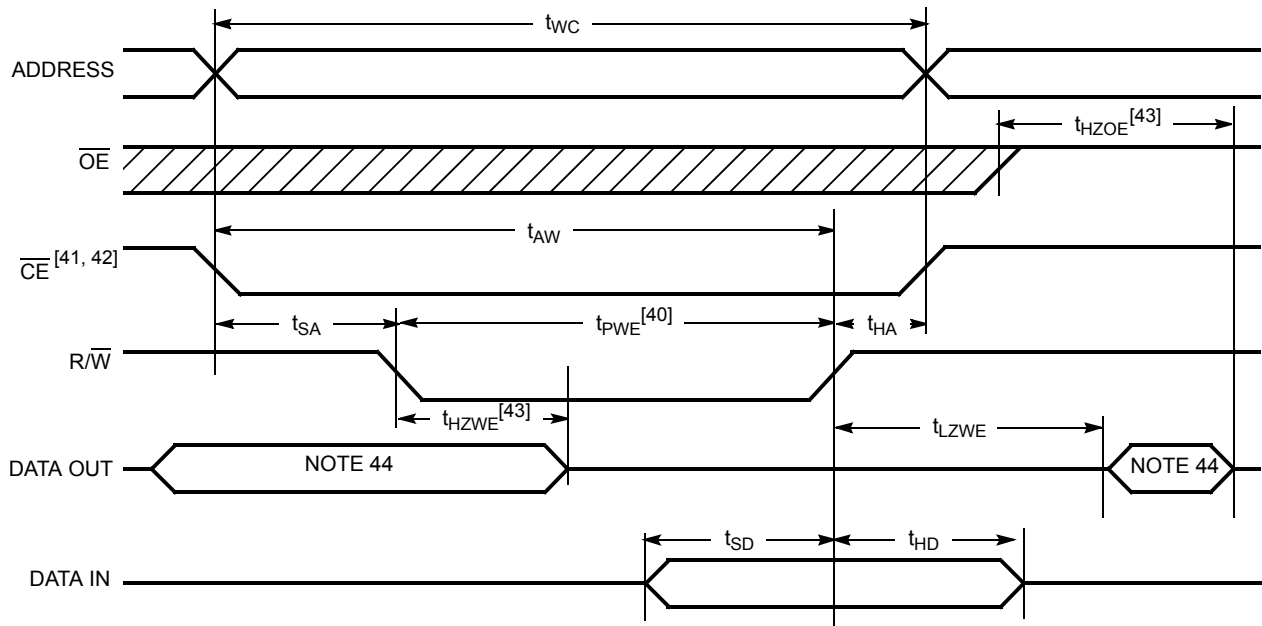


#### Notes:

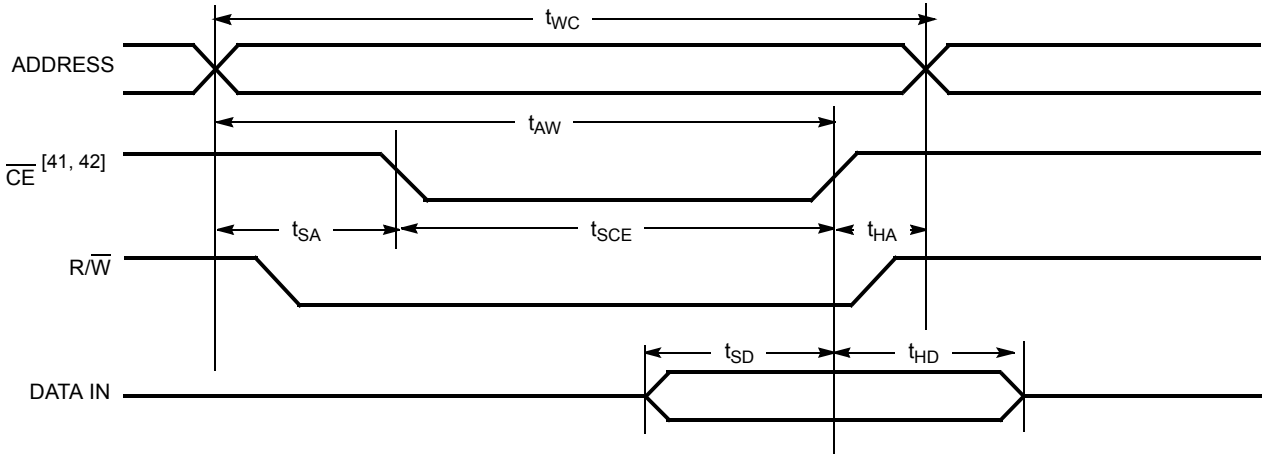
32. R/W is HIGH for read cycles.
33. Device is continuously selected  $\overline{\text{CE}} = V_{\text{IL}}$  and  $\overline{\text{UB}}$  or  $\overline{\text{LB}} = V_{\text{IL}}$ . This waveform cannot be used for semaphore reads.
34.  $\overline{\text{OE}} = V_{\text{IL}}$ .
35. Address valid prior to or coincident with  $\overline{\text{CE}}$  transition LOW.
36. To access RAM,  $\overline{\text{CE}} = V_{\text{IL}}$ ,  $\overline{\text{UB}}$  or  $\overline{\text{LB}} = V_{\text{IL}}$ ,  $\overline{\text{SEM}} = V_{\text{IH}}$ . To access semaphore,  $\overline{\text{CE}} = V_{\text{IH}}$ ,  $\overline{\text{SEM}} = V_{\text{IL}}$ .
37. R/W must be HIGH during all address transitions.
38. A write occurs during the overlap ( $t_{\text{SCE}}$  or  $t_{\text{PWE}}$ ) of a LOW  $\overline{\text{CE}}$  or  $\overline{\text{SEM}}$  and a LOW  $\overline{\text{UB}}$  or  $\overline{\text{LB}}$ .

Switching Waveforms (continued)

Write Cycle No.1: R/W Controlled Timing<sup>[37, 38, 39, 40, 41, 42]</sup>



Write Cycle No. 2: CE Controlled Timing<sup>[37, 38, 39, 44]</sup>

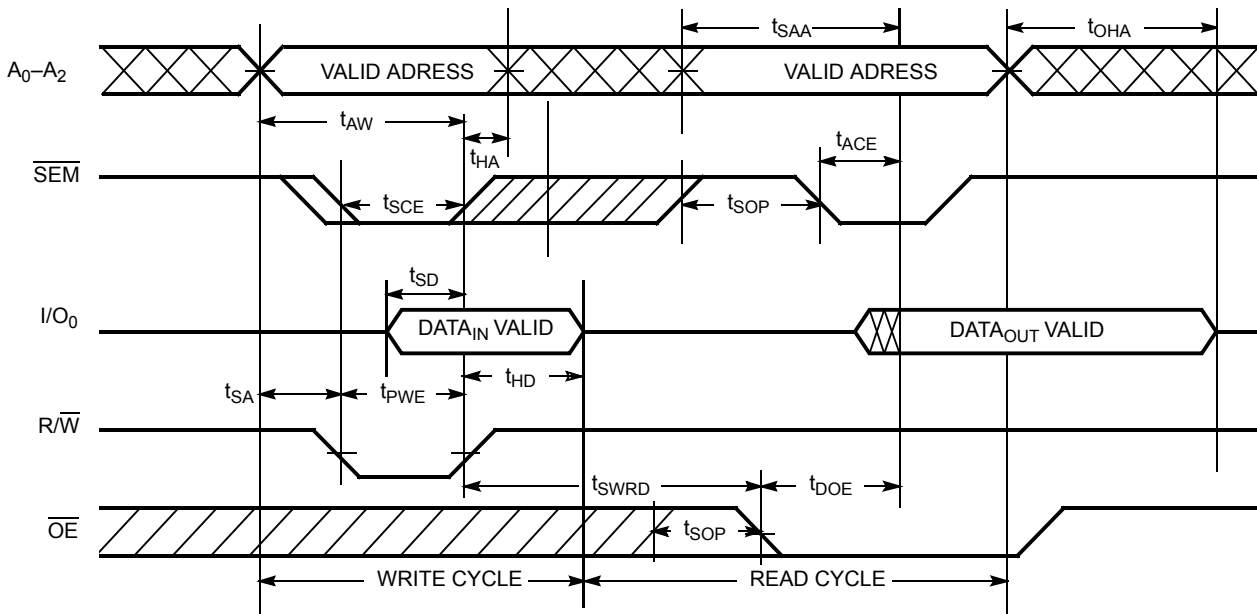


Notes:

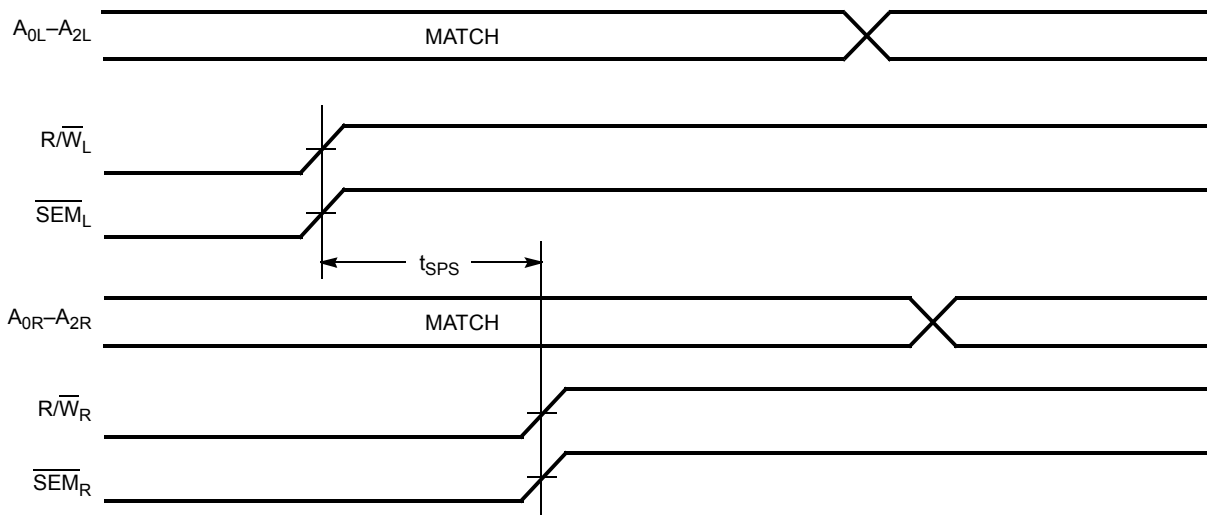
- 39.  $t_{HA}$  is measured from the earlier of  $\overline{CE}$  or  $R/\overline{W}$  or  $(\overline{SEM}$  or  $R/\overline{W})$  going HIGH at the end of write cycle.
- 40. If  $\overline{OE}$  is LOW during a  $R/\overline{W}$  controlled write cycle, the write pulse width must be the larger of  $t_{PWE}$  or  $(t_{HZWE} + t_{SD})$  to allow the I/O drivers to turn off and data to be placed on the bus for the required  $t_{SD}$ . If  $\overline{OE}$  is HIGH during an  $R/\overline{W}$  controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified  $t_{PWE}$ .
- 41. To access RAM,  $\overline{CE} = V_{IL}$ ,  $\overline{SEM} = V_{IH}$ .
- 42. To access upper byte,  $\overline{CE} = V_{IL}$ ,  $\overline{UB} = V_{IL}$ ,  $\overline{SEM} = V_{IH}$ .  
To access lower byte,  $\overline{CE} = V_{IL}$ ,  $\overline{LB} = V_{IL}$ ,  $\overline{SEM} = V_{IH}$ .
- 43. Transition is measured  $\pm 0$  mV from steady state with a 5-pF load (including scope and jig). This parameter is sampled and not 100% tested.
- 44. During this period, the I/O pins are in the output state, and input signals must not be applied.

Switching Waveforms (continued)

Semaphore Read After Write Timing, Either Side<sup>[45, 46]</sup>



Timing Diagram of Semaphore Contention<sup>[47, 48]</sup>

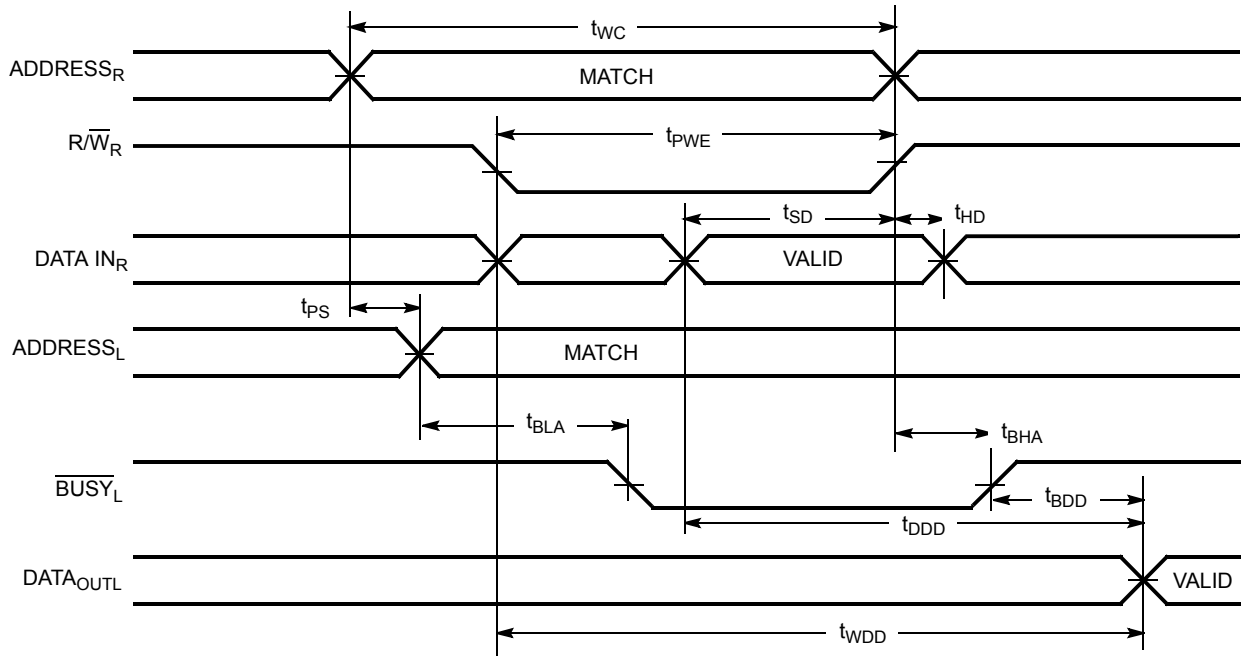


Notes:

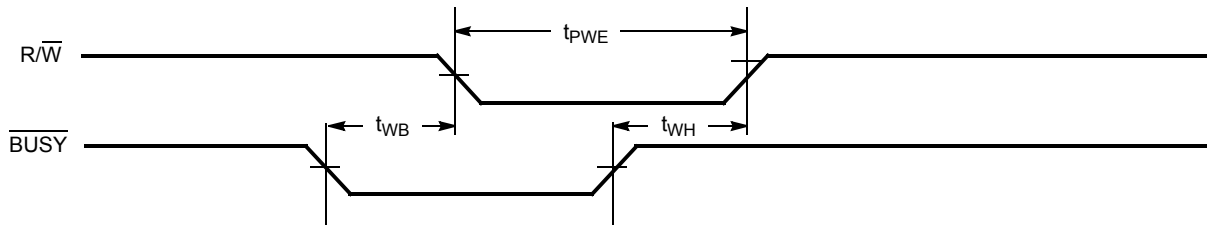
- 45. If the  $\overline{CE}$  or  $\overline{SEM}$  LOW transition occurs simultaneously with or after the  $\overline{R/W}$  LOW transition, the outputs remain in the high-impedance state.
- 46.  $\overline{CE} = \text{HIGH}$  for the duration of the above timing (both write and read cycle).
- 47.  $I/O_{0R} = I/O_{0L} = \text{LOW}$  (request semaphore);  $\overline{CE}_R = \overline{CE}_L = \text{HIGH}$ .
- 48. If t<sub>SPS</sub> is violated, the semaphore will definitely be obtained by one side or the other, but which side will get the semaphore is unpredictable.

Switching Waveforms (continued)

Timing Diagram of Read with  $\overline{\text{BUSY}}$  ( $\overline{\text{M/S}} = \text{HIGH}$ )<sup>[49]</sup>



Write Timing with Busy Input ( $\overline{\text{M/S}} = \text{LOW}$ )

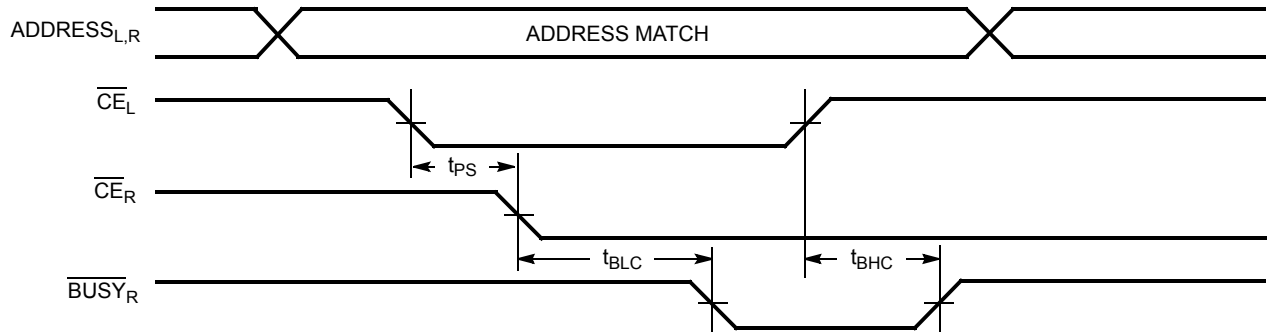


Note:  
49.  $\overline{\text{CE}}_L = \overline{\text{CE}}_R = \text{LOW}$ .

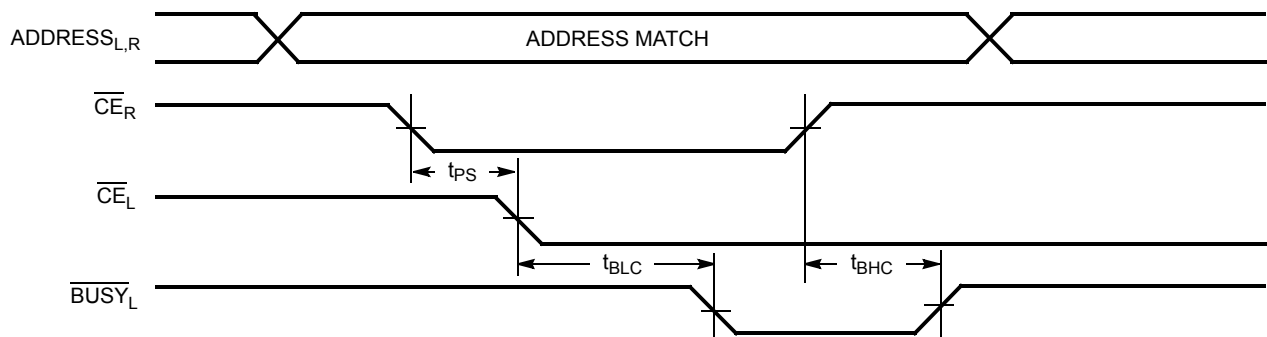
**Switching Waveforms (continued)**

**Busy Timing Diagram No.1 ( $\overline{CE}$  Arbitration)**

**$\overline{CE}_L$  Valid First<sup>[50]</sup>**

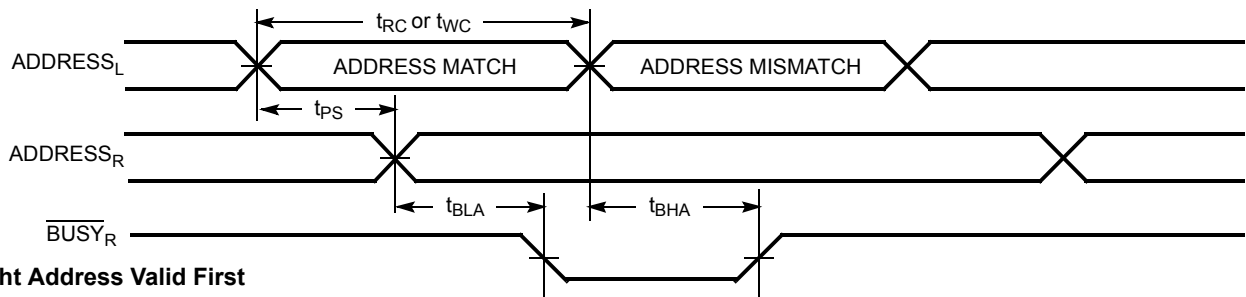


**$\overline{CE}_R$  Valid First**

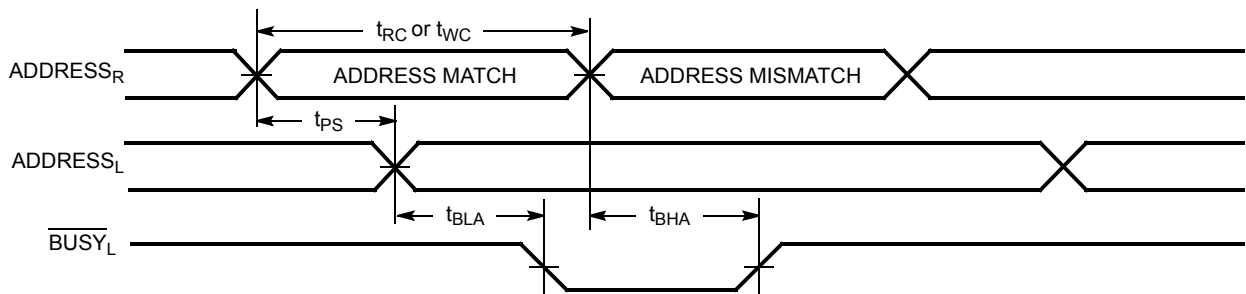


**Busy Timing Diagram No.2 (Address Arbitration)<sup>[50]</sup>**

**Left Address Valid First**



**Right Address Valid First**

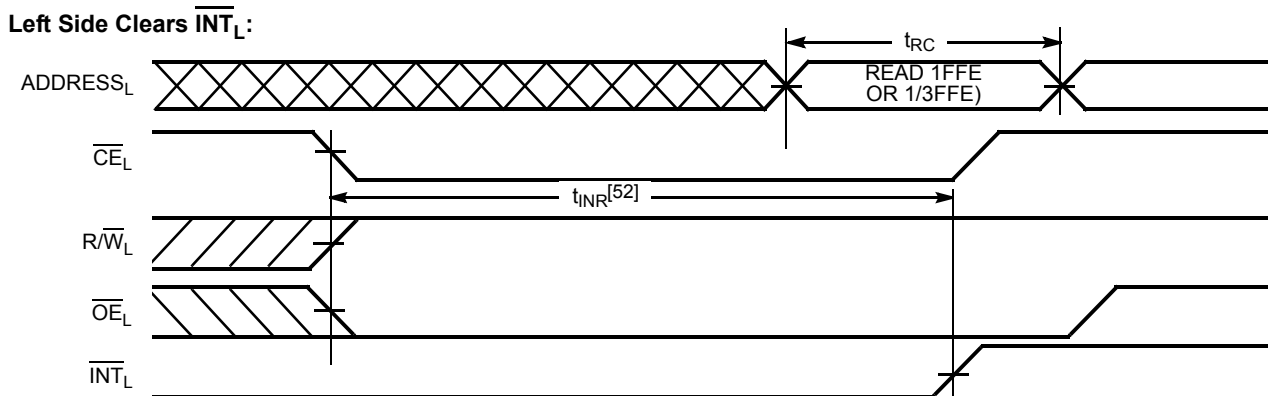
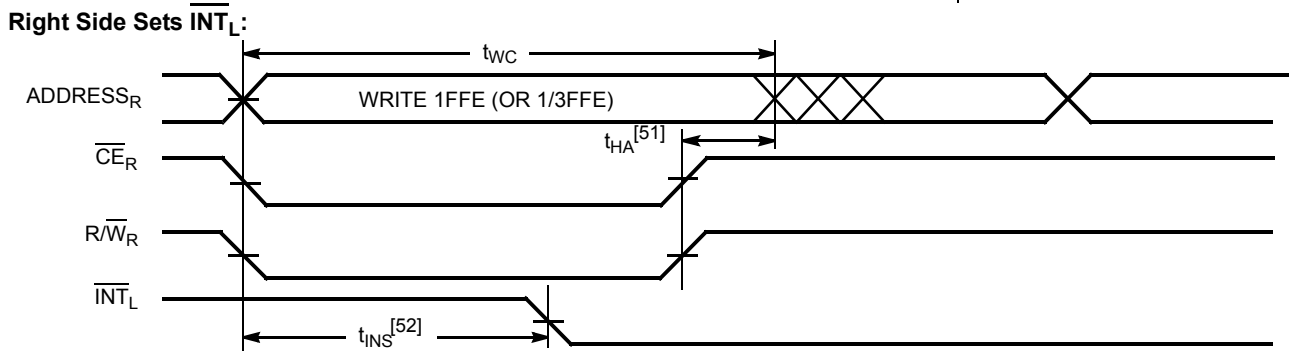
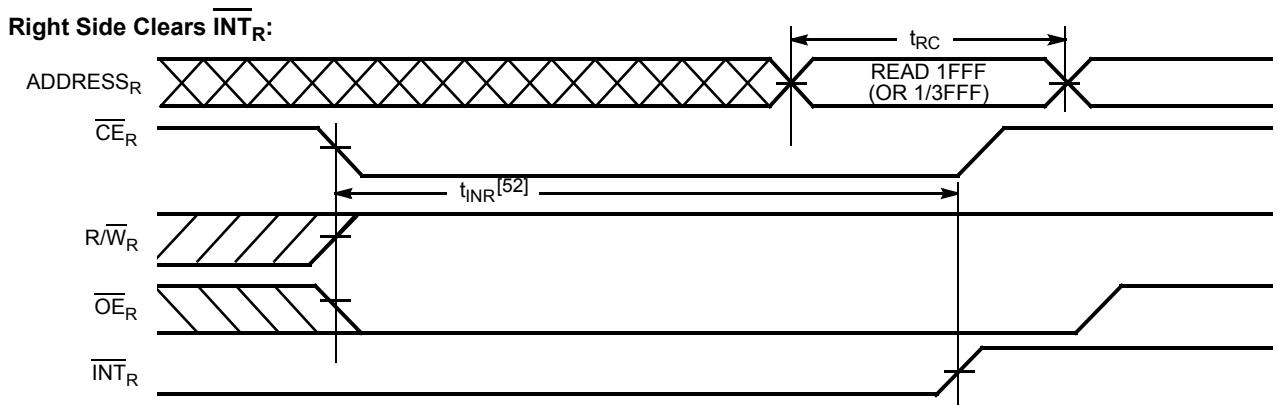
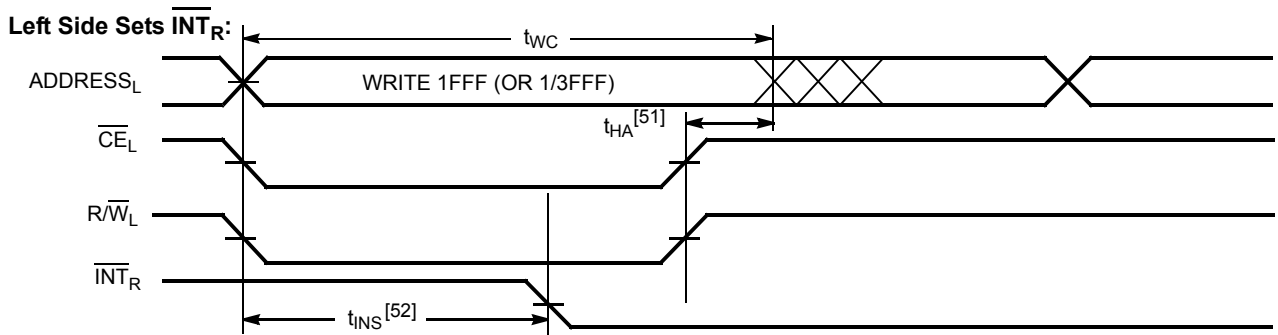


**Note:**

50. If  $t_{PS}$  is violated, the busy signal will be asserted on one side or the other, but there is no guarantee to which side  $\overline{BUSY}$  will be asserted.

Switching Waveforms (continued)

Interrupt Timing Diagrams



Notes:

- 51.  $t_{HA}$  depends on which enable pin ( $\overline{\text{CE}}_L$  or  $\overline{\text{R}}/\overline{\text{W}}_L$ ) is deasserted first.
- 52.  $t_{INS}$  or  $t_{INR}$  depends on which enable pin ( $\overline{\text{CE}}_L$  or  $\overline{\text{R}}/\overline{\text{W}}_L$ ) is asserted last.



**Ordering Information**

**16K x16 1.8V Asynchronous Dual-Port SRAM**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
40	CYDM256B16-40BVXC	BZ100	100-ball Lead-free 0.5-mm Pitch BGA	Commercial
55	CYDM256B16-55BVXC	BZ100	100-ball Lead-free 0.5-mm Pitch BGA	Commercial
55	CYDM256B16-55BVXI	BZ100	100-ball Lead-free 0.5-mm Pitch BGA	Industrial

**8K x16 1.8V Asynchronous Dual-Port SRAM**

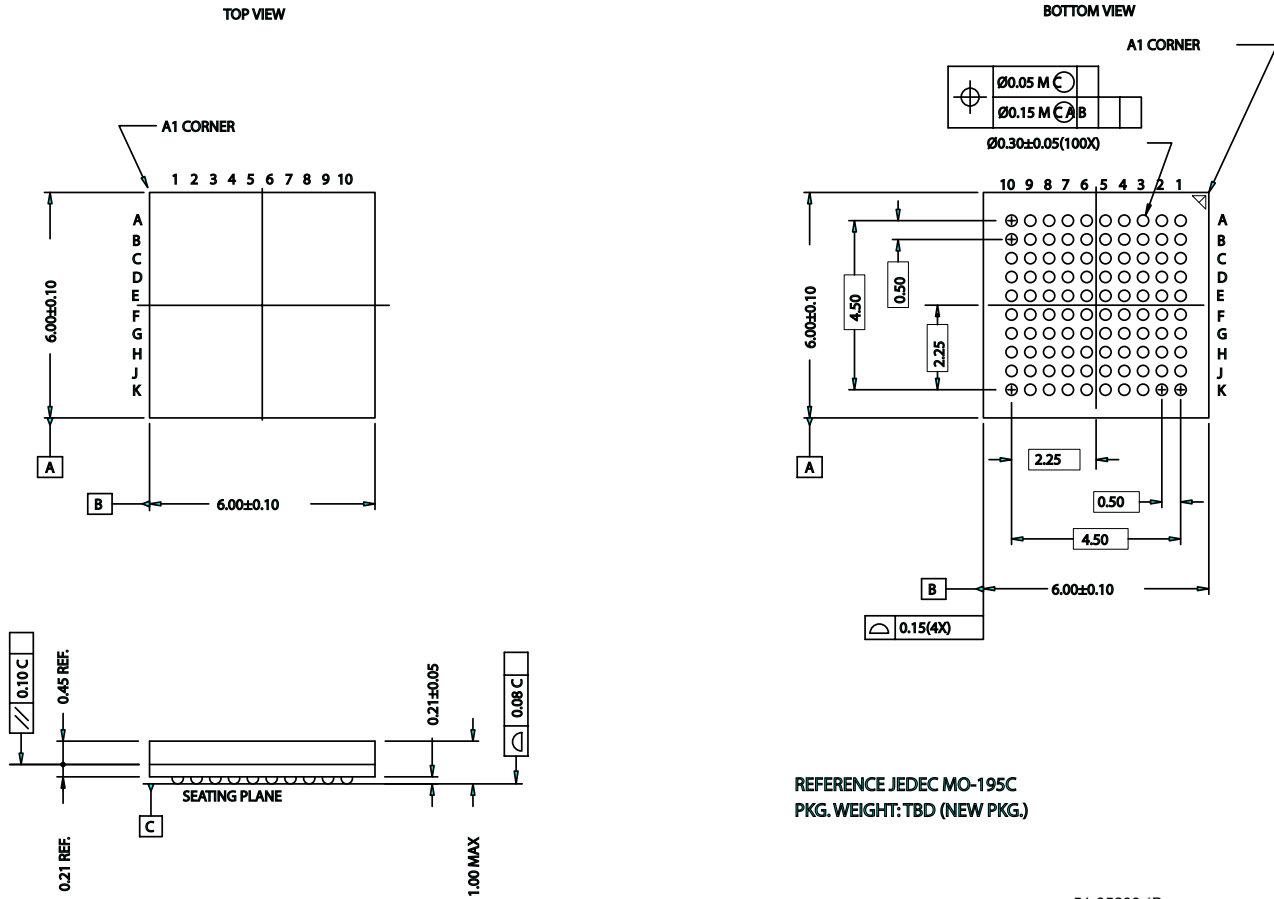
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
40	CYDM128B16-40BVXC	BZ100	100-ball Lead-free 0.5-mm Pitch BGA	Commercial
55	CYDM128B16-55BVXC	BZ100	100-ball Lead-free 0.5-mm Pitch BGA	Commercial
55	CYDM128B16-55BVXI	BZ100	100-ball Lead-free 0.5-mm Pitch BGA	Industrial

**4K x16 1.8V Asynchronous Dual-Port SRAM**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
40	CYDM064B16-40BVXC	BZ100	100-ball Lead-free 0.5-mm Pitch BGA	Commercial
55	CYDM064B16-55BVXC	BZ100	100-ball Lead-free 0.5-mm Pitch BGA	Commercial
55	CYDM064B16-55BVXI	BZ100	100-ball Lead-free 0.5-mm Pitch BGA	Industrial

Package Diagram

100 VFBGA (6 x 6 x 1.0 mm) BZ100A



51-85209-B

MoBL is a registered trademark of Cypress Semiconductor Corporation. All product and company names mentioned in this document are the trademarks of their respective holders.



**Document History Page**

<b>Document Title: CYDM064B16/CYDM128B16/CYDM256B16 1.8V 4K/8K/16K x 16 MOBL (R) Dual-Port Static RAM</b>				
<b>Document Number: 001-00217</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	369423	SEE ECN	YDT	New data sheet
*A	381721	SEE ECN	YDT	Updated 2.5V/3.0V ICC, ISB1, ISB2, ISB4 Updated VOL ODR to 0.2V
*B	396697	SEE ECN	KGH	Updated ISB2 and ISB4 typo to mA. Updated tINS and tINR for -55 to 31ns.
*C	404777	SEE ECN	KGH	Updated I <sub>OH</sub> and I <sub>OL</sub> values for the 1.8V, 2.5V and 3.0V parameters V <sub>OH</sub> and V <sub>OL</sub> Replaced -35 speed bin with -40 Updated Switching Characteristics for V <sub>CC</sub> = 2.5V and V <sub>CC</sub> = 3.0V Included note 35
*D	426637	SEE ECN	KGH	Removed part numbers CYDM128B08 and CYDM064B08
*E	733676	SEE ECN	HKH	Corrected typo for power supply description in pg 4 (3.0V instead of 3.3V) Updated tDDD timing value to be consistent with tWDD