Integrated Device Technology, Inc.

FAST CMOS UP/DOWN BINARY COUNTER

IDT54/74FCT191T/AT

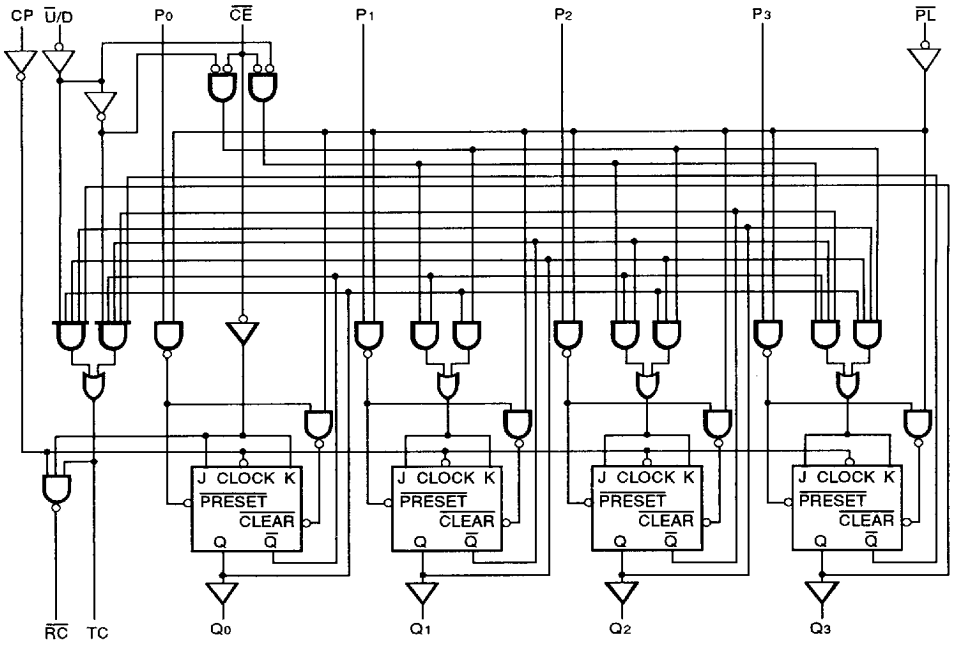
FEATURES:

- Std. and A speed grades
- Low input and output leakage ≤1μA (max.)
- CMOS power levels
- True TTL input and output compatibility
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- High drive outputs (-15mA I_{OH}, 48mA I_{OL})
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, CERPACK and LCC packages

DESCRIPTION:

The IDT54/74FCT191T and IDT54/74FCT191AT are reversible modulo-16 binary counters, featuring synchronous counting and asynchronous presetting and are built using an advanced dual metal CMOS technology. The preset feature allows the IDT54/74FCT191T and IDT54/74FCT191AT to be used in programmable dividers. The count enable input, terminal count output and ripple clock output make possible a variety of methods of implementing multiusage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

FUNCTIONAL BLOCK DIAGRAMS



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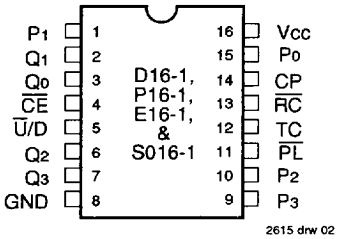
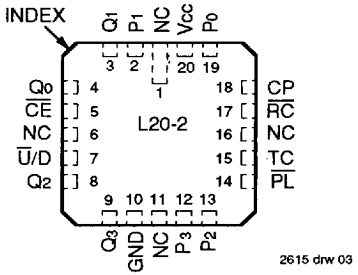
PIN CONFIGURATIONS



DIP/CERPACK/SOIC
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$\overline{CE}$	Count Enable Input (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
P0-3	Parallel Data Inputs
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
U/D	Up/Down Count Control Input
Q0-3	Flip-Flop Outputs
$\overline{RC}$	Ripple Clock Output (Active LOW)
TC	Terminal Count Output (Active HIGH)

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$\overline{RC}$ FUNCTION TABLE(2)

Inputs		Outputs	
$\overline{CE}$	CP	TC(1)	$\overline{RC}$
L	⊓	H	⊓
H	X	X	H
X	X	L	H

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MODE SELECT FUNCTION TABLE(2)

Inputs				Mode
$\overline{PL}$	$\overline{CE}$	U/D	CP	
H	L	L	↑	Count Up
H	L	H	↑	Count Down
L	X	X	X	Preset (Asynchronous)
H	H	X	X	No Change (Hold)

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NOTES:
1. TC is generated internally
2. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care, ↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

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NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

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NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level	COM'L.(5)	2.0	—	—	V
			MIL.	2.7	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current(4)	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current(4)		V_I = 0.5V	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)(4)		V_O = 0.5V	—	—	±1	
I_I	Input HIGH Current(4)	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND(3)		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.01	1	mA

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NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = –55°C.
5. Clock pin requires a minimum V_{IH} of 2.5V.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	µA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open Preset Mode $\overline{PL}$ = $\overline{CE}$ = U/D = CP = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open Preset Mode $\overline{PL}$ = $\overline{CE}$ = U/D = CP = GND One Bit Toggling at fi = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.8	2.3	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.0	3.3	
		V_{CC} = Max., Outputs Open Preset Mode $\overline{PL}$ = $\overline{CE}$ = U/D = CP = GND Four Bits Toggling at fi = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.0	6.0[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	4.0	10.0[5]	

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NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT191T				FCT191AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	C_L = 50pF R_L = 500Ω	2.5	12.0	1.5	16.0	2.5	7.8	1.5	10.5	ns
t_{PLH} t_{PHL}	Propagation Delay CP to TC		3.0	14.0	2.0	16.0	3.0	11.8	2.0	12.2	ns
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{RC}$		2.5	8.5	1.5	12.5	2.5	8.5	1.5	10.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{RC}$		2.0	8.0	2.0	8.5	2.0	7.2	2.0	8.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}$/D to $\overline{RC}$		4.0	20.0	4.0	22.5	4.0	13.0	4.0	14.7	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}$/D to TC		3.0	11.0	3.0	13.0	3.0	7.2	3.0	8.5	ns
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n		2.0	14.0	1.5	16.0	2.0	9.1	1.5	10.4	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n		3.0	13.0	3.0	14.0	3.0	8.5	3.0	9.1	ns
t_{SU}	Set-up Time, HIGH or LOW P_n to $\overline{PL}$		5.0	—	6.0	—	4.0	—	5.0	—	ns
t_H	Hold Time, HIGH or LOW P_n to $\overline{PL}$		1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{SU}	Set-up Time LOW $\overline{CE}$ to CP		10.0	—	10.5	—	9.0	—	9.5	—	ns
t_H	Hold Time LOW $\overline{CE}$ to CP		0	—	0	—	0	—	0	—	ns
t_{SU}	Set-up Time, HIGH or LOW $\overline{U}$/D to CP		12.0	—	12.0	—	10.0	—	10.0	—	ns
t_H	Hold Time, HIGH or LOW $\overline{U}$/D to CP		0	—	0	—	0	—	0	—	ns
t_W	$\overline{PL}$ Pulse Width LOW		6.0	—	8.5	—	5.5	—	8.0	—	ns
t_W	Clock Pulse Width HIGH or LOW		5.0	—	7.0	—	4.0[3]	—	6.0	—	ns
t_{REM}	Recovery Time $\overline{PL}$ to CP		6.0	—	7.5	—	5.0	—	6.5	—	ns

NOTES:
1. See test circuit and waveform.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This limit is guaranteed but not tested.

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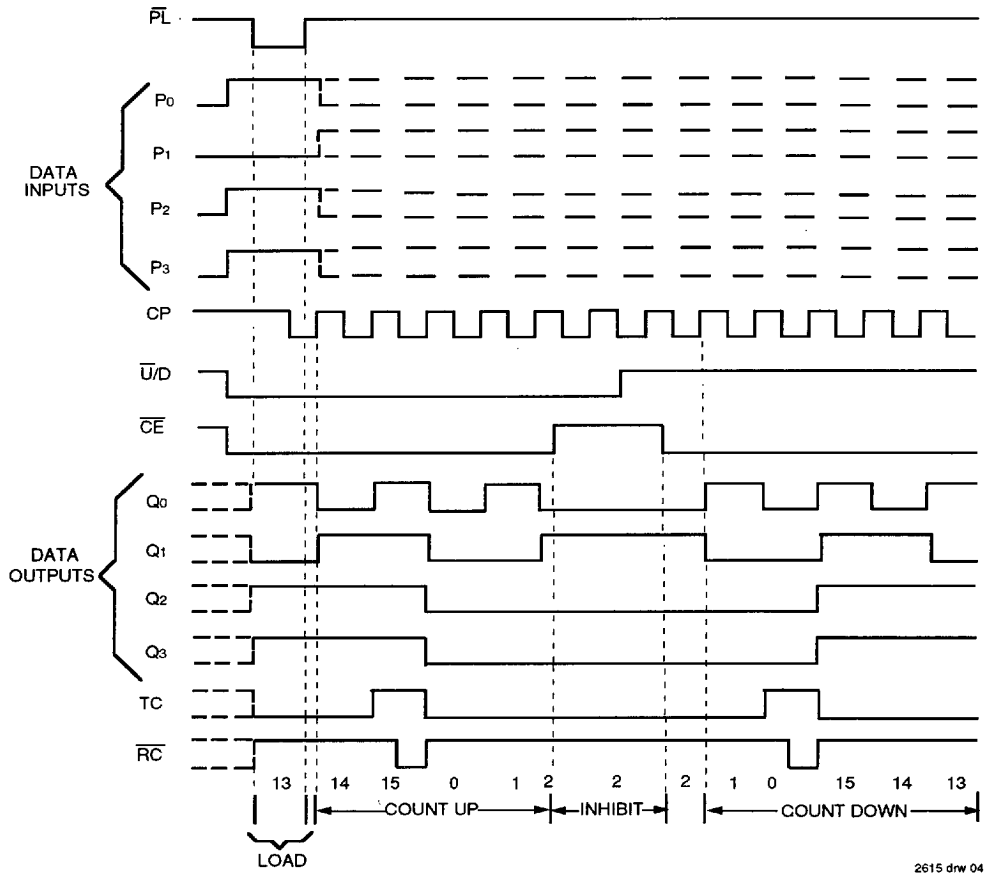
TIMING WAVEFORMS

Typical load, count and inhibit sequences

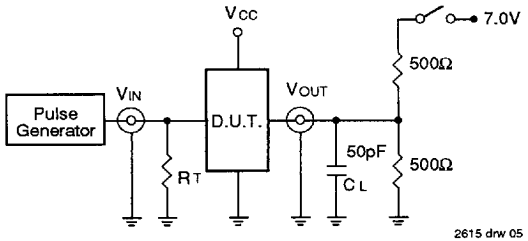
Illustrated below is the following sequence:

- Load (preset) to binary thirteen
- Count up to fourteen, fifteen (maximum), zero, one and two
- Inhibit
- Count down to one, zero (minimum), fifteen, fourteen and thirteen



TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



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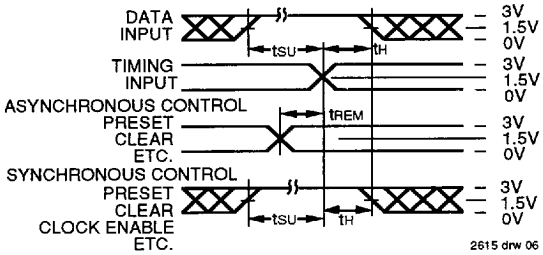
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



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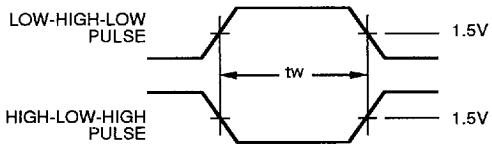
PULSE WIDTH



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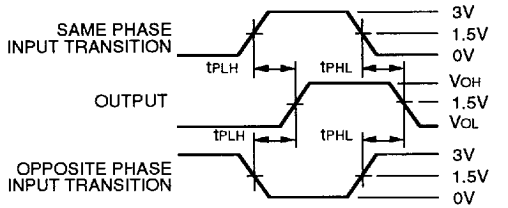
PROPAGATION DELAY



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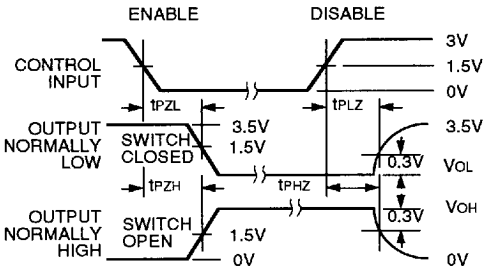
ENABLE AND DISABLE TIMES



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NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

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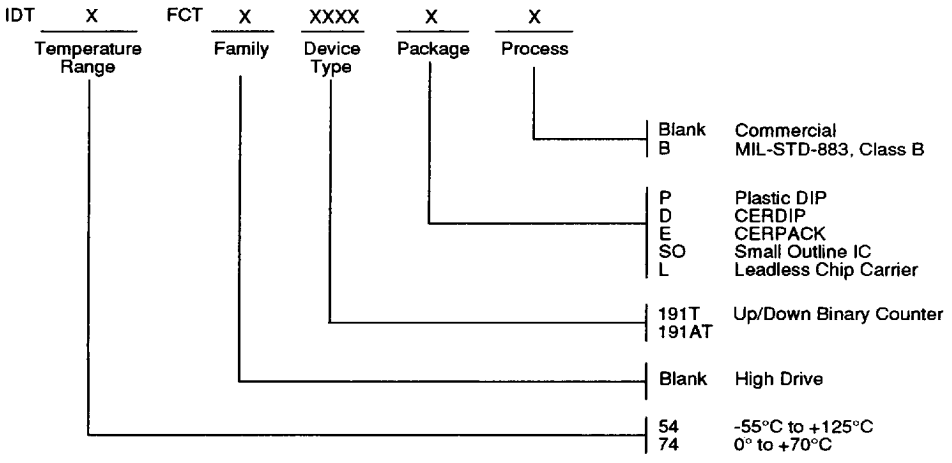
ORDERING INFORMATION



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