SANYO **SANYO Semiconductors**

DATA SHEET

CCB **LV23100V** — Bi-CMOS IC
For Portable Audio System
1-chip Tuner IC
Incorporating PLL

Overview

The LV23100V is a one-chip tuner IC incorporating PLL for portable audio system.

Functions

- AM tuner
- FM tuner
- MPX stereo decoder
- PLL frequency synthesizer

Specifications

Maximum Ratings at Ta = 25 °C

Parameter	Symbol	Conditions		Ratings	Unit
Maximum supply voltage	V_{CC} max	V_{CC}		4.0	V
	V_{DD} max	V_{DD}		4.0	V
Maximum input voltage	$V_{IN}1$ max	CE, CI, CL		6.0	V
	$V_{IN}2$ max	XIN		$V_{DD}+0.3$	V
Allowable power dissipation	Pd max	Ta≤70°C		180	mW
Maximum output voltage	V_O1 max	DO		6.0	V
	V_O2 max	XOUT, PD		$V_{DD}+0.3$	V
	V_O3 max	BO1, BO2, AOUT		12.0	V
Operating temperature	Topr			-20 to +70	°C
Storage temperature	Tstg			-40 to +125	°C

Note : This product should be handled with care because the resistance against electrostatic discharge damage is low.

- CCB is a registered trademark of SANYO Electric Co., Ltd.
- CCB is SANYO Semiconductor's original bus format. All bus addresses are managed by SANYO Semiconductor for this format.

LV23100V

Operating Condition at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		3.0	V
	V_{DD}		3.0	V
Operating supply voltage range	V_{CC} op		2.2 to 3.6	V
	V_{DD} op		2.2 to 3.6	V

PLL block Allowable Operating Range at Ta = -20°C to +70°C, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		2.2		3.6	V
Input high level voltage	V_{IH}	CE, CL, DI	$0.7V_{DD}$		6.0	V
Input low level voltage	V_{IL}	CE, CL, DI	0		$0.3V_{DD}$	-
Output voltage	V_O1	DO	0		6.0	V
	V_O2	BO1, BO2, AOUT	0		10	V
Operating frequency	$f_{IN}1$	XIN ; $V_{IN}1$		75		kHz
	$f_{IN}2$	FMIN ; $V_{IN}2$	10		160	MHz
	$f_{IN}3$	AMIN (SNS = 1) ; $V_{IN}3$	2		40	MHz
	$f_{IN}4$	AMIN (SNS = 0) ; $V_{IN}4$	0.5		10	MHz

Note : Due attention must be paid on leak because the XIN pin has an extremely high input impedance.

Operating Characteristics at Ta = 25°C, $V_{CC} = V_{DD} = 3.0V$, See the specified circuit.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Current dissipation]						
FM tuner block	$I_{CC}FM$	No input in FM mode	9	12.5	16	mA
AM tuner block	$I_{CC}AM$	No input in AM mode	4	6	8	mA
PLL block	$I_{DD}FM$	fr = 98MHz, No input at tuner	1	2	4	mA
[FM-FE characteristics] : fc = 98MHz, fm = 1kHz, dev = 22.5kHz						
3dB sensitivity	-3dBLS	V_{IN} = 60dBμV EMF reference, -3dB input		10		dBμV EMF
Actual sensitivity	QS	S/N = Input at S/N = 30dB		13		dBμV EMF
[FM-IF characteristics] : fc = 10.7MHz, fm = 1kHz, dev = 75kHz (L+R = 90%, Pilot = 10%)						
Demodulation output	V_O	V_{IN} = 100dBμV	140	180	210	mVrms
3dB sensitivity	LS	V_{IN} = 100dBμV reference, -3dB input	26	31	36	dBμV
Signal-to-noise ratio	S/N	V_{IN} = 100dBμV	63	70		dB
IF count sensitivity	IF-C1	0%mod, SDC = 1	42	50	56	dBμV
Total harmonic distortion	THD	V_{IN} = 100dBμV, MAIN-MOD		0.5	1.5	%
Separation	SEP	V_{IN} = 100dBμV, L output/R output	25	40		dB
Mute attenuation	MUTE	V_{IN} = 100dBμV, L output	55	60		dB
[AM characteristics] : fc = 1000kHz, fm = 1kHz, 30%mod						
Demodulation output	V_O	V_{IN} = 80dBμV	30	50	70	mVrms
Signal-to-noise ratio 1	S/N1	V_{IN} = 23dBμV	15	20		dB
Signal-to-noise ratio 2	S/N2	V_{IN} = 80dBμV	47	53		dB
Total harmonic distortion	THD	V_{IN} = 80dBμV		0.5	1.5	%
IF count sensitivity	IF-C	0%mod	20	27	34	dBμV

LV23100V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[PLL characteristics]						
Internal return resistance	Rf	XIN		8		MΩ
Built-in output resistance	Rd	XOUT		250		kΩ
Hysteresis width	VHIS	CE, CL, DI		$0.1V_{DD}$		V
Output high level voltage	V_{OH}	PD ; I_O = -1mA	V_{DD}-1.0			V
Output low level voltage	$V_{OL}1$	PD ; I_O = 1mA			1.0	V
	$V_{OL}2$	BO1, BO2 ; I_O = 1mA			0.25	V
		BO1, BO2 ; I_O = 5mA			1.25	V
	$V_{OL}3$	DO ; I_O = 1mA			0.25	V
	$V_{OL}4$	AOUT ; I_O = 1mA, AIN = 2.0V			0.5	V
Input high level current	$I_{IH}1$	CE, CL, DI ; V_I = 6.0V			5.0	μA
	$I_{IH}2$	XIN ; V_I = V_{DD}	0.16		0.9	μA
	$I_{IH}3$	AIN ; V_I = 6.0V			200	nA
Input low level current	$I_{IL}1$	CE, CL, DI ; V_I = 0V			5.0	μA
	$I_{IL}2$	XIN ; V_I = 0V	0.16		0.9	μA
	$I_{IL}3$	AIN ; V_I = 0V			200	nA
Output off-leak current	IOFF1	BO1, AOUT, BO2 ; V_O = 10V			5.0	μA
	IOFF2	DO ; V_O = 6.0V			5.0	μA
"H" level 3-state off-leak current	IOFFH	PD ; V_O = 6.0V		0.01	200	nA
"L" level 3-state off-leak current	IOFFL	PD ; V_O = 0V		0.01	200	NA

Package Dimensions

unit : mm (typ)

3247A

SANYO : SSOP36(275mil)

LV23100V
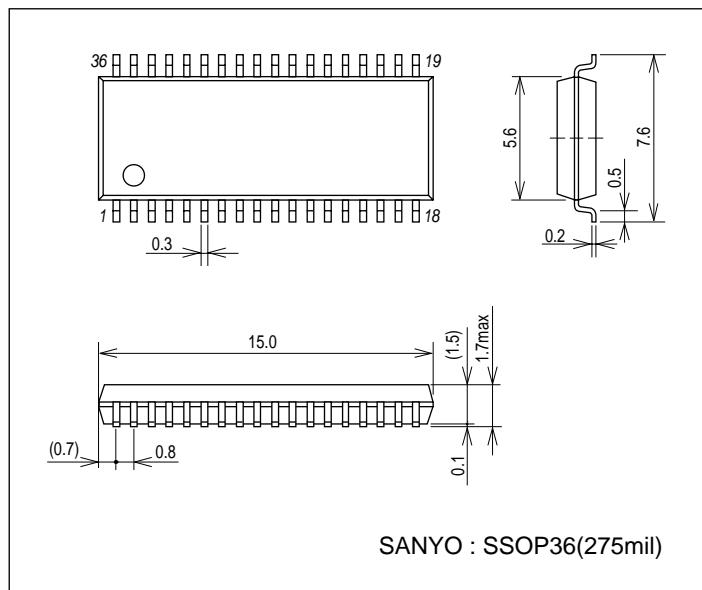
Composition of DI control data (serial data input)

(1) IN mode

Address

DI ◄ 0 0 0 1 0 1 0 0

P0 P1 P2 P3 P4 P5 P6 P7 P8 P9 P10 P11 P12 P13 P14 P15 SNS DVS CTE 0 R0 R1 R2 R3

(1)P-CTR (3)IF-CTR (2)R-CTR

(2) IN2 mode

Address

DI ◄ 1 0 0 1 0 1 0 0

0 1 0 BO2 BO1 IFSW BDSW STSW SDC DOC0 DOC1 DOC2 UL0 UL1 DZ 0 GT0 GT1 DLC XS 1 TEST0 TEST1 TEST2

(4)O-PORT (5)IFSW (6)BDSW (7)STSW (8)SD-C (9)DO-C (10)UNLOCK (11)DZ-C (3)IF-CTR (12)PD-C (2)R-CTR (13)TEST
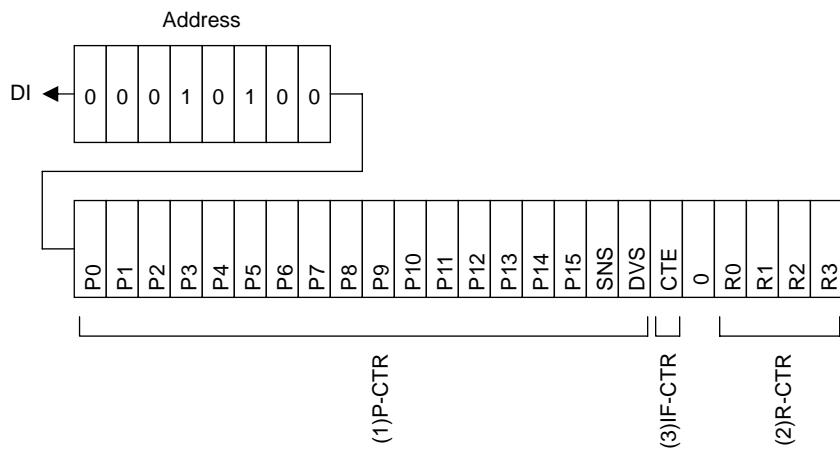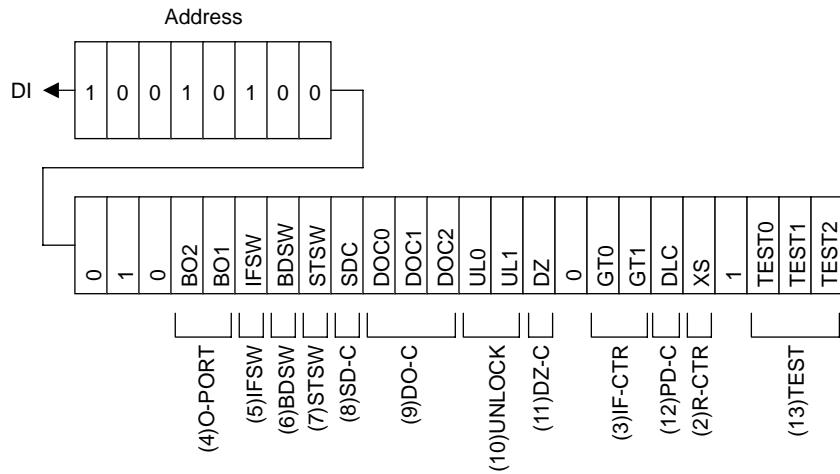
Description of DI control Data

No.	Control block data	Description	Related data
(1)	DO pin Control data DOC0 DOC1 DOC2	• Data to set the dividing number of programmable divider. Binary value with P15 assumed to be MSB. LSB varies according to DVS and SNS. (* : don't care) 	DVS	SNS	LSB	set dividing number (N)	actual dividing number
1	*	P0	272 to 65535	Twice the set value
0	1	P0	272 to 65535	Set value
0	0	P4	4 to 4095	Set value | * P0 to P3 invalid when LSB : P4 • To select the signal input (FMIN, AMIN) to the programmable divider and to change the input frequency range. (* : don't care) | DVS	SNS	Input	Operation frequency range
1	*	FMIN	10 to 160MHz
0	1	AMIN	2 to 40MHz
0	0	AMIN	0.5 to 10MHz		

Continued from preceding page.

No.	Control block data	Description	Related data
(2)	Reference divider data R0 to R3 XS	• Reference frequency (fref) selection data | R3	R2	R1	R0	Reference frequency | |---|---|---|---|---| | 0 | 0 | 0 | 0 | 25kHz | | 0 | 0 | 0 | 1 | 25kHz | | 0 | 0 | 1 | 0 | 25kHz | | 0 | 0 | 1 | 1 | 25kHz | | 0 | 1 | 0 | 0 | 12.5kHz | | 0 | 1 | 0 | 1 | 6.25kHz | | 0 | 1 | 1 | 0 | 3.125kHz | | 0 | 1 | 1 | 1 | 3.125kHz | | 1 | 0 | 0 | 0 | 5kHz | | 1 | 0 | 0 | 1 | 5kHz | | 1 | 0 | 1 | 0 | 5kHz | | 1 | 0 | 1 | 1 | 1kHz | | 1 | 1 | 0 | 0 | 3kHz | | 1 | 1 | 0 | 1 | 15kHz | | 1 | 1 | 1 | 0 | PLL INHIBIT+X'tal OSC STOP | | 1 | 1 | 1 | 1 | PLL INHIBIT | * PLL INHIBIT • The programmable divider and IF counter stop, with FMIN, AMIN, and IFIN inputs being in the pull-down condition (GND), and the charge pump has the high impedance. • XS must be zero.	
(3)	IF counter control data CTE GT0, GT1	• IF counter counting start data CTE = 1 : Counting start = 0 : Counting start • Determines the counting time of universal counter | GT1	GT0	Counting time	Wait time | |---|---|---|---| | 0 | 0 | 4ms | 3 to 4ms | | 0 | 1 | 8ms | 3 to 4ms | | 1 | 0 | 16ms | 3 to 4ms | | 1 | 1 | 32ms | 3 to 4ms |	
(4)	Output port data $\overline{BO1}$, $\overline{BO2}$	• Data to determine output of output ports $\overline{BO1}$ and $\overline{BO2}$ "Data" = 0 : OPEN 1 : Low	
(5)	MUTE control data IFSW	• Data to determine the output of output port IFSW, controlling the MUTE function. "Data" = 0 : at receiving 1 : MUTE	
(6)	FM/AM BAND selection control data BDSW	• Data to determine the output of output port BDSW, controlling selection of BAND. "Data" = 0 : AM 1 : FM	
(7)	Forced monaural control data STSW	• Data to determine the output of output port STSW, controlling the forced stereo functions. "Data" = 0 : MONO 1 : STEREO	
(8)	SD sensitivity control data SDC	• Data to determine the output of output port SDC, controlling the FM-SD sensitivity (at IF input). 	SDC	FM-SD sensitivity	 |---|---| | 0 | 38dBµV | | 1 | 48dBµV |	

Continued from preceding page.

No.	Control block data	Description	Related data
(9)	DO pin control data DOC0 DOC1 DOC2	• Data to determine the output of the DO pin. _table below_ • The open condition is selected at power ON/reset. * IF counter counting end check _diagram below_ ① With end-UC set and IF counter starting (CTE = 0→1), DO pin opens automatically. ② At end of counting of the IF counter, DO pin goes LOW and check on counting end can be made. ③ DO pin opens when serial data is entered/output (CE pin : Hi) Note : DO pin is always in the open condition during data input (IN1 and IN2 modes, during CE : Hi period), regardless of DO pin control data (DOC0 to 2). In the DO pin condition during data output (OUT mode, CE-Hi period), the content of internal DO serial data is output in synchronization with CL, regardless of DO pin control data (DOC).	UL0, UL1 CTE
(10)	Unlock detection data UL0, UL1	• Phase error (ϕE) detection width selection data to judge if PLL is locked. • Phase error exceeding the detection width is judged that PLL is locked (* : don't care) _table below_ * DO pin is LOW. Serial data output : UL = 0.	DOC0 DOC1 DOC2
(11)	Phase comparator control data DZ	• Data to control the dead zone of phase comparator _table below_ Dead zone width : DZA<DZB	
(12)	Charge pump control data DLC	• Data to enforce control of charge pump output _table below_ In case of dead lock because of VCO oscillation stop when the VCO control voltage (Vtune) is 0V, it is possible to clear dead lock by setting the charge pump output to LOW and V tune to V_{CC}. (Dead lock clear circuit)	
(13)	LSI test data TEST0 to 2	• LSI test data TEST0 TEST1 All to be set to "0" TEST2 All set to zero at power ON/reset	

Table for (9):

DOC2	DOC1	DOC0	DO pin condition
0	0	0	Open
0	0	1	Low when unlock is detected.
0	1	0	end-UC (See the item with asterisk below)
0	1	1	Open
1	0	0	Open
1	0	1	Low when stereo
1	1	0	Low when SDON
1	1	1	Open

Diagram for (9):

DO pin

① Counting start　② Counting end　③ CE : HI

Table for (10):

UL1	UL0	ϕE Detection width	Detection output
0	0	Stop	Open
0	1	0	Direct output of ϕE
1	*	±6.67μs	ϕE extended by 1 to 2 ms

Table for (11):

DZ	Charge pump output
0	DZA
1	DZB

Table for (12):

DLC	Charge pump output
0	Normal
1	Forced to LOW

DO control data (serial data output) composition

(1) OUT mode

Address

DI ← | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |

DO ← | SDIND | STIND | 0 | UL | C19 | C18 | C17 | C16 | C15 | C14 | C13 | C12 | C11 | C10 | C9 | C8 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |

(1)IN-PORT (2)UNLOCK (3)IF-CTR
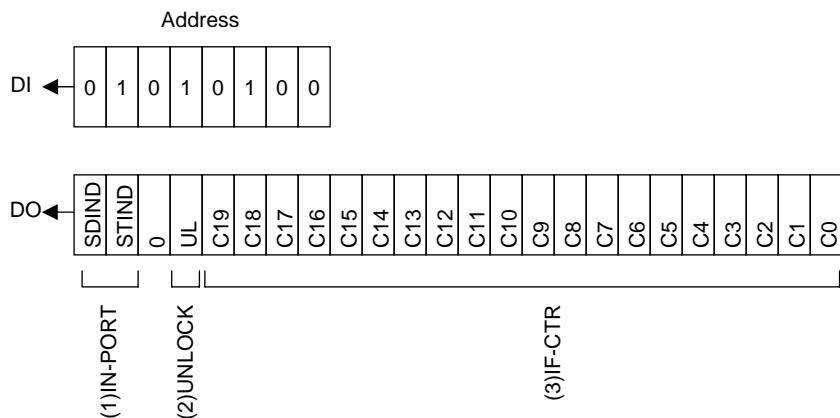
Description of DO output data

| No.	Control block data	Description	Related data

(1)	SD and Stereo indicators control data
	
	STIND, SDIND
		• Data latching SD and stereo indicator conditions.
		  Latching made in the data output (OUT) mode.
		    SDIND←SD indicator condition 0 : SD ON, 1 : SD OFF
		    STIND←Stereo indicator condition 0 : ST ON, 1 : ST OFF	

(2)	PLL unlock data
	
	UL
		• Data latching the content of unlock detection circuit
		    UL←0 : At unlock
		          1 : At lock or detection stop mode
			UL0
			UL1

(3)	IF counter, binary counter
	
	C19 to C0
		• Data latching the content of IF counter (20-bit binary counter)
		    C19←MSB of binary counter
		    C0 ←MSB of binary counter
			CTE
			GT0
			GT1

LV23100V

Serial data input (IN1/IN2) tSU, tHD, tEL, tES, tEH≥0.75μs tLC<0.75μs

CL : Normally Hi
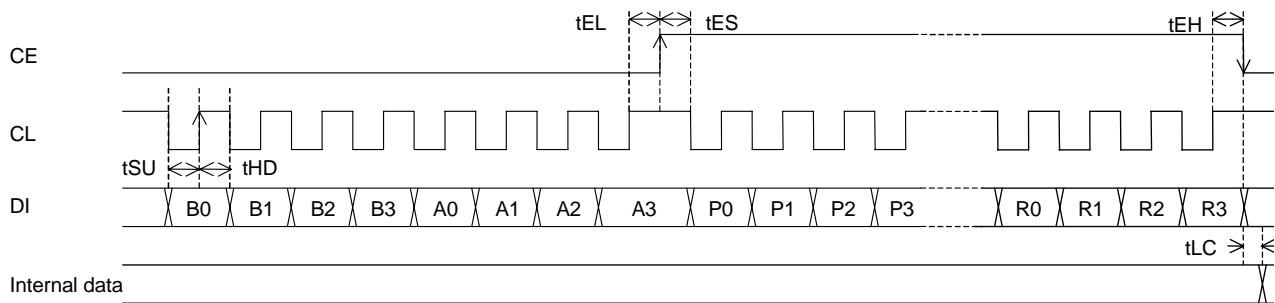
CL : Normally Low
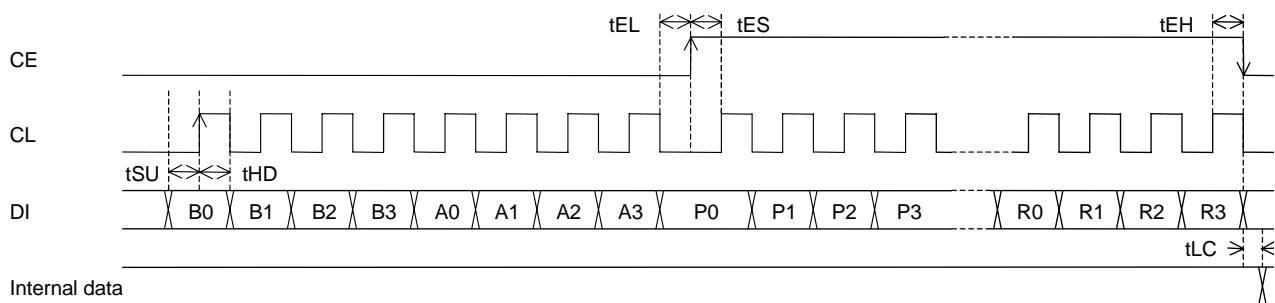
Serial data output (OUT) tSU, tHD, tEL, tES, tEH≥0.75μs tDC, tDH<0.35μs

CL : Normally Hi
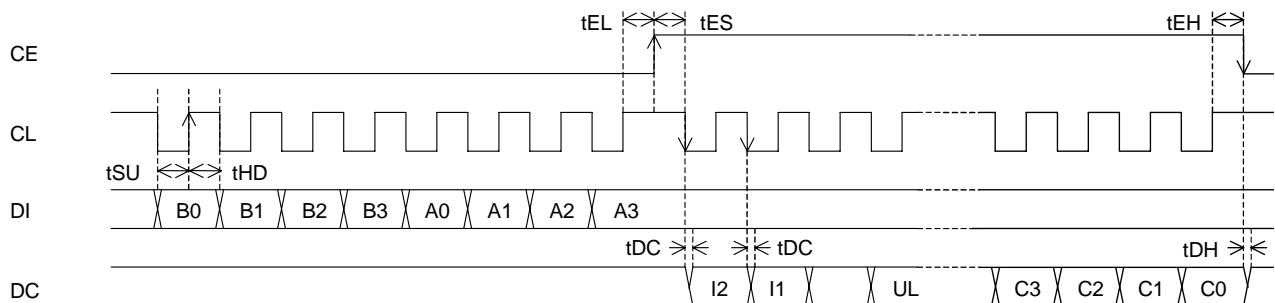

CL : Normally Hi
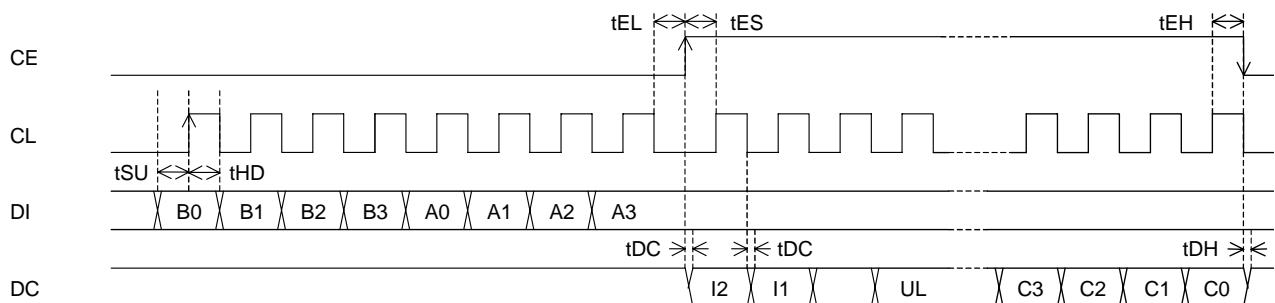

(Note) DO pin is an Nch open drain pin, so that the data varying time (tDC and tDH) differs depending on the pull-up resistance and substrate capacity.

LV23100V

Serial data timing
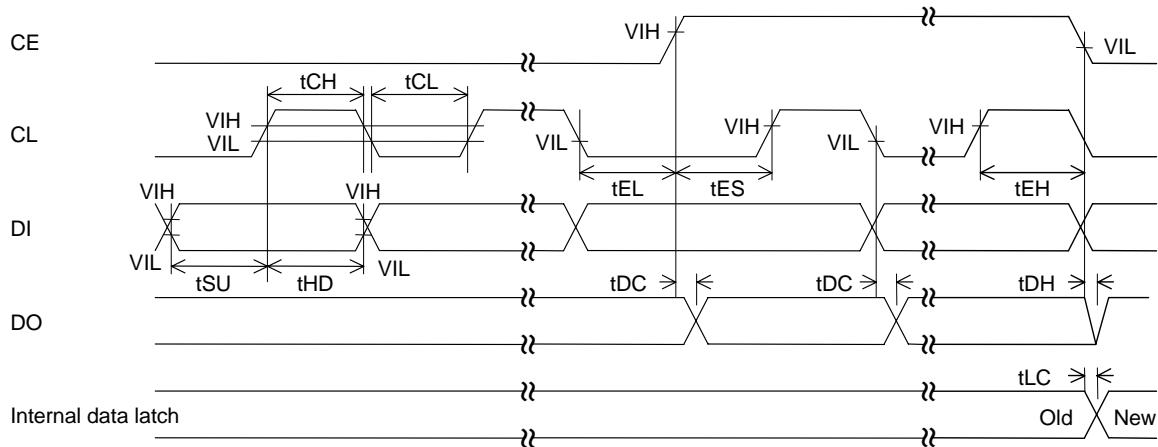
<< When CL stops at the "L" level >>
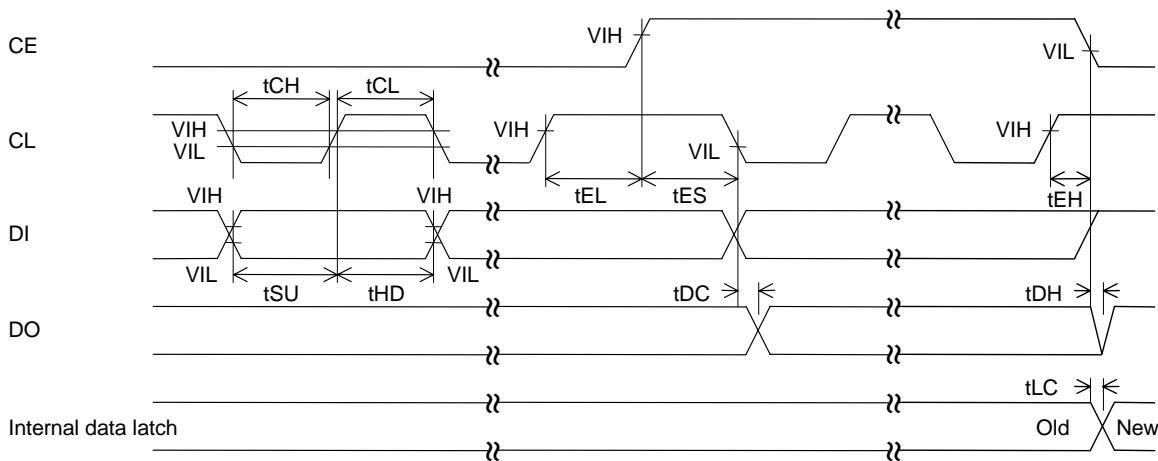
<< When CL stops at the "H" level >>

Parameter	Symbol	Pin	Conditions	Min	Typ	Max	Unit
Data setup time	tSU	DI, CL		0.75			μs
Data hold time	tHD	DI, CL		0.75			μs
Clock "L" level time	tCL	CL		0.75			μs
Clock "H" level time	tCH	CL		0.75			μs
CE wait time	tEL	CE, CL		0.75			μs
CE setup time	tES	CE, CL		0.75			μs
CE hold time	the	CE, CL		0.75			μs
Data latch change time	tLC					0.75	μs
Data output time	tDC	DO, CL	Differs depending on the pull-up resistance and substrate capacity			0.35	μs
	tDH	DO, CE					

Block Diagram and Sample Application Circuit
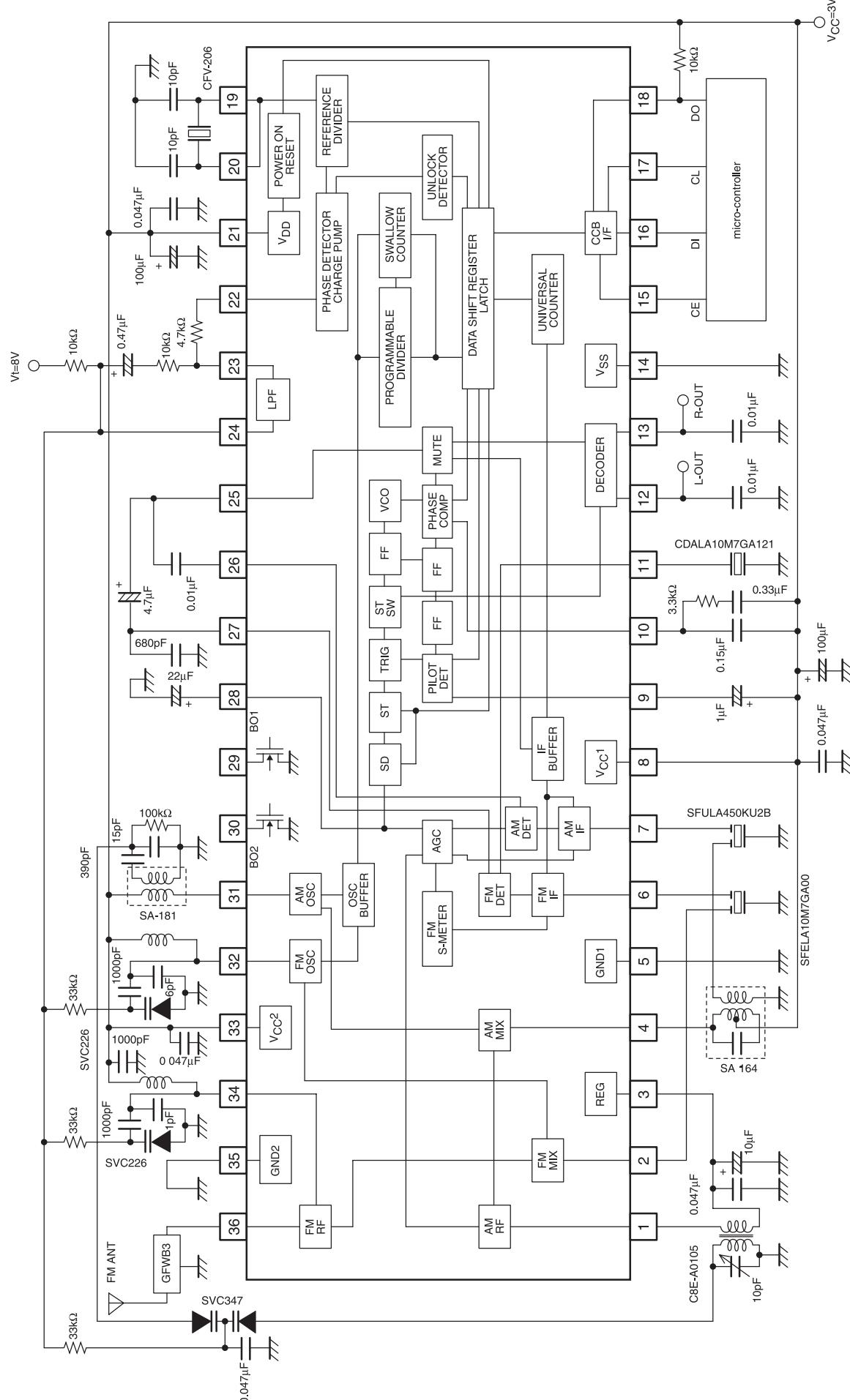
Test Circuit
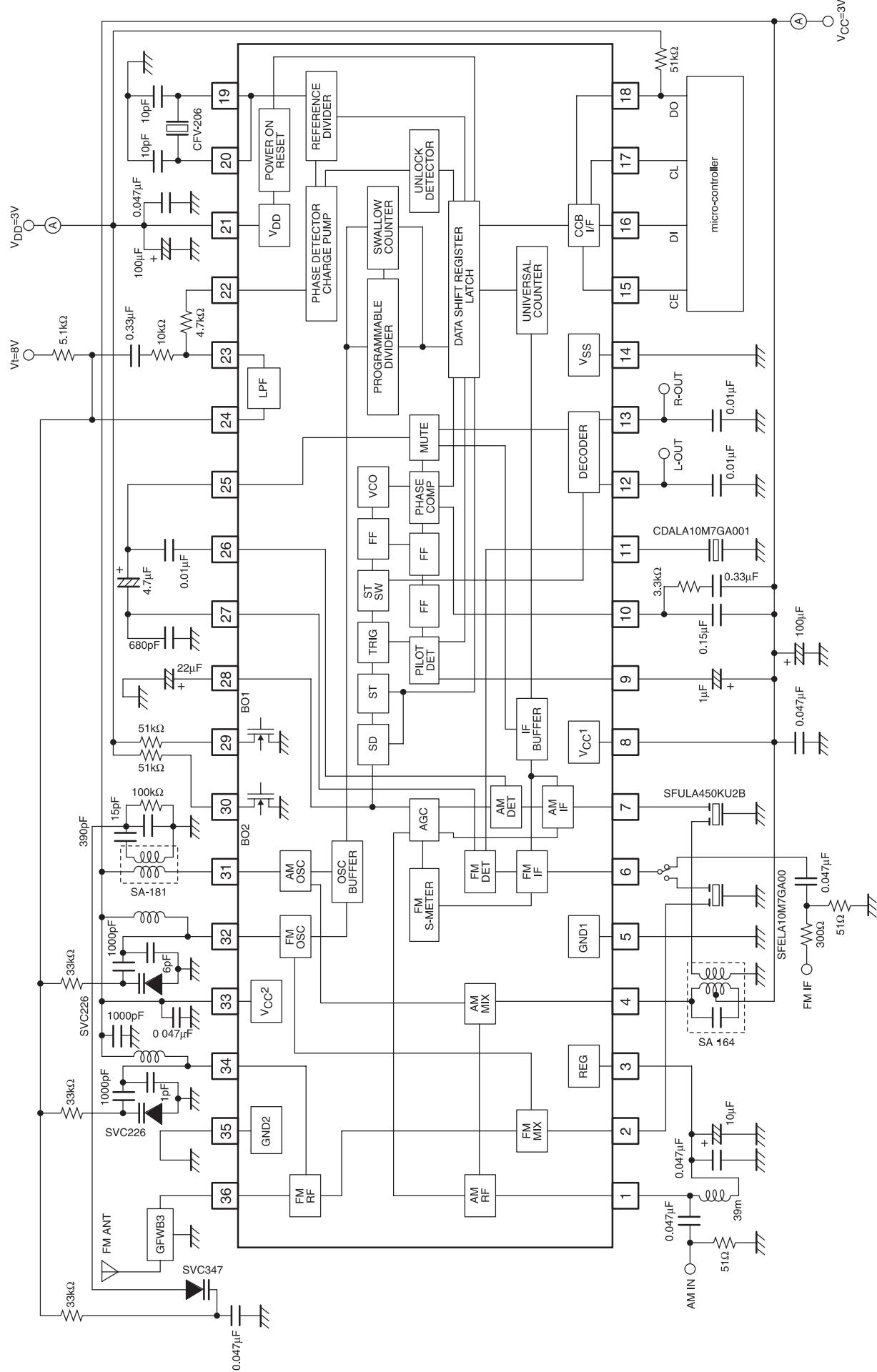
Coil specifications (bottom view)

• FM-BPF : GFWB3 (Soshin) 76MHz to 108MHz
• FM-RF : SA-149 (Sumida) 3.6mm diameter, air core, 0.6mm wire, 4.5T
• FM-OSC : SA-151 (Sumida) 3.6mm diameter, air core, 0.6mm wire, 3.5T
• FM-IF Filter : SFELA10M7GA00 (Murata)
• FM-Discriminator : CDALA10M7GA121 (Murata)

• AM-OSC : SA-181 (Sumida)

6-4	37T
3-1	74T

0.06UEW
fo = 796kHz
Qo≥80
L = 140µH

• AM-MIX : SA-164 (Sumida)

1-2	122T
4-6	9T
2-3	62T

0.06UEW
fo = 450kHz, Qo≥65
C = 180pF
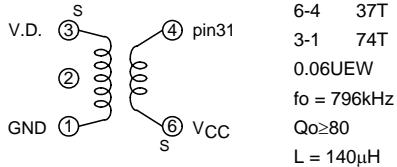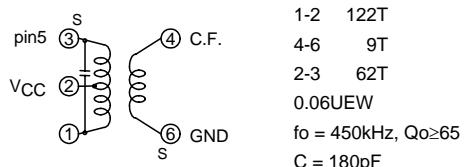
• AM-IF Filter : SFULA450KU2B (Murata)

• MW Bar-antenna : C8E-A0105 (Toko)

1-2	67T
3-4	9T

fo = 796kHz
Qo = 180min
L = 260µH

• Crystal oscillator : CFV-206 (Citizen)

This catalog provides information as of April, 2008. Specifications and information herein are subject to change without notice.