SSI 73K312L

Bell 202, 103 and CCITT V.23, V.21 Single-Chip Modem

Preliminary Data

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SILICON SYSTEMS INC 61E D

December 1992

T-75-33-05

DESCRIPTION

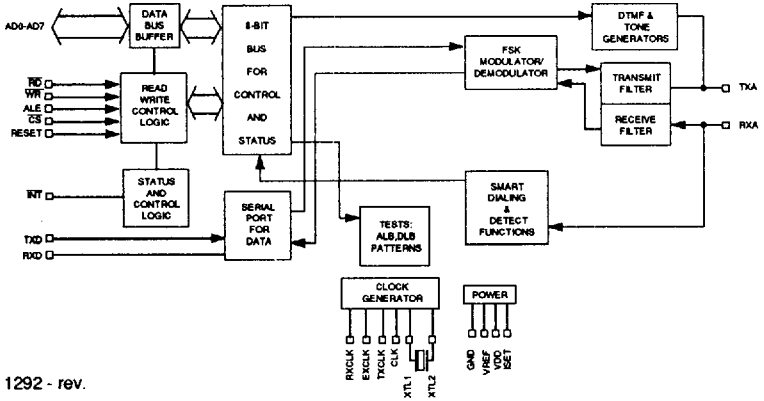
The SSI 73K312L is a highly integrated single-chip modem IC which provides the functions needed to construct a CCITT V.23, V.21, Bell 202, 103 FSK modem. The 73K312L supports asynchronous 1200 bit/s (600 bit/s at V.23 half speed mode) with or without 75/150 bit/s back channel (75 for V.23 and 150 for Bell 202) and 300 bit/s FSK (V.21 or Bell 103). The SSI 73K312L can also both detect and generate the CCITT and Bell answer tones needed for call initiation. The SSI 73K312L integrates analog, digital, and switched-capacitor array functions on a single substrate, offering excellent performance and a high level of functional integration in a single 28- or 22-pin DIP or 28 pin PLCC configuration. The SSI 73K312L operates from a single +5 V supply with very low power consumption.

The SSI 73K312L includes the FSK modulator/demodulator functions, call progress and handshake tone monitor test modes, and a tone generator capable of producing DTMF, answer, calling and 900 Hz soft carrier turnoff tones. The SSI 73K312L is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular one-chip microprocessors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or via an optional serial command bus. An ALE control line simplifies address demultiplexing. Data communications occur through a separate serial port only.

FEATURES

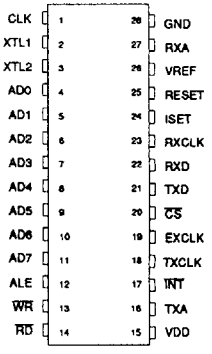
- **Bell 202, 103 and CCITT V.23, V.21 single-chip modem**
- **Full-duplex operation at 0-300 bit/s (V.21 and Bell 103)**
- **V.23 modes 1, 2, (i.e., 0-600 bit/s and 0-1200 bit/s) forward channel with or without 0-75 bit/s back channel**
- **Bell 202 0-1200 bit/s forward channel with or without 0-150 bit/s back channel**
- **Full Duplex 4-wire mode operation in V.23 and Bell 202 modes**
- **Pin and software compatible with other SSI K-Series 1-chip modems**
- **Interfaces directly with standard microprocessors (8048, 80C51 typical)**
- **Serial or parallel microprocessor bus for control**
- **Serial port for data transfer**
- **Call progress, carrier, precise answer tone (2100 or 2225 Hz), and precise mark detectors**
- **Precise calling tone and soft carrier turnoff generators/detectors (1300 Hz, 900 Hz)**
- **DTMF generator**
- **Test modes available: ALB, DL, Mark, Space, Alternating bit patterns**
- **Precise automatic gain control allows 45 dB dynamic range**
- **CMOS technology for low power consumption using 30 mW @ 5V from a single power supply**

BLOCK DIAGRAM



1292 - rev.

PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

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OPERATION

The SSI 73K312L is ideal for either free standing or integral system modem applications where multi-standard data communications is desired. Typical uses include videotex terminals, low-cost integral modems and built-in diagnostics for office automation or industrial control systems. The 73K312L's high functionality, low power consumption and efficient packaging simplify design requirements and increase system reliability in these applications. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level converter for a typical system.

Quad-mode capability in one-chip allows full-duplex V.21 and Bell 103 operation or asymetrical V.23 and Bell 202 operation over the 2-wire switched telephone network. V.23 and 202 mode full-duplex operation at 1200 bit/s is also possible when operating on 4-wire leased lines.

A soft carrier turn-off feature facilitates fast line turn around when using the 202 or V.23 modes for half-duplex applications.

The SSI 73K312L is part of Silicon Systems K-Series family of pin and function compatible single-chip modem products. These devices allow systems to be configured for higher speeds and Bell or CCITT operation with only a single component change.

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. V.21 mode uses 980 and 1180 Hz (originate, mark and space) or 1650 and 1850 Hz (answer, mark and space). V.23 mode uses 1300 and 2100 Hz for the main channel and 390 and 450 Hz for the back channel. The modulation rate of the back channel is up to 75 baud. Bell 103 mode uses 1270 and 1070 Hz (originate, mark and space) or 2225 and 2025 Hz (answer, mark and space). Bell 202 mode uses 1200 and 2200 Hz for the main channel and 387 and 487 Hz for the back channel. The modulation rate of the back channel is up to 150 baud. Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value.

PASSBAND FILTERS AND EQUALIZERS

A high and low band filter is included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line.

AGC

The automatic gain control maintains a signal level at the input to the demodulators which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping and provides a total dynamic range of >45 dB.

PARALLEL BUS INTERFACE

Six 8-bit registers are provided for control, option select and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as memory locations. Three control registers and the tone register are read/write memory. The status detect register is read only and cannot be modified except by modem response to monitored parameters. The parallel bus interface is not available with the 22-pin package.

SERIAL COMMAND INTERFACE

The serial command mode allows access to the SSI 73K312L control and status registers via a serial command port. In this mode the A0, A1 and A2 lines provide register addresses for data passed through the data pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The next eight cycles of EXCLK will then transfer out eight bits of the selected address location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transferred into the selected register occurs on the rising edge of $\overline{WR}$.

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SPECIAL DETECT CIRCUITRY

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, answer tone and weak received signal (long loop condition), special tones such as FSK marking tones, calling tones and the 900 Hz soft carrier turn-off tone are also detected. A highly frequency selective call progress detector provides adequate discrimination to accurately detect European call progress signals.

DTMF GENERATOR

The DTMF generator will output one of 16 standard dual-tones determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Tone generation is initiated when the DTMF mode is selected and the transmit enable (CR0 bit D1) is changed from 0 to 1.

SOFT CARRIER TURN-OFF TONE GENERATOR

The soft carrier turn-off tone generator will output a 900 Hz tone. When activated in Bell 202 main channel transmit mode, the output signal will shift to 900 Hz, maintaining phase continuity during the transition.

PIN DESCRIPTION

POWER

NAME	TYPE	DESCRIPTION
GND	I	System Ground.
VDD	I	Power supply input, 5V ±10%. Bypass with 0.1 and 22 µF capacitors to ground.
VREF	O	An internally generated reference voltage. Bypass with 0.1 µF capacitor to ground.
ISET	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. ISET should be bypassed to GND with a 0.1 µF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

ALE	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{CS}$.
AD0-AD7	I/O	Address/data bus. These bidirectional tri-state multi-plexed lines carry information to and from the internal registers.
$\overline{CS}$	I	Chip select. A low on this pin allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. The state of $\overline{CS}$ is latched on the falling edge of ALE.
CLK	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or clock depending on the mode: 19.2 kHz (Bell103), 15.36 kHz (V.21, V.23, Bell 202). The pin defaults to the crystal frequency on reset.

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PIN DESCRIPTION (Continued)

PARALLEL MICROPROCESSOR INTERFACE (Continued)

NAME	TYPE	DESCRIPTION
$\overline{INT}$	O	Interrupt. This open drain output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{INT}$ will stay low until the processor reads the detect register or does a full reset.
$\overline{RD}$	I	Read. A low requests a read of the SSI 73K312L internal registers. Data cannot be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active (low).
RESET	I	Reset. An active high signal on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, CR3) will be reset except for the D2 bit of CR3 which will be set to one to allow nominal transmit power. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a 1 µF capacitor to VDD.
$\overline{WR}$	I	Write. A low on this informs the SSI 73K312L that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and the latched $\overline{CS}$ are active (low).

SERIAL MICROPROCESSOR INTERFACE

A0-A2	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
DATA	I/O	Serial Control Data. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
$\overline{RD}$	I	Read. A low on this input informs the SSI 73K312L that data or status information is being read by the processor. The falling edge of the $\overline{RD}$ signal will initiate a read from the addressed register. The $\overline{RD}$ signal must continue for seven falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{WR}$	I	Write. A low on this input informs the SSI 73K312L that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.

Note: The Serial Control mode is provided in the parallel control versions by floating ALE and $\overline{CS}$ or tying ALE high and $\overline{CS}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.

The Serial mode data and clock signals are compatible with the serial port mode 0 of the 8051.

RS-232 INTERFACE

NAME	TYPE	DESCRIPTION
EXCLK	I	External Clock. Used for serial control interface to clock control data in or out of the 73K312L.
RXCLK	O	Receive Clock. In V.23 2-wire mode RXCLK equals 16 x 1200 if answering and 16 x 75 if originating. In Bell 202 2-wire mode RXCLK equals 16 x 1200 if answering and 16 x 150 if originating. In V.21 or Bell 103 mode it equals 16 x 300.
RXD	O	Received Digital Data Output. Serial receive data is available on this pin. RXD will output constant marks if no carrier is detected.
TXCLK	O	Transmit Clock. If 1200 bit/s mode is selected, TXCLK equals 16 x1200 if originating and 16 x 75 (V.23) or 16 x 150 (Bell 202) if answering. In V.21 or Bell 103 mode it equals 16 x 300.
TXD	I	Transmit Digital Data Input. Serial data for transmission is input on this pin.

ANALOG INTERFACE AND OSCILLATOR

RXA	I	Received modulated analog signal input from the phone line.
TXA	O	Transmit analog output to the phone line.
XTL1 XTL2	I I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz parallel mode crystal and two load capacitors to Ground. XTL1 can also be driven from an external clock.

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REGISTER DESCRIPTIONS

Four 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0, A1 and A2 address lines in serial mode, or the AD0, AD1 and AD2 lines in parallel mode. The AD0, AD1 and AD2 lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K312L internal state. CR3 controls the attenuation of the transmitted signal and enables receive gain boost. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer and RX output gate used in the modem initial connect sequence. All registers are read/write except for DR which is read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	SPEED SELECT		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	ADD PH. EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010			RECEIVE DATA		CARRIER DETECT	SPECIAL TONE	CALL PROGRESS	LONG LOOP
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT SPECIAL TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2/ V.23 FDX 202 FDX	DTMF1	DTMF0/ TONE SELECT
CONTROL REGISTER 2 CR2	100	THIS REGISTER LOCATION IS RESERVED FOR USE WITH OTHER K-SERIES FAMILY MEMBERS							
CONTROL REGISTER 3 CR3	101				RECEIVE ENABLE BOOST	TRANSMIT ATTEN. 3	TRANSMIT ATTEN. 2	TRANSMIT ATTEN. 1	TRANSMIT ATTEN. 0
ID REGISTER ID	110	ID	ID	ID	ID				

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

REGISTER ADDRESS TABLE

REGISTER	ADDRESS AD2 - AD0	DATA BIT NUMBER D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	SPEED SELECT		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ORIGINATE/ ANSWER
		0=V.23 or BELL 103 1=V.21 or BELL 202		0000=PWR DOWN 1000=BELL 103 or 202 1100=CCITT V.23 or V.21 1110=CCITT V.23 MC HALF SPEED				0=SQUELCH ANALOG 1=ENABLE ANALOG	V.21 AND BELL 103: 0=ANSWER 1=ORIGINATE V.23 AND BELL 202: 0=RECEIVE @ 1200/600 BIT/S TRANSMIT @ 75/150 BIT/S 1=RECEIVE @ 75/150 BIT/S TRANSMIT @ 1200/600 BIT/S
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	ADD PH. EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
			00=TX DATA 01=TX ALTERNATE 10=TX MARK 11=TX SPACE	IN V.23 or BELL 202 MODE 0=OFF 1=ON	0=NORMAL EQ. 1=ADD EXTRA PHASE EQ. IN SERIES WITH MAIN CHANNEL	0=XTAL 1=19.2 kHz or 15.36 kHz	0=NORMAL 1=RESET		00=NORMAL 01=ANALOG LOOPBACK 11=LOCAL DIGITAL LOOPBACK
DETECT REGISTER DR	010			RECEIVE DATA		CARRIER DETECT	SPECIAL TONE	CALL PROGRESS	LONG LOOP
				OUTPUTS RECEIVED DATA STREAM		0=CONDITION NOT DETECTED 1=CONDITION DETECTED			
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT SPECIAL TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2/ V.23 FDX 202 FDX	DTMF1	DTMF0/ TONE SELECT
		RXD PIN 0=NORMAL 1=TRI STATE	0=OFF 1=TRANSMITS CALLING TONE IF ORIGINATING IN CCITT MODE. TRANSMITS SCT TONE IF ORIGINATING IN BELL MODE.	0=OFF 1=ON	0=DATA 1=TX DTMF	4 BIT CODE FOR 1 OF 16 DUAL TONE COMBINATIONS. IF TRANSMIT DTMF BIT IS SET DTMF = 1	0=NORMAL 1=ALLOWS V.23 or BELL 202 FULL DUPLEX OPERATION		
CONTROL REGISTER 3 CR3	101				RECEIVE ENABLE BOOST	TRANSMIT ATTEN. 3	TRANSMIT ATTEN. 2	TRANSMIT ATTEN. 1	TRANSMIT ATTEN. 0
					0=NO BOOST 1=12 dB BOOST	0000-1111 SETS TRANSMIT ATTENUATOR 16 dB RANGE DEFAULT=0100=-10dBm			
ID REGISTER ID	110	ID	ID	ID	ID				

00XX=73K212, 322, 321
01XX=73K221, 302
10XX=73K222
1100=73K224
1110=73K324
1101=73K312

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CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	SPEED SELECT		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects answer mode in V.21 or Bell 103 (transmit in high band, receive in low band, or at 1200/1600 bit/s mode, receive at 1200/600 bit/s and transmit at 75/150 bit/s).
		1	Selects originate mode in V.21 or Bell 103 (transmit in low band, receive in high band) ,or at 1200/600 bit/s mode, receive at 75/150 bit/s and transmit at 1200/600 bit/s. If in V.23/ Bell 202 and D2 of TR=1, selects full duplex operation in 4-wire configuration.
			Note: This bit works with TR bit D0 to program special tones detected in Tone Register. See detect and tone registers.
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA.
			Note: Answer tone and DTMF transmit control require transmit enable.
D5, D4,D3, D2	Transmit Mode	D5 D4 D3 D2	
		0 0 0 0	Selects power down mode. All functions disabled except digital interface.
		1 0 0 0	Selects Bell 103 or 202.
		1 1 0 0	Selects CCITT V.23 or V.21.
		1 1 1 0	Selects CCITT V.23 MC Half Speed.
D6	Unused	0	Not used; must be written as a "0."
D7	Modulation Option	0	CCITT V.23 or Bell 103.
		1	CCITT V.21 or Bell 202.

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	ADD PH. EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D1, D0	Test Mode	D1 D0	
		0 0	Selects normal operating mode.
		0 1	Analog loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the transmitter. To squelch the TXA pin, transmit enable must be forced low.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit data from TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, CR3 except for D2 bit, Tone) are reset to zero. CR3 bit D2 is set to one. The output of the clock pin will be set to the crystal frequency.
D3	CLK Control (Clock Control)	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 19.2 kHz (Bell103) or 15.36 kHz(V.21, V.23, Bell 202).
D4	Add Ph. Eq.	0	Selects normal equalization.
		1	In V.23 or Bell 202 mode, additional phase equalization is added in series with the main channel filters.
D5	Enable Detect Interrupt	0	Disables interrupt at $\overline{INT}$ pin. All interrupts are normally disabled in power down modes.
		1	Enables $\overline{INT}$ output. An interrupt will be generated with a change in status of DR bits D1-D3. The special tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode.
D7, D6	Transmit Pattern	D7 D6	
		0 0	Selects normal data transmission as controlled by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

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DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010			RECEIVE DATA		CARR. DETECT	SPECIAL TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Long Loop	0	Indicates normal received signal.
		1	Indicates low received signal level.
D1	Call Progress Detect	0	No call progress tone detected.
		1	Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the normal 350 to 620 Hz call progress band.
D2	Special Tone Detect	0	No special tone detected as programmed by CR0 bit D0 and Tone Register bit D0.
		1	The tone is selected by bits in CR0 and TR.

Frequency (Hz)	D0 of TR	D4 of CR0	D0 of CR0	Mode
980	0	1	0	V.21
1650	0	1	1	V.21
390	0	1	1	V.23
1300	0	1	0	V.23
1300	1	1	0	V.21 or V.23
2100	1	1	1	V.21
1270	1	0	0	103
2225	1	0	1	103
387	1	0	1	202
1200	1	0	0	202
900	0	0	0	202
2225	0	0	1	103

D3	Carrier Detect	0	No carrier detected in the receive channel.
		1	Indicated carrier has been detected in the received channel.
D4	-	-	Not used.
D5	Receive Data	-	Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6, D7	-	-	Not used.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ V.23 FDX 202 FDX	DTMF 1	DTMF 0/ TONE SELECT

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Tone Select		In CCITT mode, the Tone detected in D2 bit of TR is Mark of FSK selected if this bit is 0. 2100 Hz if this bit is 1 and originating, 1300 Hz if this bit is 1 and answering. In Bell mode, the Tone detected in D2 bit of TR is 2225 Hz if this bit is 0 and originating 900 Hz (SCT) if this bit is 0 and answering Mark of FSK selected if this bit is 1.
D3, D2, D1, D0	DTMF 3, 2, 1, 0	D3 D2 D1 D0 0 0 0 0 - 1 1 1 1	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) is set. Tone encoding is shown below:

KEYBOARD EQUIVALENT	DTMF CODE D3	D2	D1	D0	TONES LOW	HIGH
1	0	0	0	1	697	1209
2	0	0	1	0	697	1336
3	0	0	1	1	697	1477
4	0	1	0	0	770	1209
5	0	1	0	1	770	1336
6	0	1	1	0	770	1477
7	0	1	1	1	852	1209
8	1	0	0	0	852	1336
9	1	0	0	1	852	1477
0	1	0	1	0	941	1336
*	1	0	1	1	941	1209
#	1	1	0	0	941	1477
A	1	1	0	1	697	1633
B	1	1	1	0	770	1633
C	1	1	1	1	852	1633
D	0	0	0	0	941	1633

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TONE REGISTER (Continued)

BIT NO.	NAME	CONDITION	DESCRIPTION
D2	V.23/ Bell 202 FDX	0	Normal Operation
		1	Enables V.23 or Bell 202 full-duplex operation if D4=0. A 4-wire configuration is required in this mode.
D4	TX DTMF Transmit DTMF	0	Disabled DTMF.
		1	Activates DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions.
D5	TX ANS (Transmit Answer tone)	0	Disables answer tone generator.
		1	Enables answer tone generator. A 2100 Hz or 2225 Hz answer tone will be transmitted continuously when the transmit enable bit is set. If TR: D0 = 0, a 2225 Hz tone will be generated. If TR: D0 = 1, a 2100 Hz tone will be generated. The device must be in answer mode.
D6	TX Calling Tone/ SCT (Soft Carrier Turn-Off)Tone	0	Disables calling or SCT tone generator.
		1	Transmit calling tone if originating in CCITT mode. Transmit SCT tone if originating in Bell mode. Transmits neither if answering.
D7	RXD Output Control	0	Enables RXD pin. Receive data will be output on RXD.
		1	Disables RXD pin.The RXD pin reverts to a high impedance with internal weak pull-up resistor.

CONTROL REGISTER 3

				D4	D3	D2	D1	D0
CR3 101				RECEIVE ENABLE BOOST	TRANSMIT ATTEN. 3	TRANSMIT ATTEN. 2	TRANSMIT ATTEN. 1	TRANSMIT ATTEN. 0

BIT NO.	NAME	CONDITION	DESCRIPTION
		D3 D2 D1 D0	
D3, D2 D1, D0	Transmit Attenuator	0 0 0 0- 1 1 1 1	Sets the attenuation level of the transmitted signal in 1 dB steps. The default (D3-D0 = 0100) is for a transmit level of -10 dBm0 at the line with the recommended hybrid transmit gain. The total range is 16 dB.
D4	Receive Gain Boost	0	12 dB receive front end boost is not used.
		1	Boost is in the path. This boost does not change reference levels. It is used to extend dynamic range by compensating for internally generated noise when receiving weak signals. The receive level detect signal and knowledge of the hybrid and transmit attenuator setting will determine when boost should be enabled.

ID REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
ID 110	ID 3	ID 2	ID 1	ID 0				

BIT NO.	NAME	CONDITION	DESCRIPTION
D7, D6	Device Identification Signature	D7 D6 D5 D4	Indicates Device:
		0 0 X X	SSI 73K212(L) or 73K322L or 73K321
		0 1 X X	SSI 73K221(L) or 73K302L
		1 0 X X	SSI 73K222(L)
		1 1 0 0	SSI 73K224L
		1 1 0 1	SSI 73K312L
		1 1 1 0	SSI 73K324L

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above absolute maximum ratings may permanently damage the device.

PARAMETER	RATING	UNIT
VDD Supply Voltage	7	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Applied Voltage	-0.3 to VDD + 0.3	V

Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD Supply voltage		4.5		5.5	V
Digital Pins					
VIH, Input High Voltage					
Reset, XTL1, XTL2		3.0		VDD	V
All other inputs		2.0		VDD	V
VIL, Input Low Voltage		0		0.8	V
IOH, Output High Current		-0.4			mA
IOL, Output Low Current				1.6	mA
TA, Operating Free-Air Temperature		-40		+85	°C

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RECOMMENDED OPERATING CONDITIONS (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
External Components*					
VREF Bypass Capacitor	(External to GND)	0.1			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.9		2.1	MΩ
ISET Bypass Capacitor	(ISET pin to GND)	0.1			µF
VDD Bypass Capacitor	(External to GND)	0.1			µF
*Refer to Application section for placement.					

DC ELECTRICAL CHARACTERISTICS
(TA = -40°C to 85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
IDD, Supply Current	CLK = 11.0592 MHz				
IDDA, Active	ISET Resistor = 2 MΩ			10	mA
IDD1, Power-down	CLK = 11.0592 MHz, ISET = GND			3	mA
IDD2, Power-down	CLK = 19.200 KHz, ISET = GND			2	mA
Digital Inputs					
IIH, Input High Current	VI = VIH Max			100	µA
IIL, Input Low Current	VI = VIL Min	-200			µA
Reset Pull-down Current	Reset = VDD	1		50	µA
Digital Outputs					
VOH, Output High Voltage	IO = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO = 1.6 mA			0.4	V
Capacitance					
Inputs	Capitance, all Digital Input pins			10	pF
XTL1 Load Capacitor	Depends on crystal		39		pF
XTL2 Load Capacitor	Depends on crystal		15		pF
CLK	Maximum Capacitive Load			15	pF

DYNAMIC CHARACTERISTICS AND TIMING
(TA = -40°C to +85°C, VDD = Recommended range unless otherwise noted.)

NOTE: The following parameters expressed in dBm0 refer to the following definition:

0 dB loss in the Transmit path to the line.

2 dB gain in the Receive path from the line.

Refer to the Basic Box Modem diagram in the Applications section for the DAA design.

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
FSK Modulator					
Output Freq. Error	CLK = 11.0592 MHz	-0.38		+0.38	%
Transmit Level	Transmit Dotting Pattern	-11		-9	dBm0
Harmonic Distortion in 700-2900 Hz band	THD in the alternate band FSK		-60	-50	dB
Output Bias Distortion	Transmit Dotting Pattern in ALB @ RXD		±5		%
Total Output Jitter	Random Input in ALB @ RXD	-15		+15	%
DTMF Generator	**TR bit D4=1, CRO bit D1 = 1**				
Freq. Accuracy		-0.25		+0.25	%
Output Amplitude	Low Band	-10		-8	dBm0
	High Band	-8		-6	dBm0
Twist	High-Band to Low-Band, as above	1.0	2.0	3.0	dB
Long Loop Detect	Not valid for Bell 202 V.23 back channel	-38		-28	dBm0
Dynamic Range			45		dB
Call Progress Detector	**Test signal is a 460 Hz sinusoid**				
Detect Level		-39		0	dBm0
Reject Level				-45	dBm0
Delay Time				35	ms
Hold Time				35	ms
Hysteresis		2			dB
Carrier Detect	**For a sinusoid at freq. = (Mark + Space)/2**				
Threshold		-48		-43	dBm0
Delay Time					
V.21		10	15	20	ms
103		8	15	20	ms
V.23 Main Channel RCV		6	10	12	ms
202 Main Channel RCV		6	8	12	ms
202, V.23 Back Channel		25	30	40	ms
Hold Time					
V.21		6	10	20	ms
103		6	12	20	ms
202, V.23 Main Channel		3	6	8	ms
202, V.23 Back Channel		10	15	25	ms
Hysteresis		2			dB

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DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Special Tone Detectors					
Detect Level	See definitions for TR bit D0 mode	-49		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 step				
2100 Hz V.21 CCITT Answer Tone		10		25	ms
1300 Hz V.23 Mark		10		25	ms
390 Hz V.23 Back Channel Mark		20		65	ms
980 or 1650 Hz V.21 Marks		10		25	ms
2225 Hz Bell Answer Tone		10		35	ms
900 Hz SCT tone	Assumes that SCT follows data in a phase continuous manner	4		10	ms
1200 Hz Bell 202 Main Channel Mark		10		25	ms
387 Hz Bell 202 Back Channel Mark		20		65	ms
1270 or 2225 Hz Bell 103 Marks		10		30	ms
Hold Time	-30 dBm0 to -70 dBm0 step				
2100 Hz V.21 CCITT Answer Tone		4		15	ms
1300 Hz V.23 Mark		3		10	ms
390 Hz V.23 Back Channel Mark		10		25	ms
980 or 1650 Hz V.21 Marks		5		15	ms
2225 Hz Bell Answer Tone		4		15	ms
900 Hz SCT tone		1		10	ms
1200 Hz Bell 202 Main Channel Mark		3		10	ms
387 Hz Bell 202 Back Channel Mark		10		25	ms
1270 or 2225 Hz Bell 103 Marks		4		15	ms
Hysteresis		2			dB
Detect Freq. Range	Any Special Tone	-3		+3	%

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Output Smoothing Filter					
Output load	TXA pin; FSK Single Tone out for THD = -50 dB in .3 to 3.4 kHz	10			kΩ
Out of Band Energy	Frequency >12 kHz in all modes			-60	dBm0
Output Impedance	TXA pin		200	300	Ω
Clock Noise	TXA pin: V.21 @ 61.44 kHz 103 @ 76.8 kHz V.23 or 202 MC @ 122.88 kHz V.23 or 202B @ 15.36 kHz		0.2	0.4	mVrms
Timing (Refer to Timing Diagrams)					
Parallel Mode					
TAL	$\overline{CS}$/Addr. setup before ALE	25			ns
TLA	$\overline{CS}$/Addr. hold after latch	20			ns
TLC	Latch to $\overline{RD}$/$\overline{WR}$ control	30			ns
TCL	$\overline{RD}$/$\overline{WR}$ Control to latch	-5			ns
TRD	Data out from $\overline{RD}$	0		140	ns
TLL	ALE width	30			ns
TRDF	Data float after READ	0		5	ns
TRW	READ width	200		25000	ns
TWW	WRITE width	140		25000	ns
TDW	Data setup before WRITE	40			ns
TWD	Data hold after WRITE	10			ns
Serial Mode					
TCKDR	Data out after CLK			300	ns
TCKW	WRITE after CLK	200			ns
TDCK	Data setup before CLK	150			ns
TAW	Address setup before control[1]	50			ns
TWA	Address hold after control[1]	50			ns
TWW	Write width	200			ns
TCKDW	Data hold after write	250			ns
TAR	Address setup before control[2]	0			ns
TRA	Address hold after control[2]	400			ns
TRD	Data out from $\overline{RD}$			350	ns
TRDF	Data float after READ	0		100	ns

[1] Control for setup is the falling edge of $\overline{WR}$.
Control for hold is the falling edge of $\overline{WR}$.

[2] Control for setup is the falling edge of $\overline{RD}$ or EXCLK.
Control for hold is the falling edge of $\overline{RD}$ or EXCLK.

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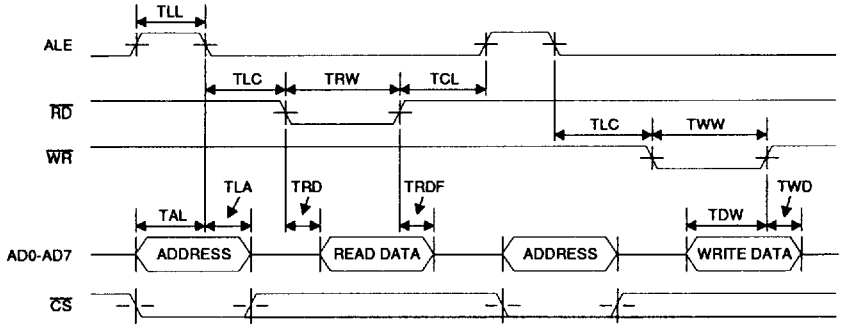
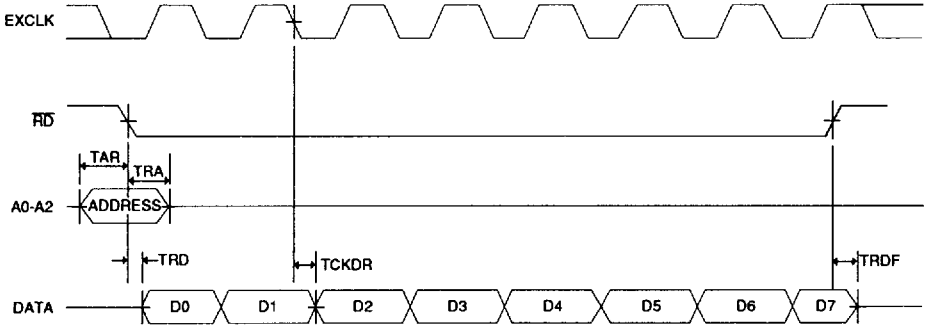
TIMING DIAGRAMS

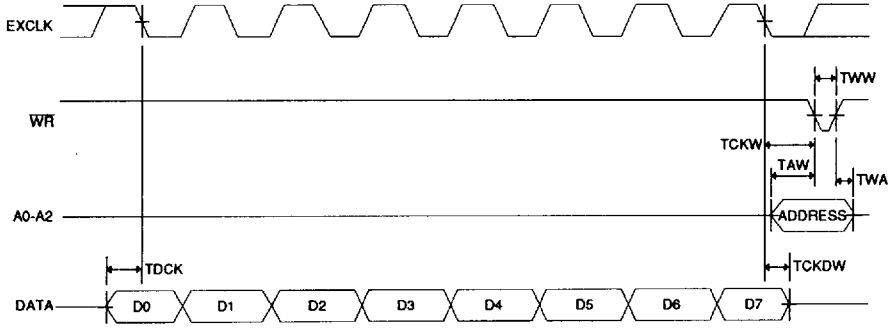
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show basic circuit diagrams for K-Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes. Two typical DAA arrangements are shown: one for a split ±5 or ±12 volt design and one for a single 5 volt design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available with two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available. The parallel versions may also be used in the serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, command data to the modem is sent over the same line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

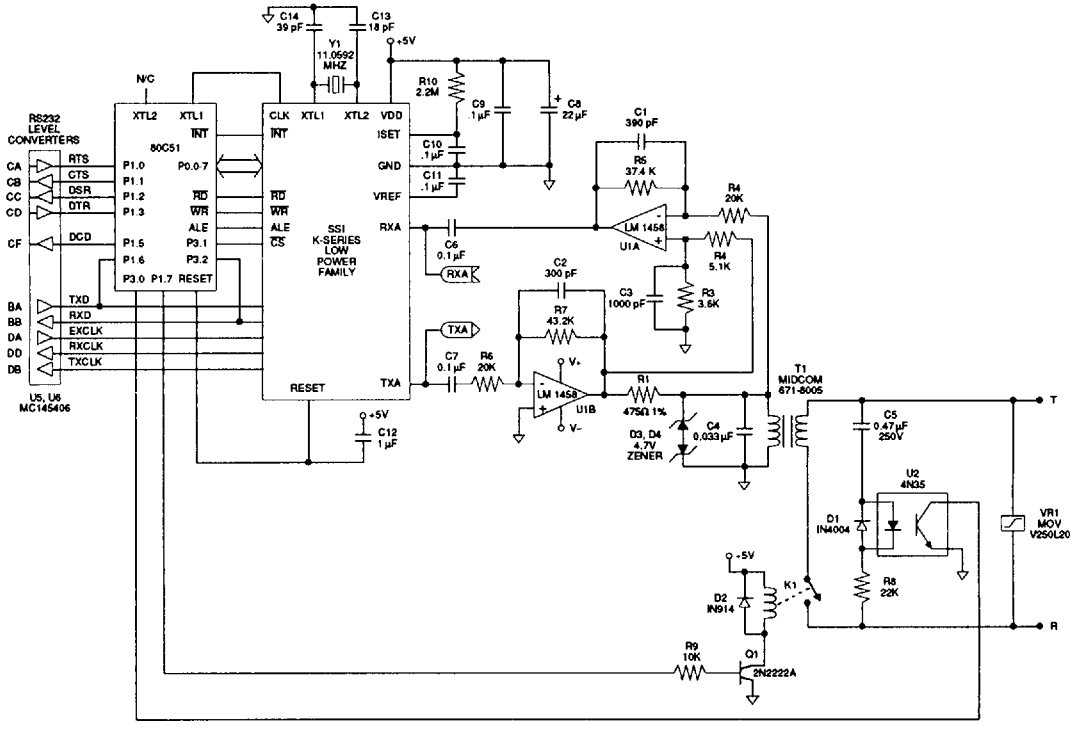


FIGURE 1: Basic Box Modem with Dual-Supply Hybrid

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DIRECT ACCESS ARRANGEMENT (DAA)

The DAAs shown are two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal common mode.

The single-supply DAA is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. The DAA (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5 volt supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (op-amp C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the summing point of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

Silicon Systems' 1-chip modem products include all basic modem functions on a single IC, accessible from a standard bus interface. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals. Unlike digital logic circuitry, however, modem designs must properly contend with precise frequency tolerances and very low level analog signals, to insure acceptable performance. Using good analog circuit

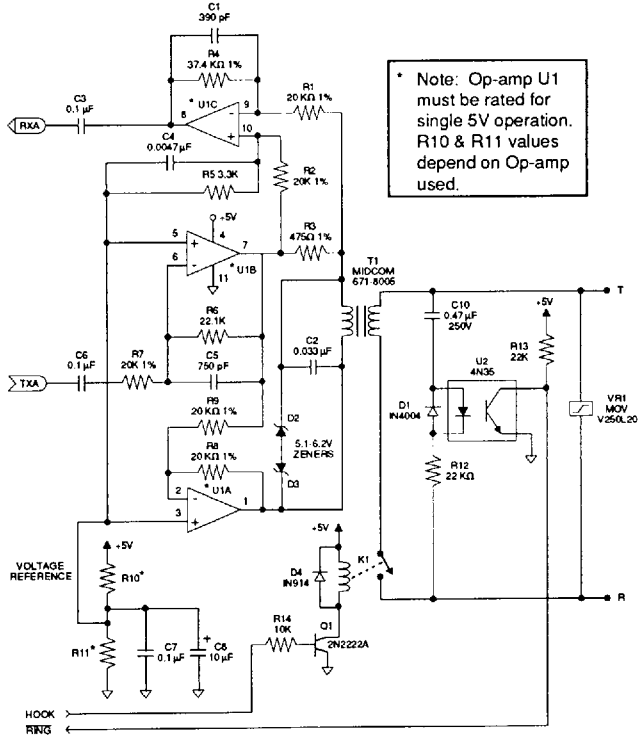

FIGURE 2: Single 5V DAA Version

design practices will generally result in a sound design. Following are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this frequency be maintained to within ±0.01% accuracy.

In order for a parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 10 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor between VDD and ground is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the DAA and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the analog supplies to avoid ground loops. The K–Series modem IC's should have both high frequency and low frequency bypassing as near to the package as possible.

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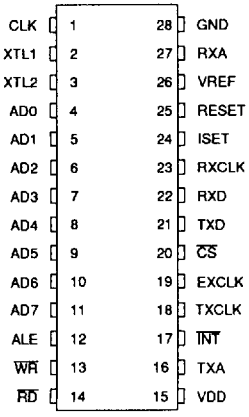
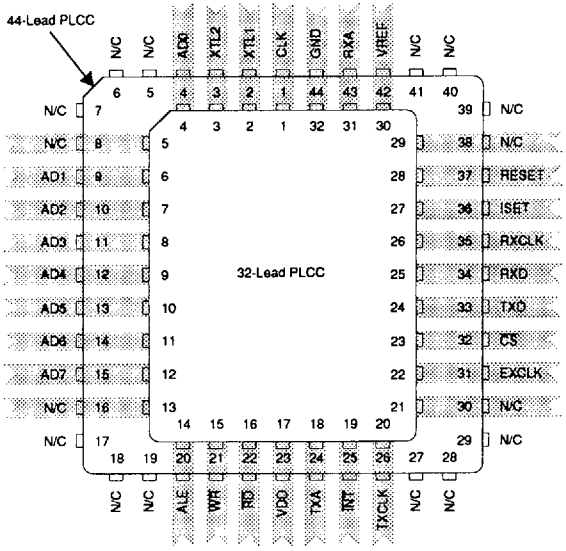
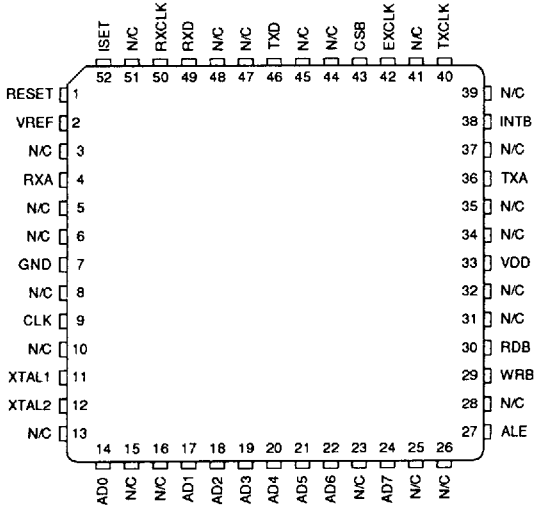
PACKAGE PIN DESIGNATIONS
(Top View)



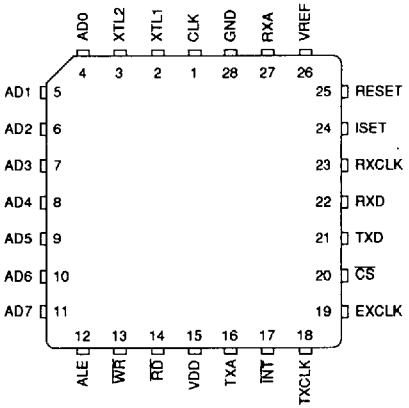
600-Mil
28-Pin DIP



32, 44-Pin PLCC



52-Lead QFP



28-Pin PLCC

CAUTION: Use handling procedures necessary for a static sensitive component.

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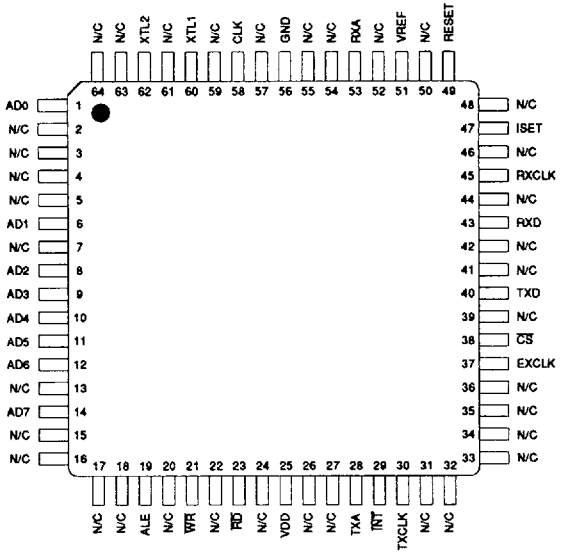

64-Lead TQFP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K312L with Serial Bus Interface		
SSI 73K312L with Parallel Bus Interface		
28-Pin Plastic Dual-In-Line	73K312L-IP	73K312L-IP
28-Pin Plastic Leaded Chip Carrier	73K312L-28IH	73K312L-28IH
32-Pin Plastic Leaded Chip Carrier	73K312L-32IH	73K312L-32IH
44-Pin Plastic Leaded Chip Carrier	73K312L-IH	73K312L-IH
52-Lead Quad Flat Pack Package	73K312L-IG	73K312L-IG
64-Lead Thin Quad Flat Pack Package	73K312L-IGT	73K312L-IGT

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 573-6000, FAX: (714) 573-6914