

54AC169 • 54ACT169 4-Stage Synchronous Bidirectional Counter

General Description

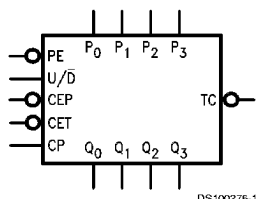
The 'AC/'ACT169 is fully synchronous 4-stage up/down counter. The 'AC/'ACT169 is a modulo-16 binary counter. It features a preset capability for programmable operation, carry lookahead for easy cascading and a U/D input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the Clock.

- Synchronous counting and loading
- Built-In lookahead carry capability
- Presettable for programmable operation
- Outputs source/sink 24 mA
- 'ACT has TTL-compatible inputs
- Standard Microcircuit Drawing (SMD) 5962-91603

Features

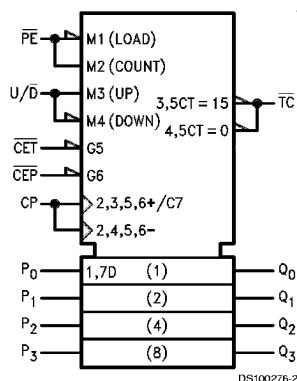
- I_{CC} reduced by 50%

Logic Symbols



Pin Names	Description
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input
P ₀ -P ₃	Parallel Data Inputs
PE	Parallel Enable Input
U/D	Up-Down Count Control Input
Q ₀ -Q ₃	Flip-Flop Outputs
TC	Terminal Count Output

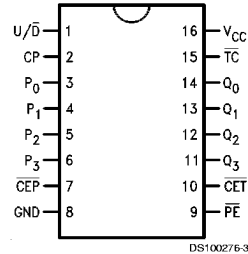
IEEE/IEC



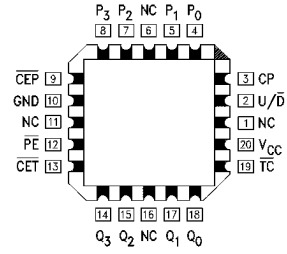
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Connection Diagrams

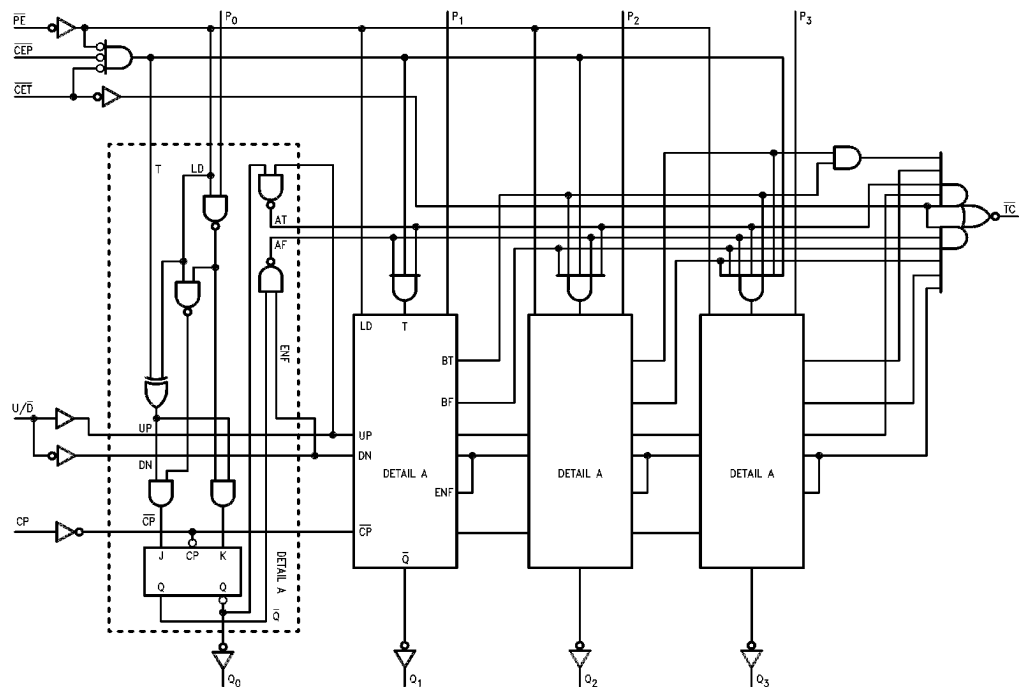
Pin Assignment
for DIP and Flatpak



Pin Assignment
for LCC



Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

The 'AC/ACT169 uses edge-triggered J-K-type flip-flops and have no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When PE is LOW, the

data on the P₀–P₃ inputs enters the flip-flops on the next rising edge of the Clock. In order for counting to occur, both CEP and CET must be LOW and PE must be HIGH; the U/D input then determines the direction of counting. The Terminal Count (TC) output is normally HIGH and goes LOW, provided that CET is LOW, when a counter reaches zero in the Count Down mode or reaches 15 in the Count Up mode. The TC output state is not a function of the Count Enable Parallel (CEP) input level. If an illegal state occurs, the 'AC169 will return to the legitimate sequence within two counts. Since

Functional Description (Continued)

the $\overline{TC}$ signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on $\overline{TC}$. For this reason the use of $\overline{TC}$ as a clock signal is not recommended (see logic equations below).

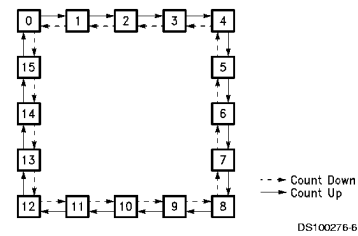
1. Count Enable = $\overline{CEP} \cdot \overline{CET} \cdot \overline{PE}$
2. Up: $\overline{TC} = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (Up) \cdot \overline{CET}$
3. Down: $\overline{TC} = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot (Down) \cdot \overline{CET}$

Mode Select Table

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	$U/\overline{D}$	Action on Rising Clock Edge
L	X	X	X	Load (P_n to Q_n)
H	L	L	H	Count Up (Increment)
H	L	L	L	Count Down (Decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagrams



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	–0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	–20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	–0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	–20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	–0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	–65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
54AC/ACT	–55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	54AC	Units	Conditions
			$T_A =$ –55°C to +125°C		
			Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage	3.0	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	3.15		
		5.5	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	1.35		
		5.5	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.9	V	$I_{OUT} = -50 \mu A$
		4.5	4.4		
		5.5	5.4		
		3.0	2.4	V	(Note 2) $V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -12 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA}$
		4.5	3.7		
		5.5	4.7		
V_{OL}	Maximum Low Level Output Voltage	3.0	0.1	V	$I_{OUT} = 50 \mu A$
		4.5	0.1		
		5.5	0.1		
		3.0	0.50	V	(Note 2) $V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA}$
		4.5	0.50		
		5.5	0.50		
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	μA	$V_I = V_{CC}, \text{GND}$

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V _{CC} (V)	54AC	Units	Conditions
			T _A = –55°C to +125°C		
			Guaranteed Limits		
I _{OLD}	Minimum Dynamic Output Current (Note 3)	5.5	50	mA	V _{OLD} = 1.65V Max
I _{OHD}		5.5	–50	mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5	80.0	μA	V _{IN} = V _{CC} or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V _{CC} (V)	54ACT	Units	Conditions
			T _A = –55°C to +125°C		
			Guaranteed Limits		
V _{IH}	Minimum High Level Input Voltage	4.5	2.0	V	V _{OUT} = 0.1V or V _{CC} – 0.1V
		5.5	2.0		
V _{IL}	Maximum Low Level Input Voltage	4.5	0.8	V	V _{OUT} = 0.1V or V _{CC} – 0.1V
		5.5	0.8		
V _{OH}	Minimum High Level Output Voltage	4.5	4.4	V	I _{OUT} = –50 μA
		5.5	5.4		
		4.5	3.70		(Note 5) V _{IN} = V _{IL} or V _{IH} I _{OH} = –24 mA
V _{OL}	Maximum Low Level Output Voltage	5.5	4.70	V	I _{OH} = –24 mA
		4.5	0.1		
		5.5	0.1		
I _{IN}	Maximum Input Leakage Current	4.5	0.50	V	(Note 5) V _{IN} = V _{IL} or V _{IH} I _{OL} = 24 mA
		5.5	0.50		
		4.5	0.1		
I _{CT}	Maximum I _{CC} /Input	5.5	1.6	mA	V _I = V _{CC} – 2.1V
I _{OLD}	Minimum Dynamic Output Current (Note 6)	5.5	50	mA	V _{OLD} = 1.65V Max
I _{OHD}		5.5	–50	mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5	80.0	μA	V _{IN} = V _{CC} or GND

Note 5: All outputs loaded; thresholds on input associated with output under test.

Note 6: Maximum test duration 2.0 ms, one output loaded at a time.

Note 7: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V) (Note 8)	54AC		Units	Fig. No.
			T _A = -55°C to +125°C C _L = 50 pF			
			Min	Max		
f _{max}	Maximum Clock Frequency	3.3 5.0	55 75		MHz	
t _{PLH}	Propagation Delay CP to Q _n ($\overline{PE}$ HIGH or LOW)	3.3 5.0	1.0 1.5	15.0 12.0	ns	
t _{PHL}	Propagation Delay CP to Q _n ($\overline{PE}$ HIGH or LOW)	3.3 5.0	1.0 1.5	16.5 13.0	ns	
t _{PLH}	Propagation Delay CP to $\overline{TC}$	3.3 5.0	3.0 3.0	22.0 16.0	ns	
t _{PHL}	Propagation Delay CP to $\overline{TC}$	3.3 5.0	3.0 3.0	22.0 16.0	ns	
t _{PLH}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	3.3 5.0	1.0 1.5	18.5 13.0	ns	
t _{PHL}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	3.3 5.0	1.0 1.5	16.0 11.0	ns	
t _{PLH}	Propagation Delay U/ $\overline{D}$ to $\overline{TC}$	3.3 5.0	1.0 1.5	18.5 13.0	ns	
t _{PHL}	Propagation Delay U/ $\overline{D}$ to $\overline{TC}$	3.3 5.0	1.0 1.5	16.5 12.0	ns	

Note 8: Voltage Range 3.3 is 3.3V ± 0.3 V

Voltage Range 5.0 is 5.0V ± 0.5 V

AC Operating Requirements

Symbol	Parameter	V _{CC} (V) (Note 9)	54AC	Units	Fig. No.
			T _A = -55°C to +125°C C _L = 50 pF		
			Guaranteed Minimum		
t _s	Setup Time, HIGH or LOW P _n to CP	3.3	7.0	ns	
		5.0	4.5		
t _h	Hold Time, HIGH or LOW P _n to CP	3.3	2.0	ns	
		5.0	2.5		
t _s	Setup Time, HIGH or LOW CEP to CP	3.3	13.5	ns	
		5.0	9.0		
t _h	Hold Time, HIGH or LOW CEP to CP	3.3	0.5	ns	
		5.0	2.5		
t _s	Setup Time, HIGH or LOW CET to CP	3.3	13.5	ns	
		5.0	9.0		

AC Operating Requirements (Continued)

Symbol	Parameter	V _{CC} (V) (Note 9)	54AC	Units	Fig. No.
			T _A = -55°C to +125°C C _L = 50 pF		
			Guaranteed Minimum		
t _h	Hold Time, HIGH or LOW $\overline{CET}$ to CP	3.3 5.0	0.5 2.5	ns	
t _s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	8.5 6.5	ns	
t _h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	0.5 2.0	ns	
t _s	Setup Time, HIGH or LOW U/ $\overline{D}$ to CP	3.3 5.0	13.0 9.0	ns	
t _h	Hold Time, HIGH or LOW U/ $\overline{D}$ to CP	3.3 5.0	0.5 2.0	ns	
t _w	CP Pulse Width, HIGH or LOW	3.3 5.0	5.0 5.0	ns	

Note 9: Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V) (Note 10)	54ACT		Units	Fig. No.
			T _A = -55°C to +125°C C _L = 50 pF			
			Min	Max		
f _{max}	Maximum Clock Frequency	5.0	75		MHz	
t _{PLH}	Propagation Delay CP to Q _n ($\overline{PE}$ HIGH or LOW)	5.0	1.5	12.5	ns	
t _{PHL}	Propagation Delay CP to Q _n ($\overline{PE}$ HIGH or LOW)	5.0	1.5	12.5	ns	
t _{PLH}	Propagation Delay CP to $\overline{TC}$	5.0	1.5	16.5	ns	
t _{PHL}	Propagation Delay CP to $\overline{TC}$	5.0	1.5	16.5	ns	
t _{PLH}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	5.0	1.5	13.5	ns	
t _{PHL}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	5.0	1.5	13.5	ns	
t _{PLH}	Propagation Delay U/ $\overline{D}$ to $\overline{TC}$	5.0	1.5	14.5	ns	
t _{PHL}	Propagation Delay U/ $\overline{D}$ to $\overline{TC}$	5.0	1.5	14.5	ns	

AC Electrical Characteristics (Continued)

Note 10: Voltage Range 5.0 is 5.0V $\pm 0.5V$

AC Operating Requirements

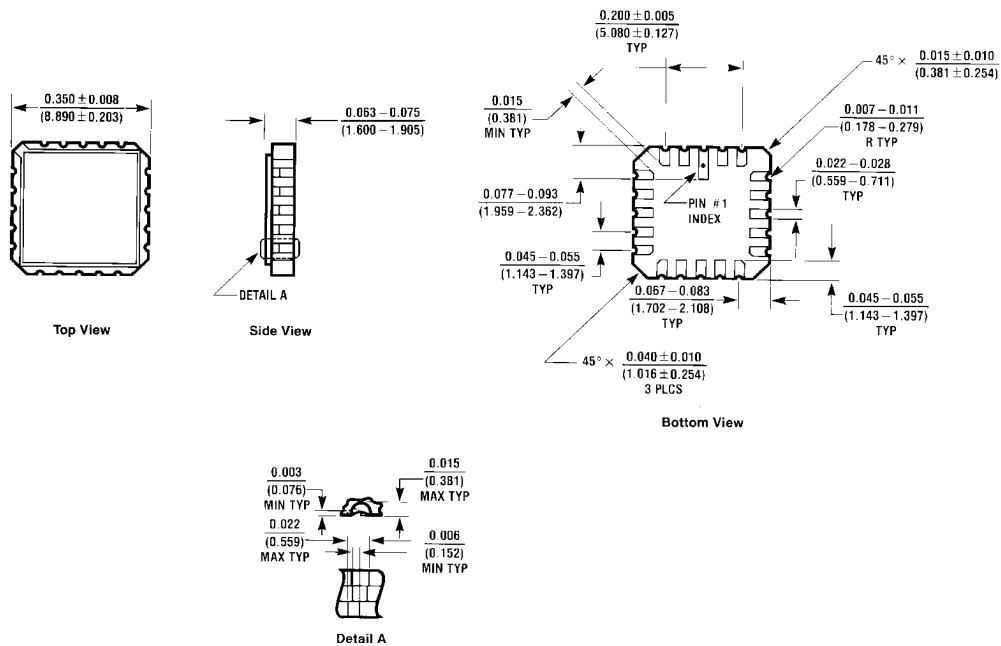
Symbol	Parameter	V _{CC} (V) (Note 11)	54ACT T _A = -55° C to +125° C C _L = 50 pF	Units	Fig. No.
			Guaranteed Minimum		
t _s	Setup Time, HIGH or LOW P _n to CP	5.0	4.5	ns	
t _h	Hold Time, HIGH or LOW P _n to CP	5.0	2.5	ns	
t _s	Setup Time, HIGH or LOW $\overline{CEP}$ to CP	5.0	9.0	ns	
t _h	Hold Time, HIGH or LOW $\overline{CEP}$ to CP	5.0	2.5	ns	
t _s	Setup Time, HIGH or LOW $\overline{CET}$ to CP	5.0	9.0	ns	
t _h	Hold Time, HIGH or LOW $\overline{CET}$ to CP	5.0	2.5	ns	
t _s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	5.0	6.5	ns	
t _h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	5.0	2.0	ns	
t _s	Setup Time, HIGH or LOW U/ $\overline{D}$ to CP	5.0	9.0	ns	
t _h	Hold Time, HIGH or LOW U/ $\overline{D}$ to $\overline{CP}$	5.0	2.0	ns	
t _w	CP Pulse Width, HIGH or LOW	5.0	5.0	ns	

Note 11: Voltage Range 5.0 is 5.0V $\pm 0.5V$

Capacitance

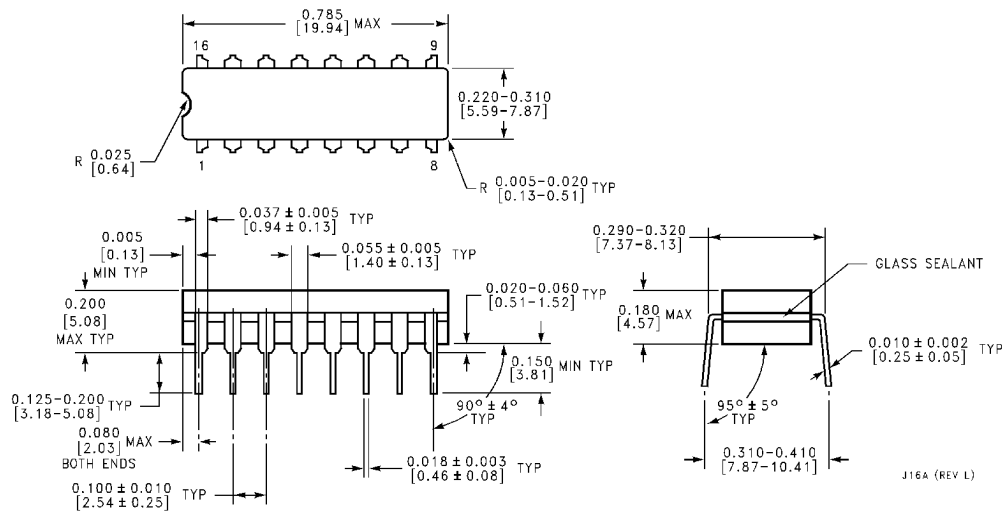
Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = Open
C _{PD}	Power Dissipation Capacitance	60.0	pF	V _{CC} = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted



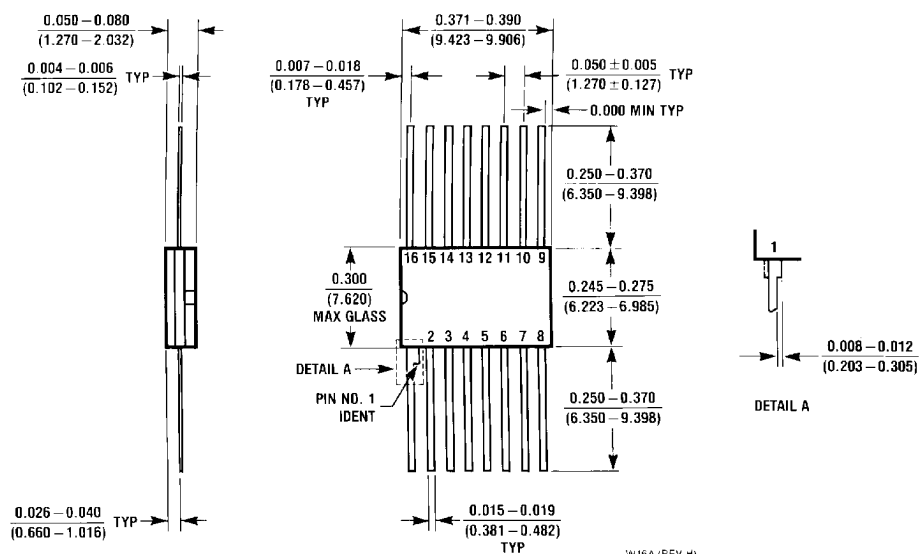
20-Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

E20A (REV D)



16-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A

J16A (REV L)

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

16-Lead Ceramic Flatpak (F)
NS Package Number W16A

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