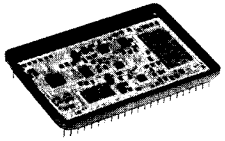
ADC-00110 AND ADC-00111

12 BIT 10 MHz T/H + A/D HYBRID
HIGH SPEED, SMALL SIZE, MIL-SPEC



DESCRIPTION

The ADC-00110 is a 12 bit, 10 MHz track/hold and A/D converter hybrid packaged in a 46 pin plug-in.

Containing T/H,A/D converter,data registers,tri-state output buffers,and timing circuits, the ADC-00110 is the fastest and smallest digitizer of its kind. The ADC-00110 operates over a temperature range of -55°C to +125°C and military processing is available.

The ADC-00110 is implemented with a 2-step A/D conversion algorithm. A number of factors contributed to achieving the ADC-00110's technical breakthroughs in speed and size.

Foremost among them are proprietary ICs for the DAC, the conversion logic, and the gain amp functions. In addition, judicious use of thin film and thick film hybrid technology resulted in minimum layout area.

With its high speed, small package and wide operating temperature range, the ADC-00110 is ideal for the most demanding military and industrial data conversion applications. Typical of these applications are radar and IR digitizing, vibration and FFT analysis, medical and nuclear instrumentation, and high-speed data acquisition and communications systems.

FEATURES

- *INCLUDES*
  - *TRACK/HOLD*
  - *A/D CONVERTER*
  - *TRI-STATE OUTPUT REGISTERS*
  - *TIMING CIRCUITS*
- *10 MHz WORD RATE*
- *SMALL 46 PIN PLUG-IN HERMETIC HYBRID*
- *INPUT VOLTAGE OPTIONS*
- *-55°C TO +125°C OPERATING TEMPERATURE*

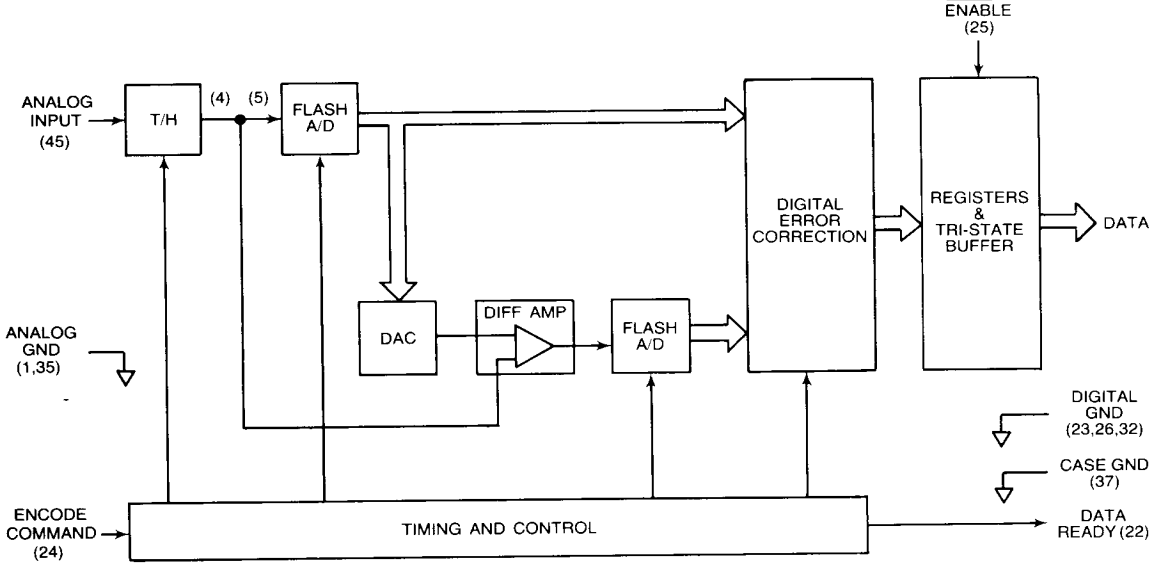


FIGURE 1. ADC-00110 BLOCK DIAGRAM

TABLE 1. ADC-00110 SPECIFICATIONS (T/H and A/D)

Typical values at +25°C case temperature, nominal power supply voltages, and 10 MHz encode rate, unless otherwise noted.

PARAMETER	UNITS	VALUES
Resolution	Bits	12
ACCURACY		
Linearity Error	%FSR	±0.025 typ, ±0.050 max
Linearity Error Tempco	ppm FSR/°C	2 max
Diff Linearity Error	LSB	±1 max
Gain Error	%FSR	±0.5 max
Gain Error Tempco	ppm FSR/°C	50
Offset Error	%FSR	±0.5 max
Offset Error Tempco	ppm FSR/°C	50 max
No Missing Codes		Guaranteed
DYNAMIC CHARACTERISTICS		
Conversion Rate	MHz	DC to 10 min
Pipeline Delay [1]	nsec	2 Encode Commands +80 nsec
Aperture Uncertainty (Jitter)	psec RMS	9 typ, 20max
Aperture Time (Delay)	nsec	6(±3)
Signal to Noise Ratio (SNR) [2]		
5MHz analog input	db	68.5 typ, 64min
1MHz analog input	db	69.5 typ, 65min
100kHz analog input	db	70.5 typ, 66min
Transient Response [3]	nsec	100 max
Overvoltage Recovery [4]	nsec	200 max
Input Bandwidth		
Small Signal, 3dB [5]	MHz	70typ, 50min
Large Signal, 3dB [6]	MHz	40typ, 30min
Total Harmonic Distortion		
5MHz analog input	db below FS	64min
100kHz analog input	db below FS	66min
Two-tone linearity(at input freq.)		
60KHz; 62KHz	db below FS	62 min
2.498MHz; 2.500MHz	db below FS	62 min
4.996M Hz; 4.998MHz	db below FS	60 min
ANALOG INPUT	ADC-	00110 00111
Voltage Range		
(Normal Operation)	V	±2.5 ±1
(Absolute Max)	V	±5 max ±2max
Impedance		
Resistance	Ohms	1M min 50k min
Capacitance	pF	10 10
ENCODE COMMAND INPUT [7] (ADC-00110)		
Logic Levels, TTL Compatible	V	Logic 0 = 0.4 Logic 1 = 2.4
Minimum Pulse Width	nsec	10
Maximum Pulse Width	nsec	Encode Command Period -20 nsec
DIGITAL OUTPUT		
Format	Bits	12 parallel; NRZ
Logic Levels, TTL Compatible	V	Logic 0 = 0.4 Logic 1 = 2.4
Time Skew	nsec	5 max
Coding		Offset binary two's complement
Drive	TTL Loads	3
POWER SUPPLIES (ADC-00110)		
+15 Volt Supply	V	+15 ±5%
Current Drain	mA	80 typ, 120 max
-15 Volt Supply	V	-15 ±5%
Current Drain	mA	80 typ, 125 max
+5 Volt Supply	V	+5 ±5%
Current Drain	mA	300 typ, 400 max
- 5.2 Volt Supply	V	- 5.2 ±5%
Current Drain	mA	600 typ, 700 max
Power Dissipation	W	7.0 typ, 9.25 max
PSRR:		
±15V Supplies	%FSR/%V_S	0.01
+ 5V and -5.2V Supplies	%FSR/%V_S	0.03

TABLE 1. ADC-00110 SPECIFICATIONS (T/H and A/D) (continued)

PARAMETER	UNITS	VALUES
POWER SUPPLIES (ADC-00111)		
+15 Volt Supply	V	+15 ±5%
Current Drain	mA	40 typ, 70 max
-15 Volt Supply	V	-15 ±5%
Current Drain	mA	40 typ, 75 max
+5 Volt Supply	V	+5 ±5%
Current Drain	mA	315 typ, 420 max
- 5.2 Volt Supply	V	- 5.2 ±5%
Current Drain	mA	615 typ, 720 max
Power Dissipation	W	5.9 typ, 8.0 max
PSRR:		
±15V Supplies	%FSR/%V_S	0.01
+ 5V and -5.2V Supplies	%FSR/%V_S	0.03
TEMPERATURE RANGE		
Operating (Case)		
-1 Option	°C	-55 to +125
-3 Option	°C	0 to +70
Storage	°C	-55 to +165

Notes:

(1) Measured from the rising edge of Encode Command to the falling edge of Data Ready; use rising edge to strobe output data into external circuits. See figure 2, timing diagram.
(2) Rms signal to rms noise ratio.
(3) For full-scale step input, 12-bit accuracy attained in specified time.
(4) Recovers to 12-bit accuracy in specified time after 2 x FS input overvoltage.
(5) With analog input 40 dB below FS.
(6) With FS analog input (Large-signal bandwidth flat within 0.2 dB,DC to 5MHz).
(7) Transition from digital 0 to digital 1 initiates encoding.

GENERAL DESCRIPTION

Figure 1 is a functional block diagram of the ADC-00110 sampling A/D converter. Its major elements are a track/hold amplifier, 6-bit and 8-bit flash A/D converters, a 6-bit D/A converter, and a differential amplifier. The remaining functions are timing and control circuits, digital buffers, and registers.

These components implement a straightforward 2-step A/D conversion algorithm. First, the conversion cycle is initiated with the receipt of an Encode Command. This causes the timing circuit to place the track/hold in the HOLD mode, storing the voltage at its analog input. The flash A/D then generates a coarse encode of the sampled voltage. Its 6-bit coarse encode output is stored temporarily in the MSB register. At the same time, the coarse 6-bit word is input to the DAC, which converts it to an analog voltage.

The differential amplifier subtracts the voltage representing the coarse encode from the sampled input, and scales it up to the correct full scale range.

Next, the 8-bit flash A/D converter generates a fine encode of the scaled difference voltage. The fine encode 8-bit word is stored in the LSB register. Finally, the contents of the 6-bit MSB and 8-bit LSB registers are combined in the digital error correction circuit to yield a 12-bit output word. This 12-bit word is stored in the output registers. The encoded digital output is available upon application of an Enable signal to the tri-state output buffer.

Since the ADC-00110 has output storage registers, its digital output is available to the user at all times, except for a short interval when it is being updated. A Data Ready output signal is provided to indicate when the digital output is valid.

Care must be taken when designing with the ADC-00110, to achieve its rated performance. This high-speed sampling A/D converter generates high-frequency power supply and ground currents. For this reason, it is recommended that decoupling

capacitors be used on each power supply line. See the paragraph on Power Supply Decoupling for more detail. High-frequency layout considerations should be kept in mind when designing a printed circuit board for the ADC-00110. Conductor lengths should be kept to a minimum, and a large area ground plane should be used to keep ground impedances as low as possible.

TIMING DIAGRAM

A Typical ADC-00110 timing diagram is shown in figure 2. Note that the Encode Command repeats at 100 nsec intervals with a throughput (pipeline) delay of 280 nsec.

A conversion cycle is initiated by the application of a positive pulse (15 nsec min) to the Encode Command pin. The rising edge of the Encode Command starts the timing cycle. First the internal track/hold is placed in the HOLD mode. The output signal is then delivered to the 6-bit flash A/D converter for a coarse conversion of thee 6 MSBs. The output of the 6-bit flash A/D is also delivered to the D/A whose output is applied to the differential amplifier. The output of the differential amplifier is then delivered to the 8-bit flash A/D converter. Once the 8-bit flash conversion is complete, the internal T/H is returned to the TRACK mode. The output of the 8-bit flash A/D converter along with the original coarse 6-bit word is input to the digital error correction circuit with output to the 12-bit register. The Encode Command input then updates the register to take data.

The idea behind pipelining is that a second Encode is started before the first Encode has completed conversion. Consequently, the input signal is encoded and output data is delivered at a 10MHz rate. The pipeline delay is two Encode periods plus 80 nsec, or 280 nsec, minimum. Since Data Ready stays low for 50 nsec, it is possible to use the Encode Command to enable and continuously take data at a 10M Hz rate, though output data lags analog input by two encode periods plus 80 nsec. Note that data is not valid during the first 5 nsec following the falling edge of Data Ready, but is otherwise valid. The timing diagram also indicates the tri-state propagation delays for both enabling and disabling the latch as 8 nsec typ, and 10 nsec max.

LAYOUT PRECAUTIONS

The ADC-00110 high-speed sampling A/D converter generates high-frequency power supply and ground currents, and is sensitive to coupled signals. High-frequency layout considerations must therefore be kept in mind when designing a printed circuit board for it. All conductor lengths must be kept to a minimum, and a large area ground plane must be used to keep ground impedances as low as possible. Analog inputs and digital outputs must be kept separated from each other to minimize crosstalk. Input and output circuits must be kept as close to the A/D converter package as possible. Likewise, the three analog ground pins must be connected to the digital ground pin as close as possible to the hybrid package, with connection to the case ground pin. While the case ground pin may be left floating it is recommended that the case be tied to system ground in order to minimize ground contributions to noise.

POWER SUPPLY DECOUPLING

Decoupling capacitors are required on each power supply to minimize noise. Figure 5 illustrates the recommended decoupling scheme. Each decoupled line must have a 10 µF or larger tantalum capacitor in parallel with a 0.01 µF ceramic capacitor. All capacitors must be mounted as close as possible to the hybrid package. While the user may use the same power supply for the 5.2V analog and digital supplies, it is recommended that the supply lines to the ADC-00110 be separated at the supply and treated as individual supplies at the board in order to minimize crosstalk. The same applies to the 5V analog and digital supplies. It is further recommended that an inductor, such as the Ferrox Cube Bead model #VK20020/4B be used in the digital supply line to prevent digital switching from being transposed on the analog supply. For instances where the user has a seperate analog and digital supplies: the +5V current drain is approximately 20% digital; and the -5.2V current drain is approximately 50% digital.

OUTPUT CODING

Output coding is illustrated in table 2. The ADC-00110 is TTL compatible and outputs offset binary and two's complement data. Moreover, data is accessed through a tri-state latch. A LOW state input to pin 25, $\overline{\text{Enable}}$, enables output data; input HIGH disables as illustrated in the figure 2.

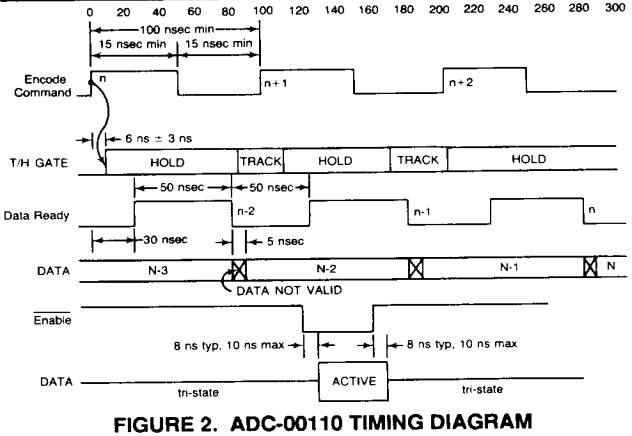


FIGURE 2. ADC-00110 TIMING DIAGRAM

TABLE 2. OUTPUT CODING

INPUT VOLTAGE	BIPOLAR	
	Offset Binary	Two's Complement
−FS	0000 0000 0000	1000 0000 0000
−¾FS	0001 1111 1111	1001 1111 1111
−½FS	0011 1111 1111	1011 1111 1111
−1 LSB	0111 1111 1110	1111 1111 1110
0	0111 1111 1111	1111 1111 1111
+1 LSB	1000 0000 0000	0000 0000 0000
+½FS	1011 1111 1111	0011 1111 1111
+¾FS	1101 1111 1111	0101 1111 1111
+FS−1LSB	1111 1111 1110	0111 1111 1110
+FS	1111 1111 1111	0111 1111 1111
	B1 thru B12	$\overline{\text{B1}}$, B2 thru B12

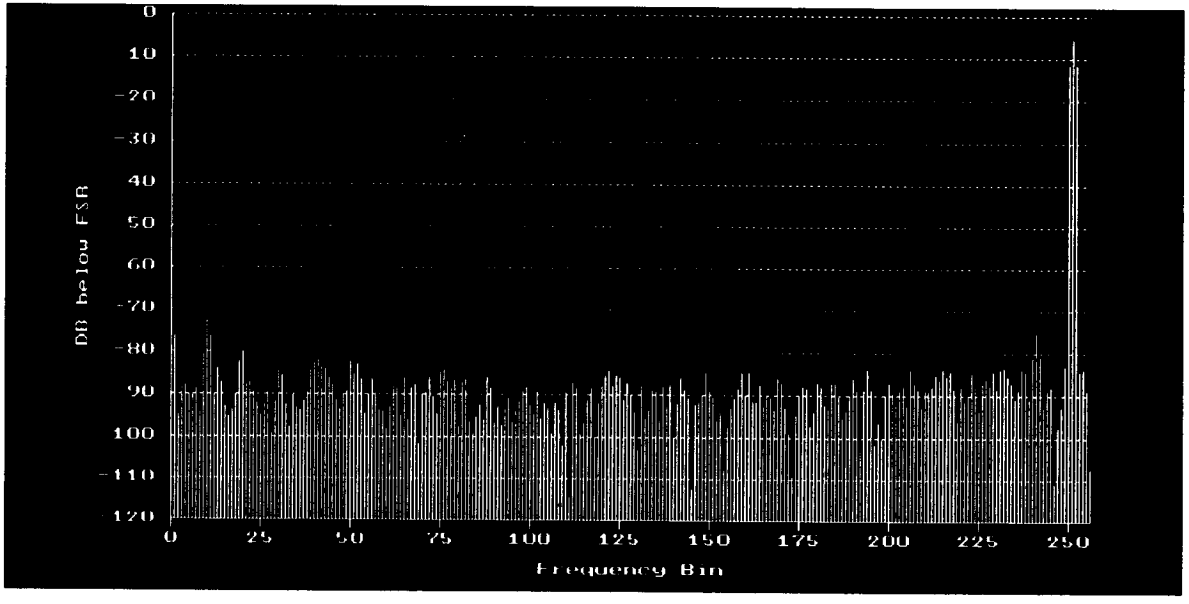
FFT TEST DESCRIPTION

In order to determine the harmonic distortion and signal to noise ratio of the ADC-00110 and ADC-00111, DDC uses some specialized hardware and an FFT analysis program. The details of the method are described below and illustrated in figure 3.

The FFT used is 512 points. The extra points that are taken can be used for either increasing the spectral resolution or for averaging a number of records to minimize the run-to run variation in readings. A single 512 point record typically gives run-to-run variations of as much as 1 db in signal to noise ratio. An 8 record average can decrease this to about 0.2 db. The 512 data samples are windowed using Hanning weighting. An FFT is then performed on the weighted bins. The frequency bins are then scanned for the bin with the largest amplitude. This is defined as the fundamental frequency. The amplitude of the fundamental is determined by computing the RMS sum of the bin below the fundamental, the fundamental and the bin above the fundamental.

This 3-cell summation yields an amplitude accurate to less than 0.01 db. The amplitude for each harmonic is calculated by summing the 3 bins around 2X the fundamental for the second harmonic, 3X the fundamental for the third and so on. This yields the harmonic distortion.

The signal to noise ratio is calculated by taking the RMS sum of the frequency bins up to 255 (the Nyquist rate) with the exception of the D.C term (bins 1, 2, and 3), the fundamental frequency (10 bins below the fundamental to 10 bins above the fundamental) and ±2 bins around each harmonic. The number of bins eliminated in each case is due to the leakage of the windowing function causing spillover into the area around the frequency terms. The summed frequency bins are then compared to the normalized fundamental for calculation of the broadband signal-to-noise ratio.



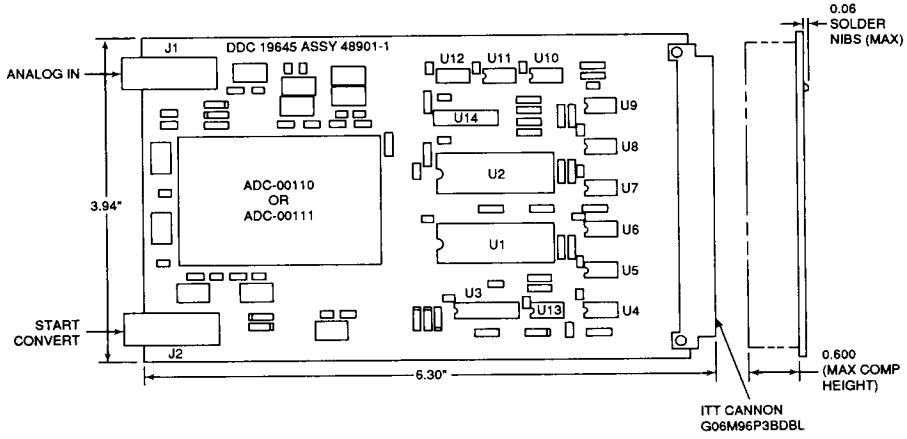
HARMONIC	BIN #	AMPLITUDE (db)
1	251	- 1.04
2	10	-70.74
3	241	-80.69
4	20	-77.65
5	231	-80.07

SIGNAL-TO-NOISE RATIO = 65.10 db
TOTAL HARMONIC DISTORTION = -68.17 db
SIGNAL-TO-(NOISE + DISTORTION) = 63.68 db
FFT size is 512 points.
Input Data Weighted by Hanning Window.

FIGURE 3. DYNAMIC TEST DATA

ADC-00110-615 EVALUATION CARD

The ADC-00110-615 Evaluation Card enables analysis of the ADC-00110 performance via digital interface. Figure 4 illustrates the ADC-00110-615 and Table 3 enumerates the input/output pin locations and functions. With on-board FIFO the card allows the user to capture up to 1024 WORDS for subsequent digital signal processing. DDC uses this fixturization for capturing data and performance of histogram and FFT in order to characterize the dynamic performance of the ADC-00110 and ADC-00111.

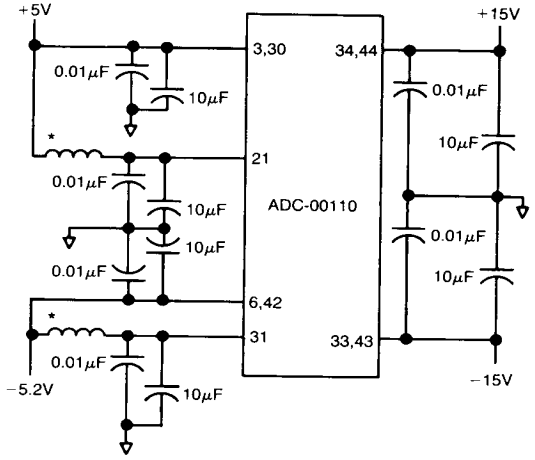


ACTIVE PARTS LIST		
COMPONENT	P/N	DESCRIPTION
U1, U2	IDT7202	FIFO
U3	75LS00N	GATE
U4 - U13	HPCL2231	OPTO-COUPLERS
U14	74HCT74	FLIP - FLOP

FIGURE 4. ADC-00110-615 MECHANICAL OUTLINE

TABLE 3. ADC-00110 VME PIN ASSIGNMENTS

ROW A				ROW C			
PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
A1	GND	A17	GND	C1	GND	C17	GND
A2	(ACQUIRE/$\overline{\text{RESET}}$)	A18	$\overline{\text{RE-TRANSMIT}}$	C2	N/C	C18	BIT2
A3	$\overline{\text{HALF-FULL FLAG}}$	A19	+5V COMP	C3	$\overline{\text{EMPTY FLAG}}$	C19	BIT1 (MSB)
A4	N/C	A20	COMP RTN	C4	BIT12	C20	$\overline{\text{BIT1}}$ ($\overline{\text{MSB}}$)
A5	GND	A21	GND	C5	GND	C21	GND
A6	GND	A22	GND	C6	BIT11	C22	OUT REG
A7	GND	A23	GND	C7	BIT10	C23	$\overline{\text{FULL FLAG}}$
A8	$\overline{\text{READ}}$	A24	+15V	C8	BIT9	C24	+15V
A9	GND	A25	GND	C9	GND	C25	GND
A10	N/C	A26	-15V	C10	BIT8	C26	-15V
A11	GND	A27	$\overline{\text{WRINH}}$	C11	BIT7	C27	DATA READY
A12	GND	A28	+5V	C12	BIT6	C28	+5V
A13	GND	A29	GND	C13	GND	C29	GND
A14	N/C	A30	-5.2V	C14	BIT5	C30	-5.2V
A15	GND	A31	-5.2V	C15	BIT4	C31	-5.2V
A16	GND	A32	N/C	C16	BIT3	C32	N/C



*Ferrite bead. (See text on **POWER SUPPLY DECOUPLING**).

FIGURE 5. POWER SUPPLY DECOUPLING

TABLE 4. ADC-00110 PIN FUNCTIONS

PIN	FUNCTION	PIN	FUNCTION
1	Analog Ground	46	Analog Return
2	NC	45	T/H Analog Input
3	+5V Analog Supply	44	+15V Supply
4	T/H Analog Output	43	−15V Supply
5	A/D Analog Input	42	−5.2V Analog Supply
6	−5.2V Analog Supply	41	NC
7	Overrange	40	NC (Factory Test Point)
8	$\overline{\text{MSB}}$	39	NC
9	Bit 1 (MSB)	38	NC
10	Bit 2	37	Case Ground
11	Bit 3	36	NC (Factory Test Point)
12	Bit 4	35	Analog Ground
13	Bit 5	34	+15V Supply
14	Bit 6	33	−15V Supply
15	Bit 7	32	Digital Ground
16	Bit 8	31	−5.2V Digital Supply
17	Bit 9	30	+5V Analog Supply
18	Bit 10	29	NC (Factory Test Point)
19	Bit 11	28	NC (Factory Test Point)
20	Bit 12 (LSB)	27	NC (Factory Test Point)
21	+5V Digital Supply	26	Digital Ground
22	Data Ready	25	Output Enable
23	Digital Ground	24	Encode Command

Notes:
1. Pins 4 and 5 are to be externally connected.
2. NC means do not connect any signal to these pins as damage may occur to the hybrid.

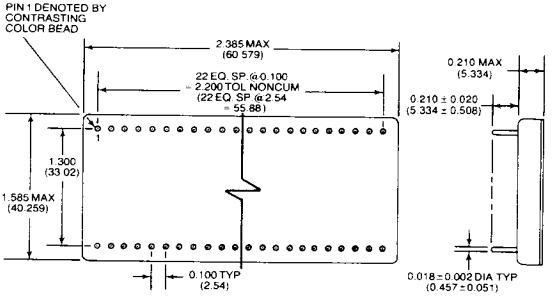
ORDERING INFORMATION

ADC- 00110 - 1 0 2

- Reliability:
  - 0 = Standard DDC procedures
  - 1 = Military processing available (Consult Factory)
  - 2 = Military processing available but without QCI testing.(Consult Factory)
- Operating Temperature Range:
  - 1 = -55 to +125°C
  - 3 = 0 to +70°C
- Input Voltage Range:
  - 0 = ±2.5V Input
  - 1 = ±1.0V Input

Consult factory for ECL Logic Compatibility.

ADC-00110-615 EVALUATION CARD



Notes:
1. Dimensions are in inches (mm).
2. Pin clusters to be centralized within ±0.010 of outline dimensions.

FIGURE 6. ADC-00110 AND ADC-00112 MECHANICAL OUTLINE

G