REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Technical changes were made in table I. Editorial changes throughout.	1990 AUG 15	W. Heckman
B	Changes in accordance with NOR 5962-R023-92.	1991 OCT 30	M. Poelking
C	Changes in accordance with NOR 5962-R189-93.	1993 JUL 07	J. Dupay
D	Add devices 03, 04, 05, and 06. Editorial changes throughout.	1994 NOV 21	M. Poelking

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV	D	D	D	D	D	D	D	D	D										
SHEET	36	37	38	39	40	41	42	43	44										
REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	29	30	31	32	33	34	35

REV STATUS OF SHEETS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
1989 FEB 16

REVISION LEVEL
D

DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS, 16-BIT MICROPROCESSOR, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-88501
A	67268	

SHEET 1 OF 44

DESC FORM 193
JUL 94

5962-E035-95

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

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1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Frequency	Circuit function
01	M80C186	10 MHz	16-bit CHMOS microprocessor
02	M80C186	12.5 MHz	16-bit CHMOS microprocessor
03	M80C186XL	20 MHz	16-bit CHMOS microprocessor
04	M80C186XL	16 MHz	16-bit CHMOS microprocessor
05	M80C186XL	12.5 MHz	16-bit CHMOS microprocessor
06	M80C186XL	10 MHz	16-bit CHMOS microprocessor

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Y	See figure 1	68	Ceramic quad package
Z	CMGA3-P68	68	Pin grid array package

1.2.3 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein). Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings.

Voltage on any pin (referenced to GND)	-1.0 V dc to +7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	1 W
Thermal resistance, junction-to-case (θ_{JC}):	
Case Y	13°C/W
Case Z	See MIL-STD-1835
Junction temperature (T_J):	+150°C
Lead temperature (soldering, 5 seconds)	+260°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC}):	
Devices 01, 02	4.75 V dc to 5.25 V dc
Devices 03 - 06	4.5 V dc to 5.5 V dc
Frequency of operation:	
Device type 01	10 MHz
Device type 02	12.5 MHz
Device type 03	20 MHz
Device type 04	16 MHz
Device type 05	12.5 MHz
Device type 06	10 MHz
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-I-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-I-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-I-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Functional block diagrams. The functional block diagrams shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Low level input voltage (Except X1)	V_{IL}		All	1, 2, 3	-0.5	0.2 V_{CC} -0.3	V
High level input voltage (All except X1, (RES))	V_{IH1}		01-02	1, 2, 3	0.2 V_{CC} +1.1	V_{CC} +0.5	V
			03-06		0.2 V_{CC} +0.9	V_{CC} +0.5	
High level input voltage at (RES)	V_{IH2}		All	1, 2, 3	3.0	V_{CC} +0.5	V
High level input voltage at (ARDY/SRDY)	V_{IH3}		01-02	1, 2, 3	0.2 V_{CC} +1.3	V_{CC} +0.5	V
Low level output voltage	V_{OL}	I_{OL} = 2.5 mA for $\overline{S0}$-$\overline{S2}$ I_{OL} = 2.0 mA for all other outputs	All	1, 2, 3		0.45	V
High level output voltage	V_{OH}	I_{OH} = -200 µA at 0.8 V_{CC}	01-02	1, 2, 3	0.8 V_{CC}	2/ V_{CC}	V
High level output voltage	V_{OH}	I_{OH} = -200 µA at V_{CC} - 0.5 V	03-06	1, 2, 3	V_{CC} - 0.5 V	2/ V_{CC}	V
High level output voltage	V_{OH}	I_{OH} = -2.4 mA at 2.4 V	All	1, 2, 3	2.4	2/ V_{CC}	V
Power supply current 3/	I_{CC}	V_{CC} = Max 4/	01	1, 2, 3		140	mA
			02			160	
			03			100	
			04			90	
			05			80	
			06			70	
Input leakage current	I_{IL}	0.45 V < V_{IN} < V_{CC}	All	1, 2, 3		±10	µA
Output leakage current	I_{OL}	0.45 V < V_{OUT} < V_{CC} 5/ At 0.5 MHz	All	1, 2, 3		±10	µA
Low level clock output voltage	V_{CLO}	I_{CLO} = 4.0 mA	01-02	1, 2, 3		0.5	V
			03-06			0.45	
High level clock output voltage	V_{CHO}	I_{CHO} = -500 µA	01-02	1, 2, 3	0.8 V_{CC}		V
			03-06		V_{CC}-0.5		
Low level clock input voltage (X1)	V_{CLI}		All	1, 2, 3	-0.5	+0.6	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
High level clock input voltage (X1)	V_{CHI}		All	1, 2, 3	3.9	V_{CC} +0.5	V
Functional tests		See 4.3.1d	All	7, 8			
Input capacitance	C_{IN}	See 4.3.1c, f = 1 MHz	All	4		10	pF
I/O capacitance	C_{IO}	See 4.3.1c, f = 1 MHz	All	4		20	pF
Data in set-up (A/D)	t_{DVCL}	See figure 4	01-02 03 04-06	9, 10, 11	20 10 15		ns
Data in hold (A/D)	t_{CLDX}		01-02 03-06	9, 10, 11	5 3		ns
ARDY resolution transition set-up time 6/	t_{ARYCH}		01-02 03 04-06	9, 10, 11	20 10 15		ns
Asynchronous ready (ARDY) set-up time	t_{ARYLCL}		01-02 03 04-06	9, 10, 11	30 15 25		ns
ARDY active hold time	t_{CLARX}		01-02 03 04-06	9, 10, 11	15 10 15		ns
ARDY inactive hold time	t_{ARYCHL}		01-02 03 04-06	9, 10, 11	15 10 15		ns
Synchronous ready (SRDY) transition set-up time	t_{SRYCL}		01-02 03 04-06	9, 10, 11	20 10 15		ns
SRDY transition hold time	t_{CLSRY}		01-02 03 04-06	9, 10, 11	20 10 15		ns
Hold set-up 6/	t_{HVCL}		01-02 03 04-06	9, 10, 11	20 10 15		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
INT_X, NMI, $\overline{TEST}$, TMRIN 6/ set-up time	t_{INVCH}	See figure 4	01-02	9, 10, 11	20		ns
			03		10		
			04-06		15		
DRQ0, $\overline{DRQ1}$, 6/ set-up time	t_{INVCL}		01-02	9, 10, 11	20		ns
			03		10		
			04-06		15		
Address valid delay	t_{CLAV}		01	9, 10, 11	5	50	ns
			02	9, 10, 11	5	37	ns
			03	9, 10, 11	1	27	ns
			04	9, 10, 11	1	33	ns
			05	9, 10, 11	3	36	ns
			06	9, 10, 11	3	44	ns
Address hold	t_{CLAX}		01-02	9, 10, 11	0		ns
			03-06		0 2/		
Address float delay	t_{CLAZ}		01	9, 10, 11	t_{CLAX}	30	ns
			02	9, 10, 11	t_{CLAX}	25	ns
			03-04	9, 10, 11	t_{CLAX}	20	ns
			05	9, 10, 11	t_{CLAX}	25	ns
			06	9, 10, 11	t_{CLAX}	30	ns
Command lines float delay	t_{CHCZ}		01	9, 10, 11		40	ns
			02	9, 10, 11		33	ns
			03	9, 10, 11		25	ns
			04	9, 10, 11		28	ns
			05	9, 10, 11		33	ns
			06	9, 10, 11		40	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Command lines valid delay (after float)	t_{CHCV}	See figure 4	01	9, 10, 11		45	ns
			02	9, 10, 11		37	ns
			03	9, 10, 11		26	ns
			04	9, 10, 11		32	ns
			05	9, 10, 11		36	ns
			06	9, 10, 11		44	ns
ALE width	t_{LHLL}		01-02 03-06	9, 10, 11	$t_{CLCL-30}$ $t_{CLCL-15}$		ns
ALE active delay	t_{CHLH}		01	9, 10, 11		30	ns
			02	9, 10, 11		25	ns
			03-04	9, 10, 11		20	ns
			05	9, 10, 11		25	ns
			06	9, 10, 11		30	ns
ALE inactive delay	t_{CHLL}		01	9, 10, 11		30	ns
			02	9, 10, 11		25	ns
			03-04	9, 10, 11		20	ns
			05	9, 10, 11		25	ns
			06	9, 10, 11		30	ns
Address hold to ALE inactive	t_{LLAX}		01	9, 10, 11	$t_{CHCL-20}$		ns
			02	9, 10, 11	$t_{CHCL-15}$		ns
		Equal loading See figure 4	03	9, 10, 11	$t_{CHCL-10}$		ns
			04-06	9, 10, 11	$t_{CHCL-15}$		ns
Data valid delay	t_{CLDV}	See figure 4	01	9, 10, 11	5	40	ns
			02	9, 10, 11	5	36	ns
			03	9, 10, 11	1	27	ns
			04	9, 10, 11	1	33	ns
			05	9, 10, 11	3	36	ns
			06	9, 10, 11	3	40	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Data hold time	t_{CLDOX}	See figure 4	01-02	9, 10, 11	3		ns
			03-04		1		
			05-06		3		
Data hold after $\overline{WR}$ (min)	t_{WHDX}		01	9, 10, 11	$t_{CLCL-34}$		ns
			02	9, 10, 11	$t_{CLCL-20}$		ns
		Equal loading See figure 4	03	9, 10, 11	$t_{CLCL-15}$		ns
			04-05	9, 10, 11	$t_{CLCL-20}$		ns
			06	9, 10, 11	$t_{CLCL-34}$		ns
$\overline{WR}$ inactive to $\overline{DEN}$ inactive	t_{WHDEX}	See figure 4	01-02	9, 10, 11	$t_{CLCH-10}$		ns
		Equal loading See figure 4	03-06	9, 10, 11	$t_{CLCH-10}$		ns
$\overline{WR}$ inactive to ALE high	t_{WHLH}	See figure 4	01-02	9, 10, 11	$t_{CLCH-14}$		ns
		Equal loading See figure 4	03-06	9, 10, 11	$t_{CLCH-14}$		ns
Control active delay 1	t_{CVCTV}	See figure 4	01	9, 10, 11	3	56	ns
			02	9, 10, 11	3	47	ns
			03	9, 10, 11	1	22	ns
			04	9, 10, 11	1	31	ns
			05	9, 10, 11	3	37	ns
			06	9, 10, 11	3	44	ns
Control active delay 2	t_{CHCTV}		01	9, 10, 11	5	44	ns
			02	9, 10, 11	5	37	ns
			03	9, 10, 11	1	22	ns
			04	9, 10, 11	1	31	ns
			05	9, 10, 11	3	37	ns
			06	9, 10, 11	3	44	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Control inactive delay	t_{CVCTX}	See figure 4	01	9, 10, 11	3	44	ns
			02	9, 10, 11	3	37	ns
			03	9, 10, 11	1	25	ns
			04	9, 10, 11	1	31	ns
			05	9, 10, 11	3	37	ns
			06	9, 10, 11	3	44	ns
$\overline{DEN}$ inactive delay (nonwrite cycle)	t_{CVDEX}		01	9, 10, 11	5	56	ns
			02	9, 10, 11	5	47	ns
			03	9, 10, 11	1	22	ns
			04	9, 10, 11	1	31	ns
			05	9, 10, 11	3	37	ns
			06	9, 10, 11	3	44	ns
2/ Address float to $\overline{RD}$ active	t_{AZRL}		All	9, 10, 11	0		ns
$\overline{RD}$ active delay	t_{CLRL}		01	9, 10, 11	5	44	ns
			02	9, 10, 11	5	37	ns
			03	9, 10, 11	1	27	ns
			04	9, 10, 11	1	31	ns
			05	9, 10, 11	3	37	ns
			06	9, 10, 11	3	44	ns
$\overline{RD}$ inactive delay	t_{CLRH}		01	9, 10, 11	5	44	ns
			02	9, 10, 11	5	37	ns
			03	9, 10, 11	1	27	ns
			04	9, 10, 11	1	31	ns
			05	9, 10, 11	3	37	ns
			06	9, 10, 11	3	44	ns
$\overline{RD}$ inactive to ALE high	t_{RHLH}	See figure 4	01-02	9, 10, 11	$t_{CLCH-14}$		ns
		Equal loading See figure 4	03-06	9, 10, 11	$t_{CLCH-14}$		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
$\overline{RD}$ inactive to address active (min)	t_{RHAV}	See figure 4	01	9, 10, 11	$t_{CLCL-40}$		ns
			02	9, 10, 11	$t_{CLCL-20}$		ns
		Equal loading See figure 4	03-06	9, 10, 11	$t_{CLCL-15}$		ns
HLDA valid delay	t_{CLHAV}	See figure 4	01	9, 10, 11	3	40	ns
			02	9, 10, 11	3	33	ns
			03	9, 10, 11	1	22	ns
			04	9, 10, 11	1	25	ns
			05	9, 10, 11	3	33	ns
			06	9, 10, 11	3	40	ns
$\overline{RD}$ pulse width (min)	t_{RLRH}		01	9, 10, 11	$2t_{CLCL-46}$		ns
			02	9, 10, 11	$2t_{CLCL-40}$		ns
			03	9, 10, 11	$2t_{CLCL-20}$		ns
			04-05	9, 10, 11	$2t_{CLCL-25}$		ns
			06	9, 10, 11	$2t_{CLCL-30}$		ns
$\overline{WR}$ pulse width (min)	t_{WLWH}		01	9, 10, 11	$2t_{CLCL-34}$		ns
			02	9, 10, 11	$2t_{CLCL-30}$		ns
			03	9, 10, 11	$2t_{CLCL-20}$		ns
			04-05	9, 10, 11	$2t_{CLCL-25}$		ns
			06	9, 10, 11	$2t_{CLCL-30}$		ns
Address valid to ALE low (min)	t_{AVLL}		01	9, 10, 11	$t_{CLCH-19}$		ns
			02	9, 10, 11	$t_{CLCH-15}$		ns
		Equal loading See figure 4	03	9, 10, 11	$t_{CLCH-10}$		ns
			04-05	9, 10, 11	$t_{CLCH-15}$		ns
			06	9, 10, 11	$t_{CLCH-18}$		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Status active delay	t_{CHSV}	See figure 4	01	9, 10, 11	5	45	ns
			02	9, 10, 11	5	35	ns
			03	9, 10, 11	1	25	ns
			04	9, 10, 11	1	31	ns
			05	9, 10, 11	3	35	ns
			06	9, 10, 11	3	45	ns
Status inactive delay	t_{CLSH}		01	9, 10, 11	5	50	ns
			02	9, 10, 11	5	35	ns
			03	9, 10, 11	1	25	ns
			04	9, 10, 11	1	30	ns
			05	9, 10, 11	3	35	ns
			06	9, 10, 11	3	46	ns
Timer output delay	t_{CLTMV}	C_L = 100 pF maximum at 10 MHz See figure 4	01	9, 10, 11		48	ns
		See figure 4	02	9, 10, 11		40	ns
			03	9, 10, 11		22	ns
			04	9, 10, 11		27	ns
			05	9, 10, 11		33	ns
			06	9, 10, 11		40	ns
Reset delay	t_{CLRO}		01	9, 10, 11		48	ns
			02	9, 10, 11		40	ns
			03	9, 10, 11		22	ns
			04	9, 10, 11		27	ns
			05	9, 10, 11		33	ns
			06	9, 10, 11		40	ns
Queue status delay	t_{CHQSV}		01-02	9, 10, 11		28	ns
			03			27	
			04			30	
			05			32	
			06			37	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
$\overline{RES}$ set-up	t_{RESIN}	See figure 4	03-06	9, 10, 11	15		ns
Status hold time	t_{CHDX}		01-02	9, 10, 11	5		ns
Address valid to clock high	t_{AVCH}		All	9, 10, 11	0		ns
$\overline{LOCK}$ valid/invalid delay	t_{CLLV}		01	9, 10, 11	3	45	ns
			02	9, 10, 11	3	40	ns
			03	9, 10, 11	1	22	ns
			04	9, 10, 11	1	35	ns
			05	9, 10, 11	3	37	ns
			06	9, 10, 11	3	40	ns
$\overline{DEN}$ inactive to DT/$\overline{R}$ low	t_{DXDL}		01-02	9, 10, 11	0		ns
		Equal loading See figure 4	03-06	9, 10, 11	0		
Chip-select active delay	t_{CLCSV}	See figure 4	01	9, 10, 11		45	ns
			02	9, 10, 11		33	ns
			03	9, 10, 11	1	25	ns
			04	9, 10, 11	1	30	ns
			05	9, 10, 11	3	33	ns
			06	9, 10, 11	3	42	ns
Chip-select hold from command inactive	t_{CXCSX}		01-02	9, 10, 11	$t_{CLCH-10}$		ns
		Equal loading See figure 4	03-06	9, 10, 11	$t_{\overline{CLCH}-10}$		
Chip-select inactive delay	t_{CHCSX}	See figure 4	01	9, 10, 11	5	40	ns
			02	9, 10, 11	5	36	ns
			03	9, 10, 11	1	20	ns
			04	9, 10, 11	1	35	ns
			05	9, 10, 11	3	30	ns
			06	9, 10, 11	3	35	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
CLKIN period	t_{CKIN}	See figure 4	01	9, 10, 11	50	1000	ns
			02	9, 10, 11	40	1000	ns
			03	9, 10, 11	25	Inf	ns
			04	9, 10, 11	31.25	Inf	ns
			05	9, 10, 11	40	Inf	ns
			06	9, 10, 11	50	Inf	ns
$\overline{RD}$ valid to Clock high	T_{RVCH}		01-02	9, 10, 11	25		ns
Chip select valid to ALE low	T_{CSVLL}		01-02	9, 10, 11	T_{CLCH}-14		ns
CLKIN fall time 2/	t_{CKHL}	See figure 4 3.5 V to 1.0 V 7/	All	9, 10, 11		5	ns
CLKIN rise time	t_{CKLH}	1.0 V to 3.5 V See figure 4 7/	All	9, 10, 11		5	ns
CLKIN low time	t_{CLCK}	@ 1.5 V See figure 4 7/ 8/	01	9, 10, 11	23		ns
			02	9, 10, 11	18		ns
			03	9, 10, 11	10	Inf	ns
			04	9, 10, 11	13	Inf	ns
			05	9, 10, 11	16	Inf	ns
			06	9, 10, 11	20	Inf	ns
CLKIN high time	t_{CHCK}		01	9, 10, 11	23		ns
			02	9, 10, 11	18		ns
			03	9, 10, 11	10	Inf	ns
			04	9, 10, 11	13	Inf	ns
			05	9, 10, 11	16	Inf	ns
			06	9, 10, 11	20	Inf	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
CLKIN to CLKOUT skew	t_{CICO}	See figure 4	01	9, 10, 11		25	ns
			02	9, 10, 11		21	ns
			03-04	9, 10, 11		17	ns
			05	9, 10, 11		21	ns
			06	9, 10, 11		25	ns
CLKOUT period	t_{CLCL}		01	9, 10, 11	100	2000	ns
			02	9, 10, 11	80	2000	ns
			03	9, 10, 11	50	Inf	ns
			04	9, 10, 11	62.5	Inf	ns
			05	9, 10, 11	80	Inf	ns
			06	9, 10, 11	100	Inf	ns
CLKOUT low time	t_{CLCH}	@ 1.5 V See figure 4/ 7/	01	9, 10, 11	$0.5t_{CLCL-8}$		ns
			02	9, 10, 11	$0.5t_{CLCL-7}$		ns
		C_L = 100 pF	03-05	9, 10, 11	$0.5t_{CLCH-5}$		ns
			06	9, 10, 11	$0.5t_{CLCH-6}$		ns
CLKOUT high time	t_{CHCL}	@ 1.5 V See figure 4/ 7/	01	9, 10, 11	$0.5t_{CLCL-8}$		ns
			02	9, 10, 11	$0.5t_{CLCL-7}$		ns
		C_L = 100 pF	03-05	9, 10, 11	$0.5t_{CLCH-5}$		ns
			06	9, 10, 11	$0.5t_{CLCH-6}$		ns
CLKOUT rise time	t_{CH1CH2}	1.0 V to 3.5 V See figure 4 7/	01-02	9, 10, 11		10	ns
			03	9, 10, 11		8	
			04-06	9, 10, 11		10	
CLKOUT fall time	t_{CL2CL1}	3.5 V to 1.0 V See figure 4 7/	01-02	9, 10, 11		10	ns
			03	9, 10, 11		8	
			04-06	9, 10, 11		10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

1/ Device types 1 and 2 are equal to V_{CC} = 5.0 V ±5% and device types 3 through 6 are equal to V_{CC} = 5.0 V ±10%.

All timings are measured at 1.5 V and 100 pF loading on CLKOUT unless specified. For device types 1 the outputs are measured with C_L = 50 - 200 pF (10 MHz), for device type 2 C_L = 50 - 100 pF (12.5 MHz). For devices 3 through 6, all output test conditions are with C_L = 50 pF unless noted. For ac tests, input V_{IL} = 0.45 V and V_{IH} = 2.4 V except at X1 where $V_{IH} = V_{CC}$ - 0.5 V. See figure 4.

2/ Guaranteed if not tested to the limits specified.

3/ Power save current (I_{PS}) at +25°C with V_{CC} = 5.0 V is typically 10 mA per MHz + 20 mA.

4/ Current is measured with the device in RESET with X1 and X2 driven and all other nonpower pins open.

5/ Pins being floated during HOLD or by invoking the ONCE mode.

6/ To guarantee recognition at next CLK.

7/ Voltages indicated refer to voltage measurements on waveforms on figure 4.

8/ t_{CLCK} and t_{CKCK} (CLKIN low and high times) should not have a duration less than 45 percent of t_{CKIN}.

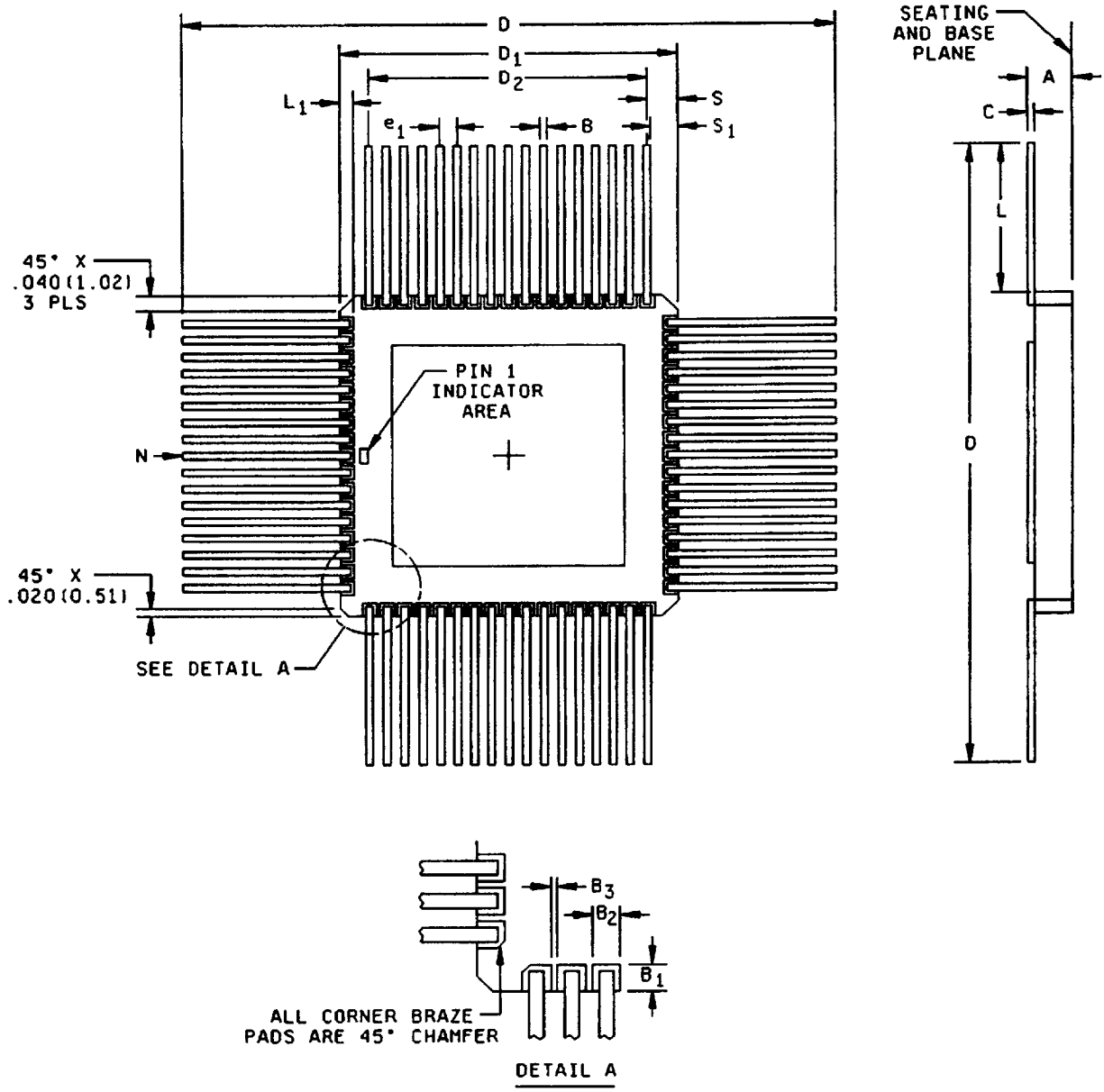


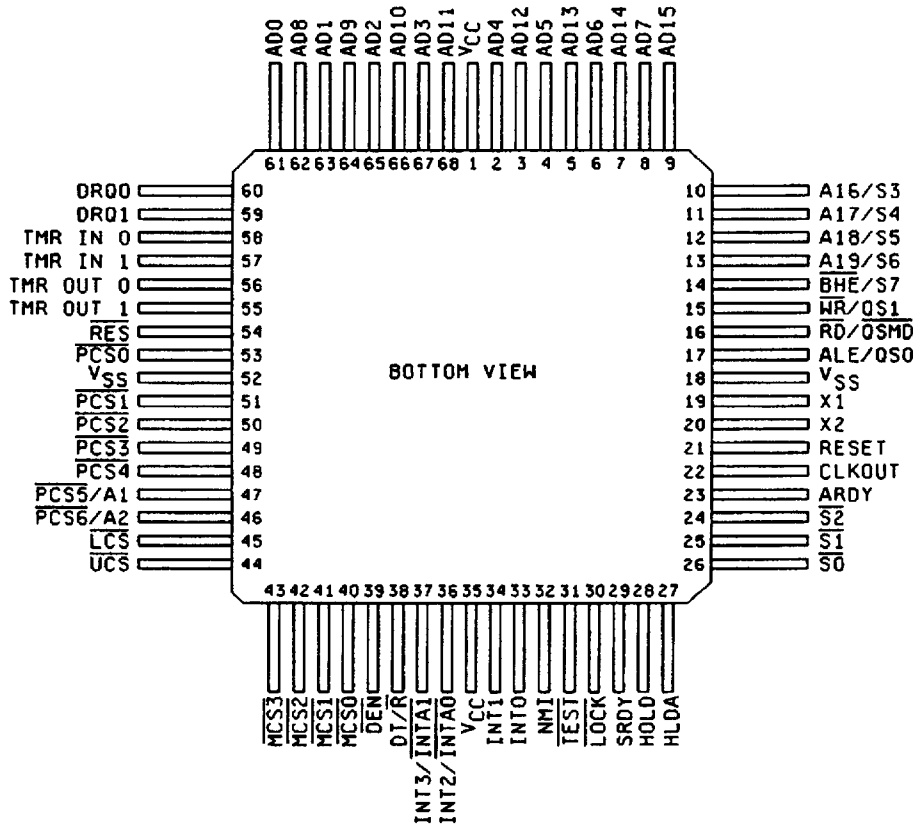
FIGURE 1. Case outline Y.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-88501
		REVISION LEVEL D	SHEET 16

Dimensions				
Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.080	.106	2.03	2.69
B	.016	.020	0.41	0.51
B_1	.040	.060	1.02	1.52
B_2	.030	.040	0.76	1.02
B_3	.005	.020	0.13	0.51
C	.008	.012	0.20	0.31
D	1.640	1.870	41.66	47.50
D_1	.935	.970	23.75	24.64
D_2	.800 BSC		20.32 BSC	
e_1	.050 BSC		1.27 BSC	
L	.375	.450	9.53	11.43
L_1	.040	.060	1.02	1.52
N	68		68	
S	.066	.087	1.68	2.21
S_1	.050		1.27	

FIGURE 1. Case outline Y - Continued.

Case outline Y



(Bottom view)

FIGURE 2. Terminal connections.

Case outline Z

Symbol	Location	Symbol	Location	Symbol	Location
V_{CC}, V_{CC}	F1, F11	A16/S3	A2	$\overline{RD}/\overline{QSMD}$	A5
V_{SS}, V_{SS}	L6, A6	AD15	B1	ARDY	B9
Reset	B8	AD14	C1	SRDY	C11
X1, X2	B7, A7	AD13	D1	$\overline{LOCK}$	D10
CLKOUT	A8	AD12	E1	$\overline{S0}$	A10
$\overline{RES}$	L5	AD11	F2	$\overline{S1}$	B10
$\overline{TEST}$	D11	AD10	G2	$\overline{S2}$	A9
TMR IN 0	L3	AD9	H2	HOLD	C10
TMR IN 1	K3	AD8	J2	(input)	
TMR OUT 0	L4	AD7	B2	HLDA	B11
TMR OUT 1	K4	AD6	C2	(output)	
DRQ0	L2	AD5	D2	$\overline{UCS}$	L10
DRQ1	K2	AD4	E2	$\overline{LCS}$	K9
NMI	E10	AD3	G1	$\overline{MCS0}$-3	J10, J11 K10, K11
INT0, INT1	E11, F10	AD2	H1	$\overline{PCS0}$	K5
INT2/$\overline{INTA0}$	G10	AD1	J1	$\overline{PCS1}$-4	K6,L7,K7,L8
INT3/$\overline{INTA1}$	G11	AD0	K1	$\overline{PCS5}$/A1	K8
A19/S6	B4	$\overline{BHE}$/S7	A4	$\overline{PCS6}$/A2	L9
A18/S5	A3	ALE/QS0	B6	DT/$\overline{R}$	H10
A17/S4	B3	$\overline{WR}$/QS1	B5	$\overline{DEN}$	H11

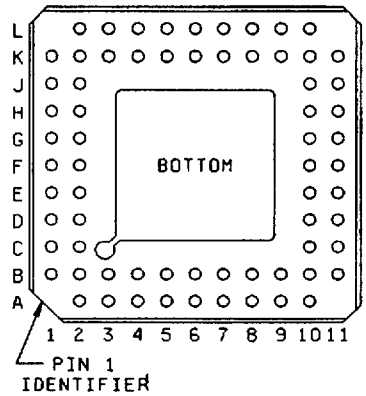


FIGURE 2. Terminal connections - Continued.

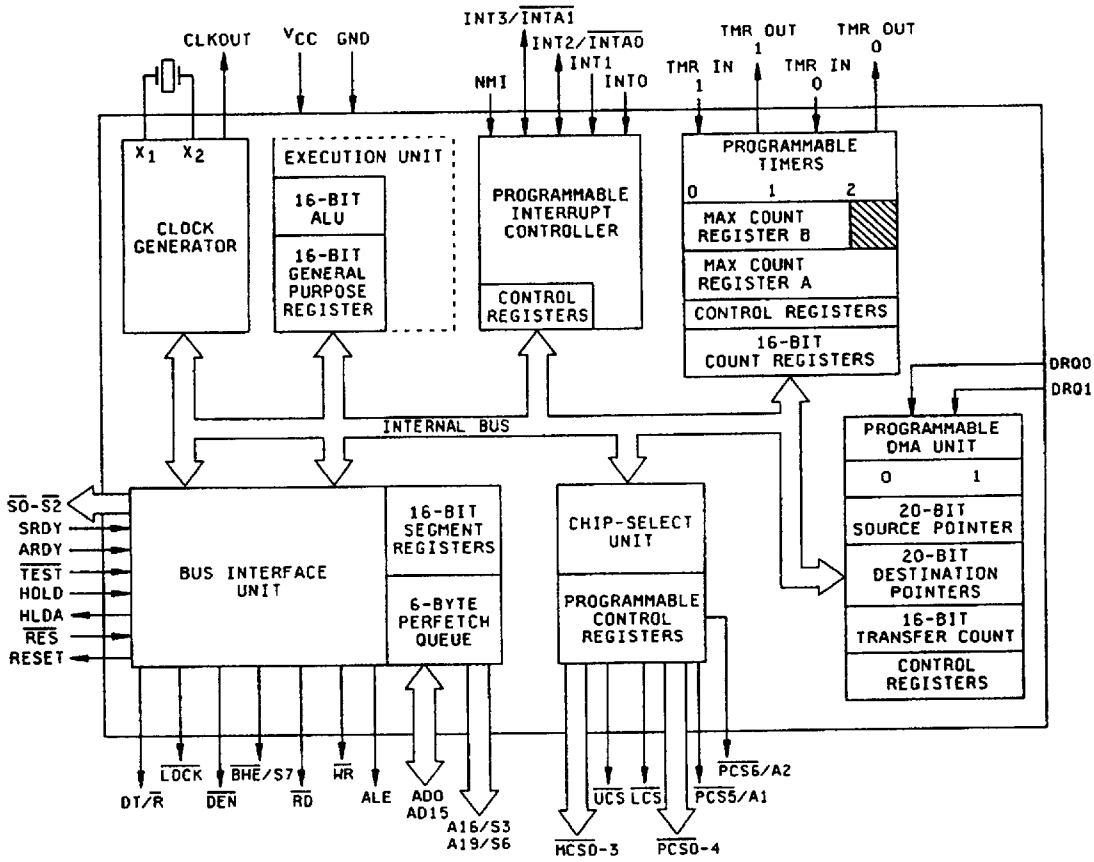


FIGURE 3. Functional block diagram.

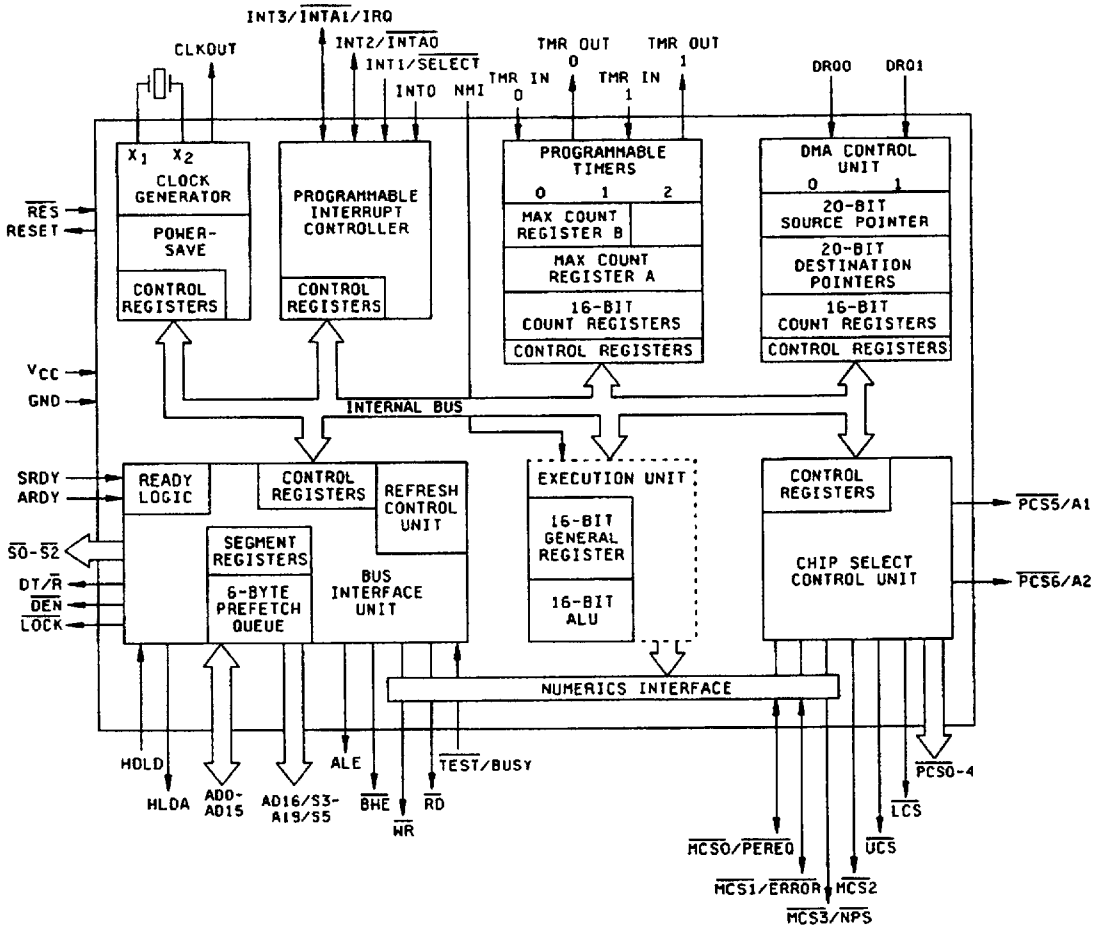


FIGURE 3. Functional block diagram. - Continued

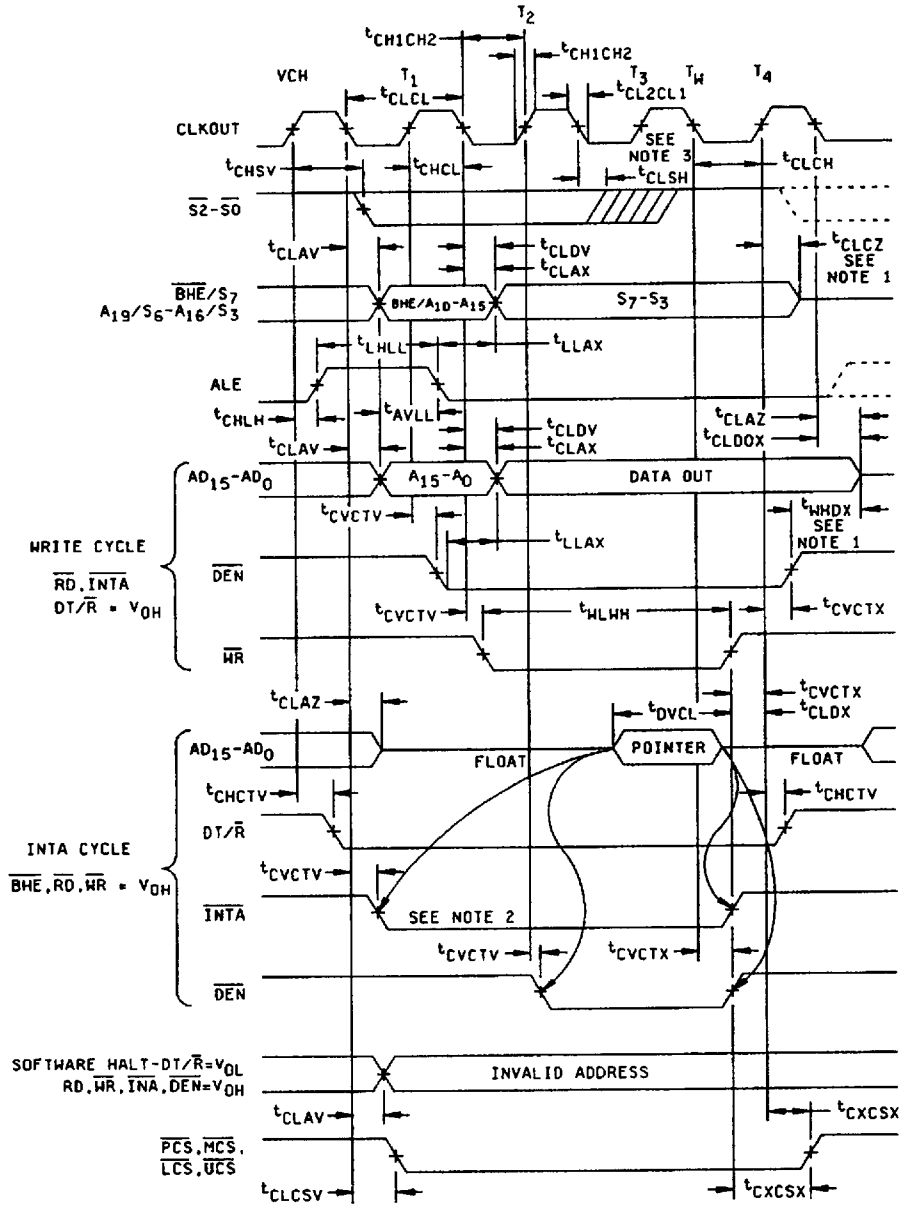
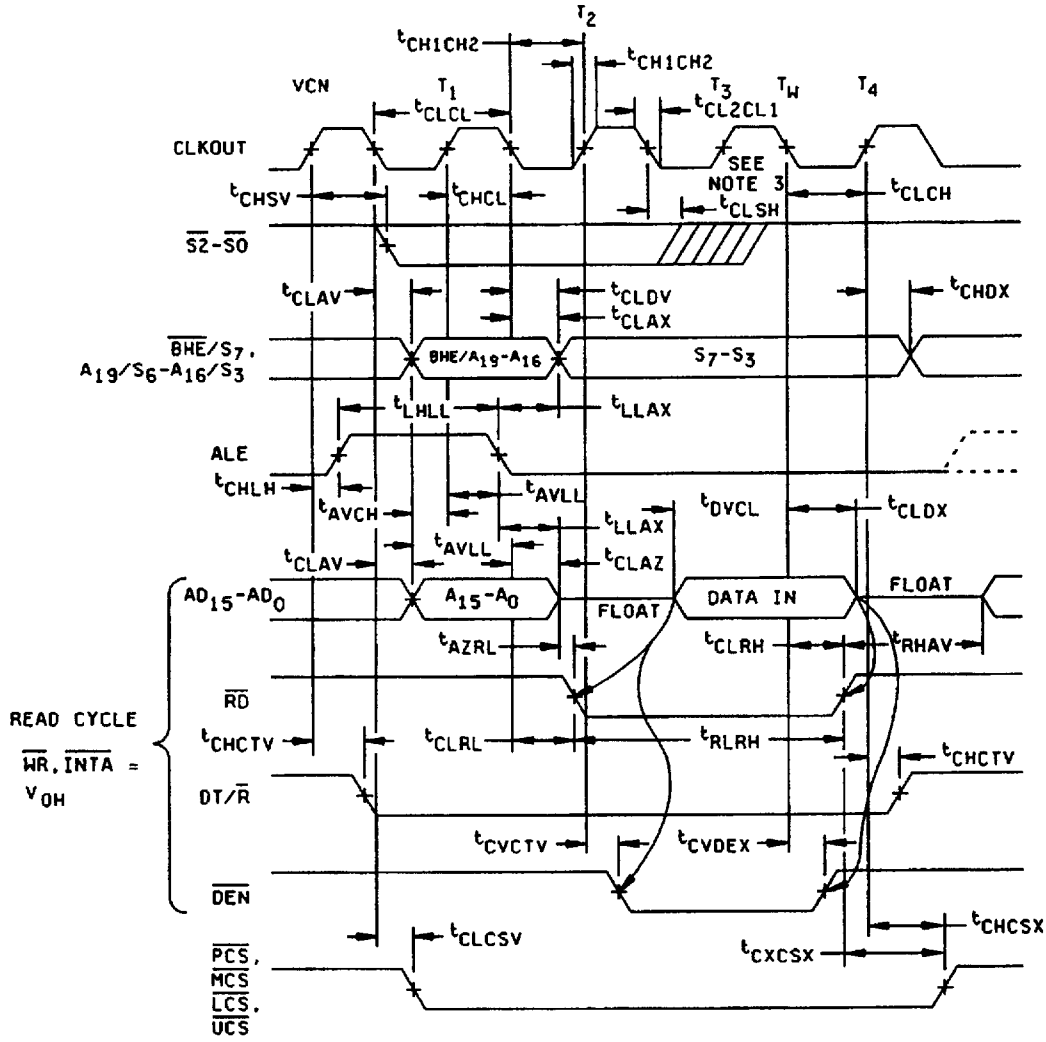


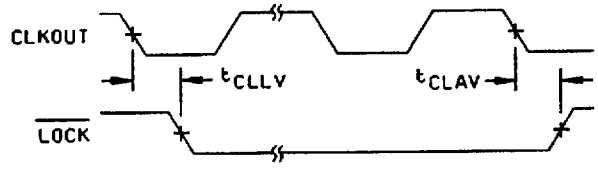
FIGURE 4. Timing waveforms.



NOTES:
1. Following a write cycle, the local bus is floated by the devices only when the devices enters a "hold acknowledge" state.
2. INTA occurs one clock later in slave-mode.
3. Status inactive just prior to T_4.
4. Latched A1 and A2 have the same timings as PCS5 and PCS6.
5. For write cycle followed by read.

FIGURE 4. Timing waveforms - Continued.

BUS LOCK SIGNAL TIMING



ASYNCHRONOUS SIGNAL RECOGNITION

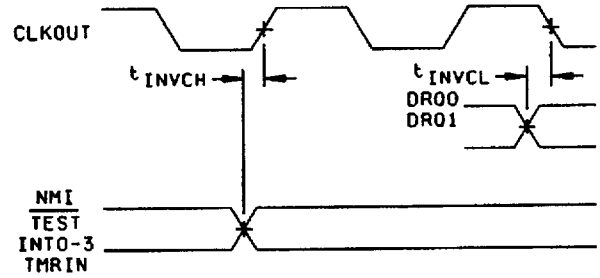
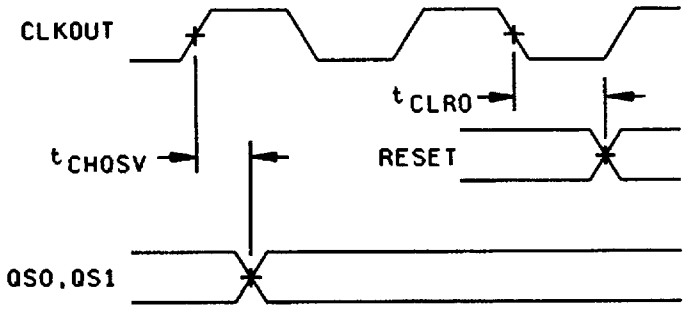


FIGURE 4. Timing waveforms - Continued.

QUEUE STATUS TIMING



READY TIMING

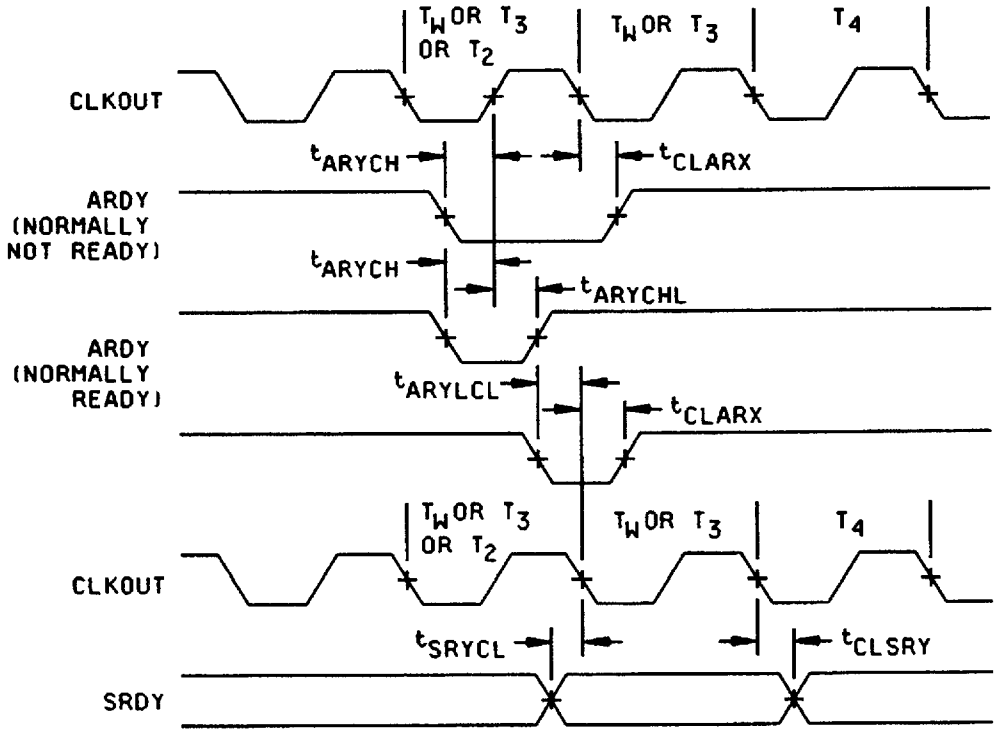


FIGURE 4. Timing waveforms - Continued.

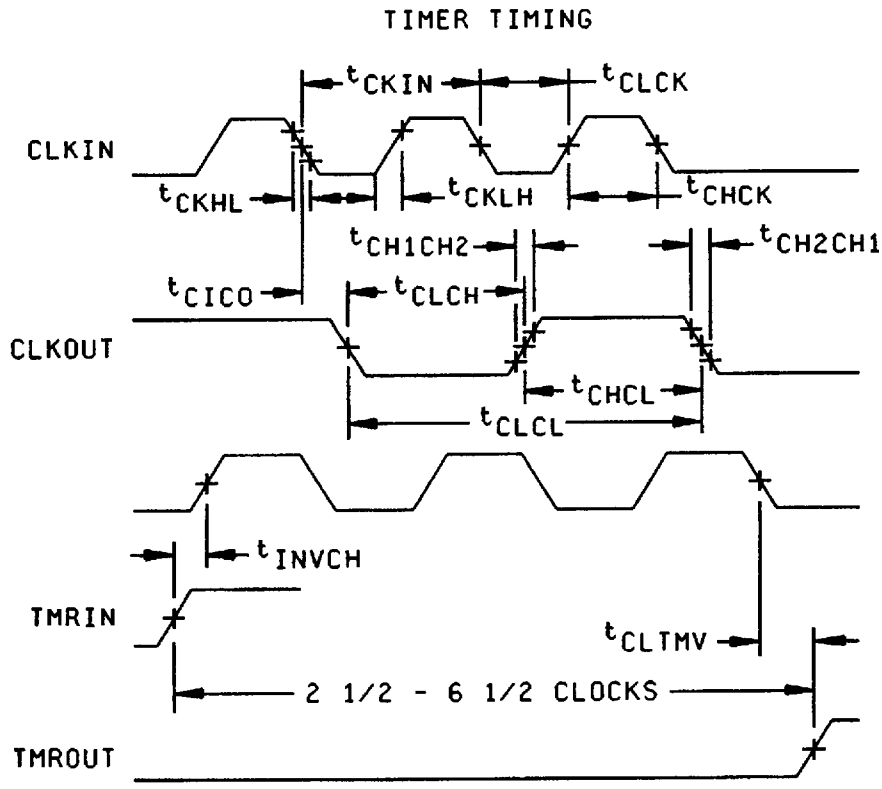


FIGURE 4. Timing waveforms - Continued.

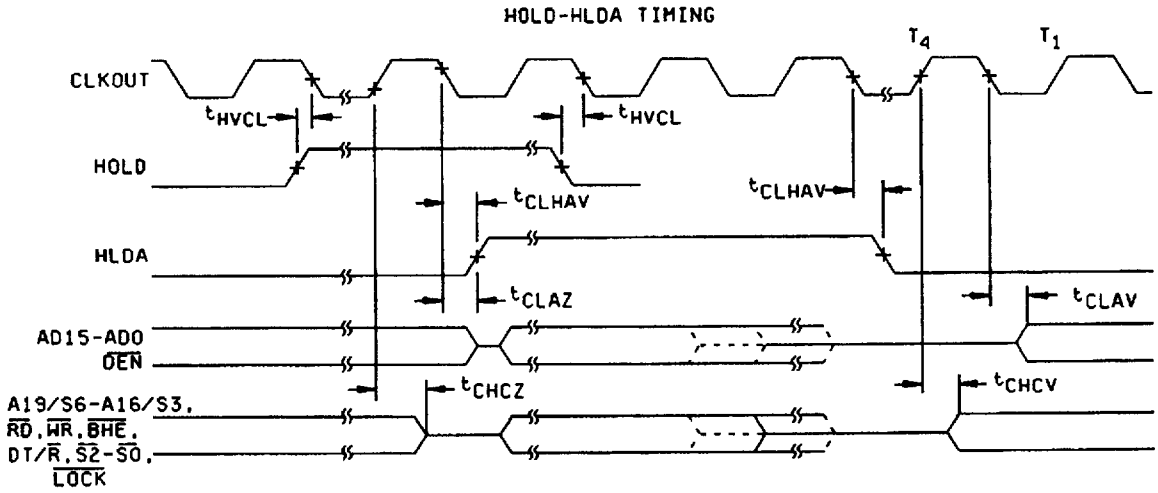


FIGURE 4. Timing waveforms - Continued.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 8A, 10

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of five devices with zero rejects shall be required

d. Subgroups 7 and 8 functional testing shall include verification of the instruction set (see Table III).

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein).

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal .

TABLE III. Instruction set summary.

Function	Format	Clock cycles	Comments
Data transfer			
MOV = Move:			
Register to register/memory	1 0 0 0 1 0 0 w mod reg r/m	2/12	
Register/memory to register	1 0 0 0 1 0 1 w mod reg r/m	2/9	
Immediate to register/memory	1 1 0 0 0 1 1 w mod 0 0 0 r/m data data if w = 1	12-13	8/16-bit
Immediate to register	1 0 1 1 w reg data data if w = 1	3-4	8/16-bit
Memory to accumulator	1 0 1 0 0 0 0 w addr-low addr-high	9	
Accumulator to memory	1 0 1 0 0 0 1 w addr-low addr-high	8	
Register/memory to segment register	1 0 0 0 1 1 1 0 mod 0 reg r/m	2/9	
Segment register to register/ memory	1 0 0 0 1 1 0 0 mod 0 reg r/m	2/11	
PUSH = Push:			
Memory	1 1 1 1 1 1 1 1 mod 1 1 0 r/m	16	
Register	0 1 0 1 0 reg	10	
Segment register	0 0 0 reg 1 1 0	9	
Immediate	0 1 1 0 1 0 s 0 data data if s = 0	10	
PUSHA = Push All	0 1 1 0 0 0 0 0	36	
POP = Pop:			
Memory	1 0 0 0 1 1 1 1 mod 0 0 0 r/m	20	
Register	0 1 0 1 1 reg	10	
Segment register	0 0 0 reg 1 1 1 (reg ≠ 01)	8	
POPA = Pop All	0 1 1 0 0 0 0 1	51	
XCHG = Exchange:			
Register/memory with register	1 0 0 0 0 1 1 w mod reg r/m	4/17	
Register with accumulator	1 0 0 1 0 reg	3	
IN = Input from:			
Fixed port	1 1 1 0 0 1 0 w port	10	
Variable port	1 1 1 0 1 1 0 w	8	

TABLE III. Instruction set summary - Continued.

Function	Format	Clock cycles	Comments
OUT = Output to:			
Fixed port	1 1 1 0 0 1 1 w port	9	
Variable port	1 1 1 0 1 1 1 w	7	
XLAT = Translate byte to AL	1 1 0 1 0 1 1 1	11	
LEA = Load EA to register	1 0 0 0 1 1 0 1 mod reg r/m	6	
LDS = Load pointer to DS	1 1 0 0 0 1 0 1 mod reg r/m (mod ≠ 11)	18	
LES = Load pointer to ES	1 1 0 0 0 1 0 0 mod reg r/m (mod ≠ 11)	18	
LAHF = Load AH with flags	1 0 0 1 1 1 1 1	2	
SAHF = Store AH into flags	1 0 0 1 1 1 1 0	3	
PUSHF = Push flags	1 0 0 1 1 1 0 0	9	
POPF = Pop flags	1 0 0 1 1 1 0 1	8	
SEGMENT = Segment Override:			
CS	0 0 1 0 1 1 1 0	2	
SS	0 0 1 1 0 1 1 0	2	
DS	0 0 1 1 1 1 1 0	2	
ES	0 0 1 0 0 1 1 0	2	
ARITHMETIC			
ADD = Add:			
Reg/memory with register to either	0 0 0 0 0 0 d w mod reg r/m	3/10	
Immediate to register/memory	1 0 0 0 0 0 s w mod 0 0 0 r/m data data if s w = 01	4/16	
Immediate to accumulator	0 0 0 0 0 1 0 w data data if w = 1	3/4	8/16-bit
ADC = Add with carry:			
Reg/memory with register to either	0 0 0 1 0 0 d w mod reg r/m	3/10	
Immediate to register/memory	1 0 0 0 0 0 s w mod 0 1 0 r/m data data if s w=01	4/16	
Immediate to accumulator	0 0 0 1 0 1 0 w data data if w = 1	3/4	8/16-bit
INC = Increment:			
Register/memory	1 1 1 1 1 1 1 w mod 0 0 0 r/m	3/15	
Register	0 1 0 0 0 reg	3	

TABLE III. Instruction set summary - Continued.

Function	Format	Clock cycles	Comments
SUB = Subtract:			
Reg/memory and register to either	0 0 1 0 1 0 d w mod reg r/m	3/10	
Immediate from register/memory	1 0 0 0 0 0 s w mod 1 0 1 r/m data data if s w = 01	4/16	
Immediate from accumulator	0 0 1 0 1 1 0 w data data if w = 1	3/4	8/16-bit
SBB = Subtract with borrow:			
Reg/memory and register to either	0 0 0 1 1 0 d w mod reg r/m	3/10	
Immediate from register/memory	1 0 0 0 0 0 s w mod 0 1 1 r/m data data if s w = 01	4/16	
Immediate from accumulator	0 0 0 1 1 1 0 w data data if w = 1	3/4	8/16-bit
DEC = Decrement:			
Register/memory	1 1 1 1 1 1 1 w mod 0 0 1 r/m	3/15	
Register	0 1 0 0 1 reg	3	
CMP = Compare:			
Register/memory with register	0 0 1 1 1 0 1 w mod reg r/m	3/10	
Register with register/memory	0 0 1 1 1 0 0 w mod reg r/m	3/10	
Immediate with register/memory	1 0 0 0 0 0 s w mod 1 1 1 r/m data data if s w = 01	3/10	
Immediate with accumulator	0 0 1 1 1 1 0 w data data if w = 1	3/4	8/16-bit
NEG = Change sign	1 1 1 1 0 1 1 w mod 0 1 1 r/m	3/10	
AAA = ASCII adjust for add	0 0 1 1 0 1 1 1	8	
DAA = Decimal adjust for add	0 0 1 0 0 1 1 1	4	
AAS = ASCII adjust for subtract	0 0 1 1 1 1 1 1	7	
DAS = Decimal adjust for substract	0 0 1 0 1 1 1 1	4	
MUL = Multiply (unsigned):	1 1 1 1 0 1 1 w mod 1 0 0 r/m		
Register-Byte		26-28	
Register-Word		35-37	
Memory-Byte		32-34	
Memory-Word		41-43	
IMUL = Integer multiply (signed):	1 1 1 1 0 1 1 w mod 1 0 1 r/m		
Register-Byte		25-28	
Register-Word		34-37	
Memory-Byte		31-34	
Memory-Word		40-43	

TABLE III. Instruction set summary - Continued.

Function	Format	Clock cycles	Comments
ARITHMETIC (Continued):			
IMUL = Integer immediate multiply (signed)	0 1 1 0 1 0 s 1 mod reg r/m data data if s = 0	22-25/ 29-32	
DIV = Divide (unsigned):	1 1 1 1 0 1 1 w mod 1 1 0 r/m		
Register-Byte		29	
Register-Word		38	
Memory-Byte		35	
Memory-Word		44	
IDIV = Integer divide (signed):	1 1 1 1 0 1 1 w mod 1 1 1 r/m		
Register-Byte		44-52	
Register-Word		53-61	
Memory-Byte		50-58	
Memory-Word		59-67	
AAM = ASCII adjust for multiply	1 1 0 1 0 1 0 0 0 0 0 0 1 0 1 0	19	
AAD = ASCII adjust for divide	1 1 0 1 0 1 0 1 0 0 0 0 1 0 1 0	15	
CBW = Convert byte to word	1 0 0 1 1 0 0 0	2	
CWD = Convert word to double word	1 0 0 1 1 0 0 1	4	
LOGIC			
Shift/rotate instructions:			
Register/memory by 1	1 1 0 1 0 0 0 w mod TTT r/m	2/15	
Register/memory by CL	1 1 0 1 0 0 1 w mod TTT r/m	5+n/17 +n	
Register/memory by count	1 1 0 0 0 0 0 w mod TTT r/m count	5+n/17 +n	

TTT	Instruction
0 0 0	ROL
0 0 1	ROR
0 1 0	RCL
0 1 1	RCR
1 0 0	SHL/SAL
1 0 1	SHR
1 1 1	SAR

TABLE III. Instruction set summary - Continued.

Function	Format	Clock cycles	Comments
AND = And: Reg/memory and register to either	0 0 1 0 0 0 d w mod reg r/m	3/10	
Immediate to register/memory	1 0 0 0 0 0 0 w mod 1 0 0 r/m data data if w = 1	4/16	
Immediate to accumulator	0 0 1 0 0 1 0 w data data if w = 1	3/4	8/16-bit
TEST = And function to flags, no result: Register/memory and register	1 0 0 0 0 1 0 w mod reg r/m	3/10	
Immediate data and register/ memory	1 1 1 1 0 1 1 w mod 0 0 0 r/m data data if w = 1	4/10	
Immediate data and accumulator	1 0 1 0 1 0 0 w data data if w = 1	3/4	8/16-bit
OR = Or: Reg/memory and register to either	0 0 0 0 1 0 d w mod reg r/m	3/10	
Immediate to register/memory	1 0 0 0 0 0 0 w mod 0 0 1 r/m data data if w = 1	4/16	
Immediate to accumulator	0 0 0 0 1 1 0 w data data if w = 1	3/4	8/16-bit
XOR = Exclusive or: Reg/memory and register to either	0 0 1 1 0 0 d w mod reg r/m	3/10	
Immediate to register/memory	1 0 0 0 0 0 0 w mod 1 1 0 r/m data data if w = 1	4/16	
Immediate to accumulator	0 0 1 1 0 1 0 w data data if w = 1	3/4	8/16-bit
NOT = Invert register/memory	1 1 1 1 0 1 1 w mod 0 1 0 r/m	3/10	
STRING MANIPULATION:			
MOVS = Move byte/word	1 0 1 0 0 1 0 w	14	
CMPS = Compare byte/word	1 0 1 0 0 1 1 w	22	
SCAS = Scan byte/word	1 0 1 0 1 1 1 w	15	
LODS = Load byte/wd to AL/AX	1 0 1 0 1 1 0 w	12	
STOS = Store byte/wd from AL/A	1 0 1 0 1 0 1 w	10	
INS = input byte/wd from DX port	0 1 1 0 1 1 0 w	14	
OUTS = Output byte/wd to DX port	0 1 1 0 1 1 1 w	14	

TABLE III. Instruction set summary - Continued.

Function	Format	Clock cycles	Comments
STRING MANIPULATION (Continued):			
Repeated by count in CX			
MOVS = Move string	1 1 1 1 0 0 1 0 1 0 1 0 0 1 0 w	8+8n	
CMPS = Compare string	1 1 1 1 0 0 1 z 1 0 1 0 0 1 1 w	5+22n	
SCAS = Scan string	1 1 1 1 0 0 1 z 1 0 1 0 1 1 1 w	5+15n	
LODS = Load string	1 1 1 1 0 0 1 0 1 0 1 0 1 1 0 w	6+11n	
STOS = Store string	1 1 1 1 0 0 1 0 1 0 1 0 1 0 1 w	6+9n	
INS = Input string	1 1 1 1 0 0 1 0 0 1 1 0 1 1 0 w	8+8n	
OUTS = Output string	1 1 1 1 0 0 1 0 0 1 1 0 1 1 1 w	8+8n	
CONTROL TRANSFER			
CALL = Call:			
Direct within segment	1 1 1 0 1 0 0 0 disp-low disp-high	15	
Register/memory indirect within segment	1 1 1 1 1 1 1 1 mod 0 1 0 r/m	13/19	
Direct intersegment	1 0 0 1 1 0 1 0 segment offset segment selector	23	
Indirect intersegment	1 1 1 1 1 1 1 1 mod 0 1 1 r/m	38	
JMP = Unconditional jump:			
Short/long	1 1 1 0 1 0 1 1 disp-low	14	
Direct within segment	1 1 1 0 1 0 0 1 disp-low disp-high	14	
Register/memory indirect within segment	1 1 1 1 1 1 1 1 mod 1 0 0 r/m	11/17	
Direct intersegment	1 1 1 0 1 0 1 0 segment offset segment selector	14	
Indirect intersegment	1 1 1 1 1 1 1 1 mod 1 0 1 r/m	26	
RET = Return from CALL:			
Within segment	1 1 0 0 0 0 1 1	16	
Within seg adding immed to SP	1 1 0 0 0 0 1 0 data-low data-high	18	
Intersegment	1 1 0 0 1 0 1 1	22	
Intersegment adding immediate to SP	1 1 0 0 1 0 1 0 data-low data-high	25	

TABLE III. Instruction set summary - Continued.

Function	Format		Clock cycles	Comments
CONTROL TRANSFER (Continued):				
JE/JZ = Jump on equal/zero	0 1 1 1 0 1 0 0	disp	4/13	JMP not taken/JMP taken
JL/JNGE = Jump on less/not greater or equal	0 1 1 1 1 1 0 0	disp	4/13	
JLE/JNG = Jump on less or equal/ not greater	0 1 1 1 1 1 1 0	disp	4/13	
JB/JNAE = Jump on below/not above or equal	0 1 1 1 0 0 1 0	disp	4/13	
JBE/JNA = Jump on below or equal/not above	0 1 1 1 0 1 1 0	disp	4/13	
JP/JPE = Jump on parity/parity even	0 1 1 1 1 0 1 0	disp	4/13	
JO = Jump on overflow	0 1 1 1 0 0 0 0	disp	4/13	
JS = Jump on sign	0 1 1 1 1 0 0 0	disp	4/13	
JNE/JNZ = Jump on not equal/ not zero	0 1 1 1 0 1 0 1	disp	4/13	
JNL/JGE = Jump on not less/ greater or equal	0 1 1 1 1 1 0 1	disp	4/13	
JNLE/JG = Jump on not less or equal/greater	0 1 1 1 1 1 1 1	disp	4/13	
JNB/JAE = Jump on not below/ above or equal	0 1 1 1 0 0 1 1	disp	4/13	
JNBE/JA = Jump on not below or equal/above	0 1 1 1 0 1 1 1	disp	4/13	
JNP/JPO = Jump on not par/par odd	0 1 1 1 1 0 1 1	disp	4/13	
JNO = Jump on not overflow	0 1 1 1 0 0 0 1	disp	4/13	
JNS = Jump on not sign	0 1 1 1 1 0 0 1	disp	4/13	
JCXZ = Jump on CX zero	1 1 1 0 0 0 1 1	disp	5/15	
LOOP = Loop CX times	1 1 1 0 0 0 1 0	disp	6/16	
LOOPZ/LOOPE = Loop while zero/ equal	1 1 1 0 0 0 0 1	disp	6/16	LOOP not taken/LOOP taken
LOOPNZ/LOOPNE = Loop while not zero/equal	1 1 1 0 0 0 0 0	disp	6/16	

TABLE III. Instruction set summary - Continued.

Function	Format	Clock cycles	Comments
ENTER = Enter procedure	1 1 0 0 1 0 0 0 data-low data-high L		
L = 0		15	
L = 1		25	
L > 1		22+16 (n-1)	
LEAVE = Leave procedure	1 1 0 0 1 0 0 1	8	
INT = Interrupt:			
Type specified	1 1 0 0 1 1 0 1 type	47	
Type 3	1 1 0 0 1 1 0 0	45	if INT. taken/
INTO = Interrupt on overflow	1 1 0 0 1 1 1 0	48/4	if INT. not taken
IRET = Interrupt return	1 1 0 0 1 1 1 1	28	
BOUND = Detect value out of range	0 1 1 0 0 0 1 0 mod reg r/m	33-35	
PROCESSOR CONTROL			
CLC = Clear carry	1 1 1 1 1 0 0 0	2	
CMC = Complement carry	1 1 1 1 0 1 0 1	2	
STC = Set carry	1 1 1 1 1 0 0 1	2	
CLD = Clear direction	1 1 1 1 1 1 0 0	2	
STD = Set direction	1 1 1 1 1 1 0 1	2	
CLI = Clear interrupt	1 1 1 1 1 0 1 0	2	
STI = Set interrupt	1 1 1 1 1 0 1 1	2	
HLT = Halt	1 1 1 1 0 1 0 0	2	
WAIT = Wait	1 0 0 1 1 0 1 1	6	if $\overline{\text{test}}$ = 0
LOCK = Bus lock prefix	1 1 1 1 0 0 0 0	2	
ESC = Processor Extension Escape	1 0 0 1 1 T T T mod LLL r/m (TTT LLL are opcode to processor extension)	6	

TABLE III. Instruction set summary - Continued.

The effective address (EA) of the memory operand is computed according to the mod and r/m fields:

if mod = 11 then r/m is treated as a REG field

if mod = 00 then DISP = 0*, disp-low and disp-high are absent

if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent

if mod = 10 then DISP = disp-high: disp-low

if r/m = 000 then EA = (BX) + (SI) + DISP

if r/m = 001 then EA = (BX) + (DI) + DISP

if r/m = 010 then EA = (BP) + (SI) + DISP

if r/m = 011 then EA = (BP) + (DI) + DISP

if r/m = 100 then EA = (SI) + DISP

if r/m = 101 then EA = (DI) + DISP

if r/m = 110 then EA = (BP) + DISP*

if r/m = 111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (before data if required)

*Except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

EA calculation time is 4 clock cycles for all modes, and is included in the execution times given whenever appropriate.

SEGMENT OVERRIDE PREFIX

| 0 0 1 reg 1 1 0 |

reg is assigned according to the following:

reg	Segment Register
00	ES
01	CS
10	SS
11	DS

TABLE III. Instruction set summary - Continued.

REG is assigned according to the following table:

16-Bit(w = 1)	8-Bit(w = 0)
000 AX	000 AL
001 CX	001 CL
010 DX	010 DL
011 BX	011 BL
100 SP	100 AH
101 BP	101 CH
110 SI	110 DH
111 DI	111 BH

The physical addresses of all operands addressed by the BP register are computed using the SS segment register. The physical addresses of the destination operands of the string primitive operations (those addressed by the DI register) are computed using the ES segment, which may not be overridden.

6.4 Symbols, definitions, and functional descriptions. The symbols, definitions, and functional descriptions for this device shall be as follows:

Symbol	Name and function
V_{CC}	System power: +5 volt power supply.
V_{SS}	System ground.
RESET	Reset output indicates that the devuce CPU is being reset, and can be used as a system reset. It is active HIGH, synchronized with the processor clock, and lasts an integer number of clock periods corresponding to the length of the $\overline{RES}$ signal. Reset goes inactive 2 clockout periods after $\overline{RES}$ goes inactive. When tied to the TEST/$\overline{BUSY}$ pin, Reset forces the devices into enhanced mode.

X1, X2	Crystal inputs, X1 and X2, provide an external connections for a fundamental mode or third overtone parallel resonant crystal for the internal oscillator. X1 can interface to an external clock instead of a crystal. In this case, minimize the capacitance on X2 or drive X2 with complemented X1. The input or oscillator frequency is internally divided by two to generate the clock signal (CLKOUT).
CLKOUT	Clock output provides the system with a 50 percent duty cycle waveform. All device pin timings are specified relative to CLKOUT. CLKOUT has sufficient MOS drive capabilities for the numeric processor extension.
$\overline{RES}$	System reset causes the device to immediately terminate its present activity, clear the internal logic, and enter a dormant state. This signal may be asynchronous to the device clock. The device begins fetching instructions approximately 61/2 clock cycles after $\overline{RES}$ is returned HIGH. For proper initialization, V_{CC} must be within specifications and the clock signal must be stable for more than 4 clocks with $\overline{RES}$ held low. $\overline{RES}$ is internally synchronized. This input is provided with a Schmitt-trigger to facilitate power-on $\overline{RES}$ generation via an RC network. When $\overline{RES}$ occurs, the device will drive the status lines to an inactive level for one clock, and then float them.
$\overline{TEST}$/BUSY	The $\overline{TEST}$ pin is sampled during and after reset to determine whether the device is to enter compatible or enhanced mode. Enhanced mode requires $\overline{TEST}$ to be high on the rising edge of $\overline{RES}$ and low four clocks later. Any other combination will place the device in compatible mode. A weak internal pullup insures a high state when the pin is not driven. $\overline{TEST}$, in compatible mode this pin is configured to operate as $\overline{TEST}$. This pin is examined by the WAIT instruction. If the $\overline{TEST}$ input is high when WAIT execution begins, instruction execution will suspend. $\overline{TEST}$ will be resampled every five clocks until it goes low, at which time execution will resume. If interrupts are enabled while the device is waiting for $\overline{TEST}$, interrupts will be serviced. BUSY, in enhanced mode, this pin is configured to operate as BUSY. The BUSY input is used to notify the device of numerics processor extension activity. Floating point instructions executing in the device sample the BUSY pin to determine when the numeric processor is ready to accept a new command. BUSY is active high.
TMR IN 0, TMR IN 1	Timer inputs are used either as clock or control signals, depending upon the programmed timer mode. These inputs are active high (or low-to-high transitions are counted) and internally synchronized.
TMR OUT 0, TMR OUT 1	Timer outputs are used to provide single pulse or continuous waveform generation, depending upon the timer mode selected.
DRQ0, DRQ1	DMA request is driven high by an external device when it desires that a DMA (channel 0 or 1) perform a transfer. These signals are active high, level-triggered, and internally synchronized.
NMI	Nonmaskable interrupt is an edge-triggered input which causes a type 2 interrupt. NMI is not maskable internally. A transition from a low to high initiates the interrupt at the next instruction boundary. NMI is latched internally. An NMI duration of one clock or more will guarantee service. This input is internally synchronized.
INT0, INT1, INT2/$\overline{INTA0}$, INT3/$\overline{INTA1}$	Maskable interrupt requests can be requested by activating one of these pins. When configured as inputs, these pins are active high. Interrupt requests are synchronized internally. INT2 and INT3 may be configured via software to provide active-low interrupt-acknowledge output signals. All interrupt inputs may be configured via software to be either edge-or level-triggered. To ensure recognition, all interrupt requests must remain active until the interrupt is acknowledged. When slave mode is selected, the function of these pins changes.

A19/S6,
A18/S5,
A17/S4,
A16/S3

Address bus outputs (16-19) and bus cycle status (3-6) reflect the four most significant address bits during T_1. These signals are active high. During T_2, T_3, T_W, and T_4, status information is available on these lines as encoded below:

	Low	High
S6	Processor cycle	DMA cycle

S3, S4, and S5 are defined as LOW during T_2-T_4.

AD_{15}-AD_0

Address/data bus (0-15) signals constitute the time multiplexed memory or I/O address (T_1) and data (T_2, T_3, T_W, and T_4) bus. The bus is active high A_0 is analogous to $\overline{BHE}$ for the lower byte of the data bus, pins D_7 through D_0. It is low during T_1 when a byte is to be transferred onto the lower portion of the bus in memory of I/O operations.

$\overline{BHE}$/S7

The $\overline{BHE}$ (bus high enable) signal is analogous to A0 in that it is used to enable data on to the most significant half of the data bus, pins D15-D8. BHE will be low during T_1 when the upper byte is transferred and will remain low through T_3 and T_W. $\overline{BHE}$ does not need to be latched $\overline{BHE}$ will float during hold or reset. In enhanced mode, $\overline{BHE}$ will also be used to signify DRAM refresh cycles. A refresh cycle is indicated by $\overline{BHE}$ and A0 being high.

$\overline{BHE}$ and A0 encodings

$\overline{BHE}$ value	A0 value	Function
0	0	Word transfer
0	1	Byte transfer on upper half of data bus (D_{15}-D_8)
1	0	Byte transfer on lower half of data bus (D_7-D_0)
1	1	Refresh

ALE/QS0

Address latch enable/queue status 0 is provided by the device to latch the address. ALE is active high. Addresses are guaranteed to be valid on the trailing edge of ALE. The ALE rising edge is generated off the rising edge of the CLKOUT immediately preceding T_1 of the associated bus cycle. The trailing edge is generated off the CLKOUT rising edge in T_1. Note that ALE is never floated.

$\overline{WR}$/QS1

Write strobe/queue status 1 indicates that the data on the bus is to be written into a memory or an I/O device. $\overline{WR}$ is active for T_2, T_3, and T_W of any write cycle. It is active low, and floats during "HOLD" or "Reset". It is driven high for one clock during reset, and then floated. When the device is in queue status mode, the ALE/QS0 and $\overline{WR}$/QS1 pins provide information about processor instruction queue interaction.

QS1	QS0	Queue operation
0	0	No queue operation
0	1	First opcode byte fetched from the queue
1	1	Subsequent byte fetched from the queue
1	0	Empty the queue

$\overline{RD}/\overline{QSMD}$ — Read strobe indicates that the device is performing a memory or I/O read cycle. $\overline{RD}$ is active low for T_2, T_3, and T_W of any read cycle. It is guaranteed not to go low in T_2 until after the address bus is floated. $\overline{RD}$ is active low, and floats during "HOLD." $\overline{RD}$ is driven high for one clock during reset, and then the output driver is floated. A weak internal pull-up mechanism on the $\overline{RD}$ line holds it high when the line is not driven. During RESET the pin is sampled to determine whether the device should provide ALE, $\overline{WR}$, and $\overline{RD}$, or if the queue-status should be provided. $\overline{RD}$ should be connected to GND to provide queue-status data.

ARDY — Asynchronous ready informs the device that the addressed memory space or I/O device will complete a data transfer. The ARDY input pin will accept an asynchronous input, and is active high. Only the rising edge is internally synchronized by the device. This means that the falling edge of ARDY must be synchronized to the device clock. If connected to V_{CC}, no WAIT states are inserted. Asynchronous ready (ARDY) or synchronous ready (SRDY) must be active to terminate a bus cycle. If unused, this line should be tied low to yield control to the SRDY pin.

SRDY — Synchronous ready must be synchronized externally to the device. The use of SRDY provides a relaxed system-timing specification on the ready input. This is accomplished by eliminating the one-half clock cycle which is required for internally resolving the signal level when using the ARDY input. This line is active high. If this line is connected to V_{CC}, no WAIT states are inserted. Asynchronous ready (ARDY) or synchronous ready (SRDY) must be active before a bus cycle is terminated. If unused, this line should be tied LOW. If unused, this line should be tied low to yield control to the ARDY pin.

$\overline{S0}$, $\overline{S1}$, $\overline{S2}$ — Bus cycle status $\overline{S0}$-$\overline{S2}$ are encoded to provide bus-transaction information.

device bus cycle status information			
$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Bus cycle initiated
0	0	0	Interrupt acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1	0	0	Instruction fetch
1	0	1	Read data from memory
1	1	0	Write data to memory
1	1	1	Passive (no bus cycle)

The status pins float during "HOLD/HLDA."

$\overline{S2}$ may be used as a logical M/$\overline{IO}$ indicator, and $\overline{S1}$ as a DT/$\overline{R}$ indicator.

The status lines are driven high for one clock during reset, and then floated until a bus cycle begins.

$\overline{LOCK}$	$\overline{LOCK}$ output indicates that other system bus masters are not to gain control of the system bus while $\overline{LOCK}$ is active low. The $\overline{LOCK}$ signal is requested by the $\overline{LOCK}$ prefix instruction and is activated at the beginning of the first data cycle associated with the instruction following the LOCK prefix. It remains active until the completion of the instruction following the LOCK prefix. No prefetches will occur while $\overline{LOCK}$ is asserted. $\overline{LOCK}$ is active low and is driven high for one clock during RESET. $\overline{LOCK}$ on devices 03-06 stay high during reset, while it is floated on the 01 and 02 devices.
HOLD (input) HLDA (output)	HOLD indicates that another bus master is requesting the local bus. The HOLD input is active high. HOLD may be asynchronous with respect to the device clock. The device will issue a HLDA (high) in response to a HOLD request at the end of T_4 or T_1. Simultaneous with the issuance of HLDA the device will float the local bus and control lines. After HOLD is detected as being LOW, the device will lower HLDA. When the device needs to run another bus cycle, it will again drive the local bus and control lines. In enhanced mode, HLDA will go low when a DRAM refresh cycle is pending in the device and an external bus master has control of the bus. It will be up to the external master to relinquish the bus by lowering HOLD so that the device may execute the refresh cycle. Lowering HOLD for four clocks and returning high will insure only one refresh cycle to the external master. HLDA will immediately go active after the refresh cycle has taken place.
$\overline{UCS}$	Upper memory chip select is an active low output whenever a memory reference is made to the defined upper portion (1K-256K block) of memory. This line is not floated during bus HOLD. The address range activating $\overline{UCS}$ is software programmable. $\overline{UCS}$ and $\overline{LCS}$ are sampled upon the rising edge of $\overline{RES}$. If both pins are held low, the device will enter ONCE mode. In ONCE mode all pins assume a high impedance state and remain so until a subsequent RESET. $\overline{UCS}$ has weak internal pullup for normal operation.
$\overline{LCS}$	Lower memory chip select is active LOW whenever a memory reference is made to the defined lower portion (1K-256K) of memory. This line is not floated during bus HOLD. The address range activating $\overline{LCS}$ is software programmable. $\overline{UCS}$ and $\overline{LCS}$ are sampled upon the rising edge of $\overline{RES}$. If both pins are held low, the device will enter ONCE mode. In ONCE mode all pins assume a high impedance state and remain so until a subsequent RESET. $\overline{UCS}$ has weak internal pullup for normal operation.
$\overline{MCS0}$/$\overline{PEREQ}$ $\overline{MCS1}$/$\overline{ERROR}$ $\overline{MCS2}$ $\overline{MCS3}$/$\overline{NPS}$	Mid-range memory chip select signals are active low when a memory reference is made to the defined mid-range portion of memory (8K-512K). These lines are not floated during bus HOLD. The address ranges activating $\overline{MCS0}$-3 are software programmable. In enhanced mode, $\overline{MCS0}$ becomes a $\overline{PEREQ}$ input (processor extension request). When connected to the numerics processor extension, this input is used to signal the device when to make numeric data transfers to and from the NPX. $\overline{MCS3}$ becomes $\overline{NPS}$ (numeric processor select) which may only be activated by communication to the numeric processor extension. $\overline{MCS1}$ becomes $\overline{ERROR}$ in enhanced mode and is used to signal numeric coprocessor errors.
$\overline{PCS0}$ $\overline{PCS1}$-4	Peripheral chip select signals 0-4 are active low when a reference is made to the defined peripheral area (64K byte I/O space). These lines are not floated during bus HOLD. The address ranges activating $\overline{PCS0}$-4 are software programmable.
$\overline{PCS5}$/A1	Peripheral chip select 5 or latched A_1 may be programmed to provide a sixth peripheral chip select, or to provide an internally latched A_1 signal. The address range activating $\overline{PCS5}$ is software programmable. When programmed to provide latched A_1, rather than $\overline{PCS5}$, this pin will retain the previously latched value of A_1 during a bus HOLD. A_1 is active high.

$\overline{PCS6}$/A2	Peripheral chip select 6 or latched A_2 may be programmed to provide a seventh peripheral chip select, or to provide an internally latched A_2 signal. The address range activating $\overline{PCS6}$ is software programmable. When programmed to provide latched A_2, rather than $\overline{PCS6}$, this pin will retain the previously latched value of A_2 during a bus HOLD. A_2 is active HIGH.
DT/$\overline{R}$	Data transmit/receive controls the direction of data flow through the external data bus transceiver. When low, data is transferred to the device. When high the device places write data on the data bus.
$\overline{DEN}$	Data enable is provided as a data bus transceiver output enable. $\overline{DEN}$ is active low during each memory and I/O access. $\overline{DEN}$ is high whenever DT/$\overline{R}$ changes state.

6.5 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.6 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.7 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.