REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

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	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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APPROVED BY

DRAWING APPROVAL DATE 20 JANUARY 1989

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, MEMORY, DIGITAL, CMOS 512X8, PROM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-88690

SHEET 1 OF 14

DESC FORM 193
SEP 87

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5962-E987

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-88690	01	J	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	(See 6.4)	512 X 8 CMOS PROM	220 ns
02	(See 6.4)	512 X 8 CMOS PROM	140 ns

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
J	D-3 (24-lead, 1.290" x .610" x .225"), dual-in-line package
L	D-9 (24-lead, 1.280" x .310" x .200"), dual-in-line package
3	C-4 (28-terminal, .460" x .460" x .100"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage to ground potential - - - - - - - - - -	-0.3 V dc to +7.0 V dc
DC voltage applied to outputs- - - - - - - - - - - -	-0.3 V dc to V_{CC} +0.3 V dc
DC input voltage range - - - - - - - - - - - - - - - -	-0.3 V dc to V_{CC} +0.3 V dc
Storage temperature range- - - - - - - - - - - - - -	-65°C to +150°C
Maximum power dissipation (P_D) - - - - - - - - - - -	1.0 W
Lead temperature (soldering, 10 seconds) - - - - - -	+275°C
Thermal resistance, junction-to-case (θ_{JC}): Cases J, L, and 3- - - - - - - - - - - - - - - - -	See MIL-M-38510, appendix C
Junction temperature (T_J)- - - - - - - - - - - - - - -	+150°C 1/

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) - - - - - - - - - - - - - -	4.5 V dc to 5.5 V dc
High level input voltage range (V_{IH}) - - - - - - - - -	+2.4 V dc to V_{CC} +0.3 V dc
Low level input voltage range (V_{IL})- - - - - - - - - -	-0.3 V dc to +0.8 V dc
Case operating temperature range (T_C)- - - - - - - - -	-55°C to +125°C

1/ Maximum junction temperature may be increased to +175°C during burn-in and steady-state life.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.2.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, or C inspection (see 4.3), the devices shall be programmed by the manufacturer prior to test in a checkerboard pattern (a minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of bits programmed.

3.2.2.2 Programmed devices. The requirements for supplying programmed devices are not part of this drawing.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55^\circ C \le T_C \le +125^\circ C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified 1/		Group A subgroups	Device types	Limits Min	Limits Max	Unit
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -1.0 mA		1,2,3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 3.2 mA		1,2,3	All		0.4	V
Input leakage current (except P input)	I_I	V_{CC} = 5.5, 0 V $\le$ VIN $\le$ 5.5 V		1,2,3	All	-1.0	1.0	µA
Output leakage current, high impedance	I_{OZ}	V_{CC} = 5.5 V, $\overline{G}$ = 5.5 V, GND $\le V_{I/O} \le V_{CC}$		1,2,3	All	-1.0	1.0	µA
Operating supply current	I_{CC}	V_{CC} = 5.5 V, $\overline{G} = V_{CC}$, I_{OUT} = 0 mA, f = 1 MHz 0 V $\le V_{IN} \le$ 5.5 V		1,2,3	All		20	mA
Standby supply current	I_{SB}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, 0 V $\le V_{IN} \le$ 5.5 V		1,2,3	All		100	µA
Input capacitance	C_{IN}	V_{CC} = open, f = 1.0 MHz, T_A = +25°C, see 4.3.1.c, All measurements are referenced to device ground	Case J	4	All		10	pF
			Case L				13	
			Case 3				8.0	
Input/output capacitance	C_{OUT}	V_{CC} = open, f = 1.0 MHz, T_A = +25°C, see 4.3.1c, All measurements are referenced to device ground	Case J	4	All		12	pF
			Case L				15	
			Case 3				10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^\circ C \le T_C \le +125^\circ C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified 1/	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Address access time	t_{AVQV}	See figures 3 and 4 2/	9,10,11	01		220	ns
				02		140	
Output enable access time	t_{GVQV}		9,10,11	01		150	ns
				02		50	
Chip enable access time	t_{ELQV}		9,10,11	01		200	ns
				02		120	
Address setup time	t_{AVEL}		9,10,11	01	20		ns
				02	20		
Address hold time	t_{ELAX}		9,10,11	01	60		ns
				02	25		
Chip enable low pulse width	t_{ELEH}		9,10,11	01	200		ns
				02	120		
Chip enable high pulse width	t_{EHEL}		9,10,11	01	150		ns
				02	40		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^\circ C \le T_C \le +125^\circ C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified 1/	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Read cycle time	t_{ELEL}	See figures 3 and 4 2/	9,10,11	01	350		ns
				02	160		
Output enable time	t_{GVQX} 3/		9,10,11	01	5.0	150	ns
				02	5.0	50	
Output disable time	t_{GXQZ} 3/		9,10,11	01		150	ns
				02		50	

1/ All measurements are performed with P hardwired to GND. See 6.4 2/.

2/ Test conditions assume signal transition times of 5.0 ns or less. Timing is referenced at input and output levels of 1.5 V and input pulse levels of 0 to 3.0 V. Output loading is I_{OL} = +1.0 mA and I_{OH} = -1.0 mA with a load capacitance of 50 pF.

3/ If not tested, shall be guaranteed to limits specified in table I.

Device types	All	
Case outlines	J and L	3
Terminal number	Terminal symbol	
1	A_7	NC
2	A_6	A_7
3	A_5	A_6
4	A_4	A_5
5	A_3	A_4
6	A_2	A_3
7	A_1	A_2
8	A_0	A_1
9	Q_0	A_0
10	Q_1	NC
11	Q_2	Q_0
12	GND	Q_1
13	Q_3	Q_2
14	Q_4	GND
15	Q_5	NC
16	Q_6	Q_3
17	Q_7	Q_4
18	P	Q_5
19	$\overline{E}$	Q_6
20	G3	Q_7
21	$\overline{G2}$	NC
22	$\overline{G1}$	P
23	A_8	$\overline{E}$
24	V_{CC}	G3
25	---	$\overline{G2}$
26	---	$\overline{G1}$
27	---	A_8
28	---	V_{CC}

FIGURE 1. Terminal connections.

Time reference (See figure 5)	Inputs			Outputs	Function
	$\overline{E}$	$\overline{G}$	A	Q	
-1	H	H	X	Z	Memory disabled
0	¯|_	H	V	Z	Cycle begins-addresses are latched
1	L	L	X	X	Output enabled
2	L	L	X	V	Output valid
3	_|¯	L	X	V	Output latched
4	H	H	X	Z	Read accomplished and output disabled
5	H	H	X	Z	Prepare for next cycle (same as -1)
6	¯|_	H	X	Z	Cycle ends, next cycle begins (same as 0)

H = Logic high voltage level

L = Logic low voltage level

Z = High impedance state

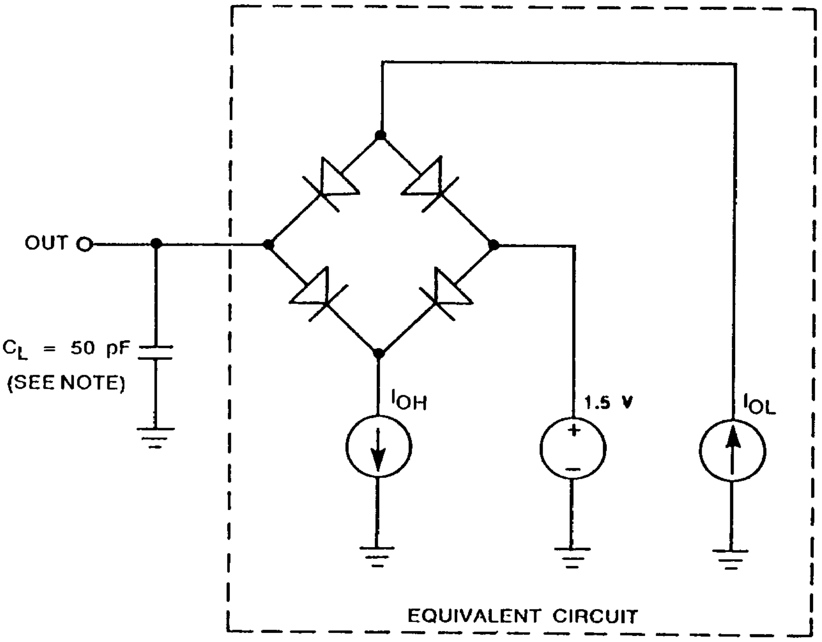
X = Don't care

¯|_ = High-to-low transition

_|¯ = Low-to-high transition

V = Valid

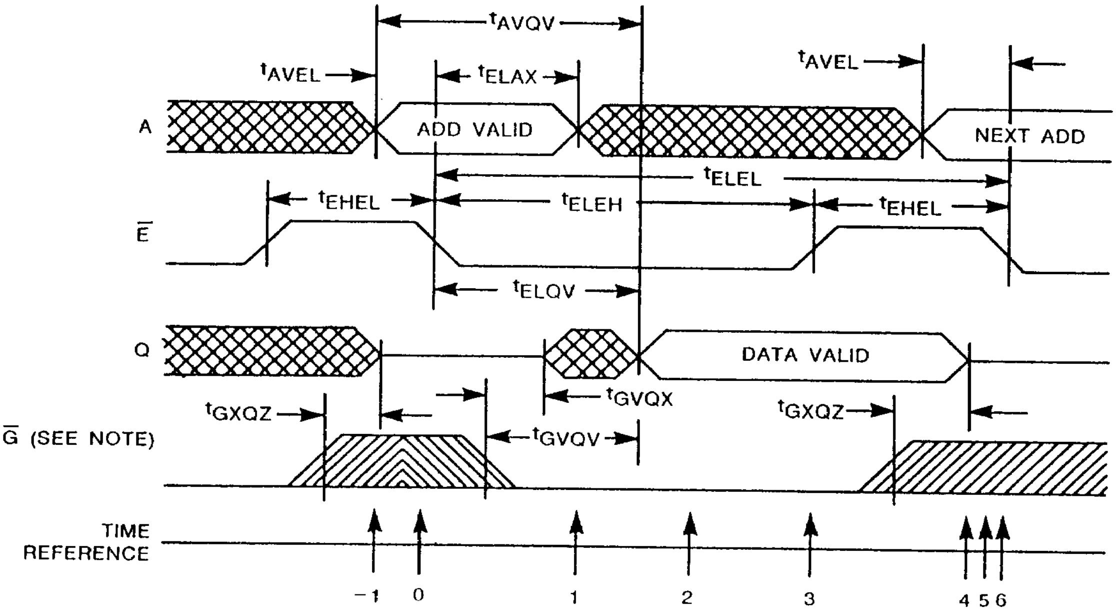
FIGURE 2. Truth table (unprogrammed).



NOTE: C_L = Load capacitance and includes scope and jig capacitance.

FIGURE 3. Output load circuit or equivalent.

READ CYCLE



NOTE: G has the same timing as $\overline{G}$ except signal is inverted.

FIGURE 4. Read cycle waveforms.

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3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Processing options. Since the PROM is an unprogrammed memory capable of being programmed by either the manufacturer or the user to result in a wide variety of PROM configurations, two processing options are provided for selection in the contract, using an altered item drawing.

3.5.1 Unprogrammed PROM delivered to the user. All testing shall be verified through group A testing as defined in 4.3.1. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.5.2 Manufacturer-programmed PROM delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing shall be satisfied by the manufacturer prior to delivery.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

  (1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

  (2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

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4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial characterization and after process or design changes which may affect capacitance. Sample size is fifteen devices with no failures, and all input and output terminals tested.

d. Unprogrammed devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9, 10, and 11.

(1) A sample shall be selected to satisfy programmability requirements prior to performing subgroup 9. Twelve devices shall be submitted to programming (see 3.2.2.1). If more than two devices fail to program, the lot shall be rejected. At the manufacturers option, the sample may be increased to 24 total devices with no more than four total device failures allowable.

(2) Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroup 9, 10, 11. If more than two devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than four total device failures allowable.

e. Subgroups 7 and 8 must verify the truth table as specified on figure 2 herein.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004) for unprogrammed devices	1*,2,3,7,8
Final electrical test parameters (method 5004) for programmed devices	1*,2,3,7,8A,8B, 9,10,11
Group A test requirements (method 5005)	1,2,3,4**,7,8A,8B, 9,10,11
Groups C and D end-point electrical parameters (method 5005)	2,3,7,8

* PDA applies to subgroup 1.
** See 4.3.1c.

4.4 Programming procedures. The programming procedures shall be as specified by the device manufacturer.

4.5 Electrostatic discharge sensitivity (ESDS). Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015 and MIL-M-38510 for initial testing and after any design or process changes which may affect input or output protection circuitry. The option to categorize devices as ESD sensitive without performing the test is not allowed. Only those device types that pass ESDS testing at 1000 volts or greater shall be considered as conforming to the requirements of this drawing.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

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6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 2/
5962-8869001JX 5962-8869001LX 5962-88690013X	34371 34371 34371	HM1-6642/883 HM6-6642/883 HM4-6642/883
5962-8869002JX 5962-8869002LX 5962-88690023X	34371 34371 34371	HM1-6642B/883 HM6-6642B/883 HM4-6642B/883

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

2/ Harris Semiconductor 6642 series, fuse link proms require that program pin P be hardwired to GND except for programming.

Vendor CAGE number	Vendor name and address	Programming procedure	Fusible link
34371	Harris Semiconductor P. O. Box 883 Melbourne, FL 32901	A	Nichrome

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