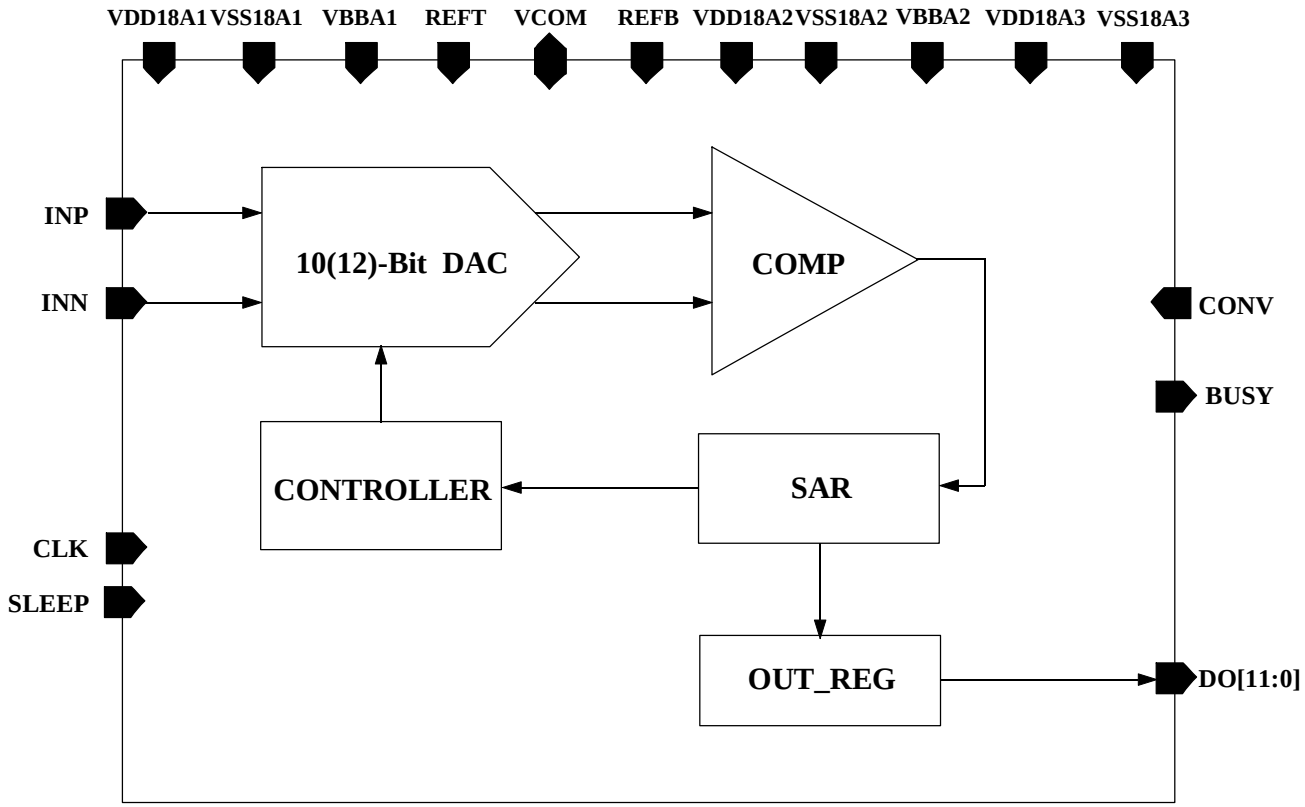
GENERAL DESCRIPTION

The ADC1255X is a CMOS 10-bit low supply, low power, successive approximation A/D converter which is composed of auto-zeroing comparator, 10-bit DAC, clock generator, successive approximation register(SAR) and output register. The 10-bit DAC consists of capacitor arrays and resistor strings. The conversion result can be accessed over a parallel interface. The ADC1255X operates with a single +1.8V power supply and the conversion rate is up to 250KSPS.

FEATURES

- **Resolution: 10-Bit**
- **Differential Linearity Error:±1.0 LSB(Max)**
- **Integral Linearity Error:±2.0 LSB(Typ)**
- **Maximum Conversion Rate: 250KSPS**
- **Low Power Consumption: 2.2mW(Typ)**
- **Power Supply Voltage: 1.8V(Typ)**
- **No Pipeline Delays**
- **No Missing Code Guaranteed**
- **Operation Temperature Range: 0º C~70º C**

FUNCTIONAL BLOCK DIAGRAM



Ver 1.1 (Jan., 2000)

CORE PIN DESCRIPTION

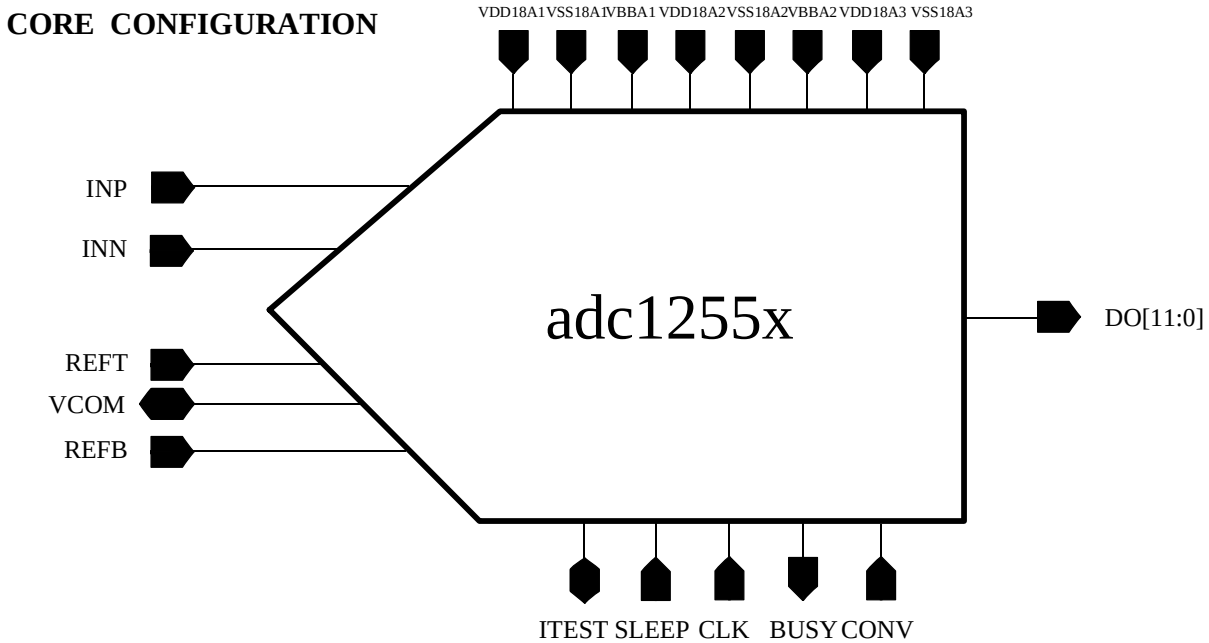
NAME	I/O TYPE	I/O PAD	PIN DESCRIPTION
REFT	AI	pia_abb	Reference Top Voltage
VCOM	AI	pia_abb	Analog Common Voltage; Reference Middle Voltage
REFB	AI	pia_abb	Reference Bottom Voltage
VDD18A1	AP	vdd1t_abb	Analog Power
VBBA1	AG	vbb_abb	Analog Bulk
VSS18A1	AG	vss1t_abb	Analog Ground
INP	AI	piar10_abb	Analog Input(+)
INN	AI	piar10_abb	Analog Input(-)
ITEST	AB	pia_abb	Current Bias Test
SLEEP	DI	picc_abb	SLEEP; Power Saving Mode (Active High)
CLK	DI	picc_abb	Master Clock Input
DO[11:2]	DO	poa_abb	Digital Output Data
DO[1:0]	DO	poa_abb	Extra Digital Output Data
BUSY	DO	poa_abb	No Sleep Mode; BUSY = "HIGH"
CONV	DI	picc_abb	Conversion Control Pin (Active High)
VSS18A2	DG	vss1t_abb	Digital Ground
VBBA2	DG	vbb_abb	Digital Bulk
VDD18A2	DP	vdd1t_abb	Digital Power
VSS18A3	DG	vss1t_abb	Output Buffer Ground
VDD18A3	DP	vdd1t_abb	Output Buffer Power

I/O TYPE ABBR.

- AI : Analog Input
- DI : Digital Input
- AO : Analog Output
- DO : Digital Output
- AP : Analog Power
- AG : Analog Ground
- DP : Digital Power
- DG : Digital Ground

- AB : Analog Bidirection
- DB : Digital Bidirection

CORE CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	VDD	3.3	V
Analog Input Voltage	AIN	VSS to VDD	V
Digital Input Voltage	DIN	VSS to VDD	V
Digital Output Voltage	V_{OH}, V_{OL}	VSS to VDD	V
Reference Voltage	REFT/REFB	VSS to VDD	V
Storage Temperature Range	Tstg	-45 to 150	°C
Operating Temperature Range	Topr	0 to 70	°C

NOTES

1. ABSOLUTE MAXIMUM RATING specifies the values beyond which the device may be damaged permanently. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and function operation under any of these conditions is not implied.
2. All voltages are measured with respect to VSS unless otherwise specified.
3. 100pF capacitor is discharged through a 1.5kΩ resistor (Human body model)

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	VDD18A1 VDD18A2 VDD18A3	1.7	1.8	-	V
Reference Input Voltage	REFT REFB	-	1.35 0.45	-	V
Analog Input Voltage	INP INN	0.0	- 0.9	1.8	V
Operating Temperature	Toper	0	-	70	°C

NOTES

It is strongly recommended that all the supply pins (VDD18A1, VDD18A2, VDD18A3) be powered from the same source to avoid power latch-up.

ANALOG SPECIFICATIONS

Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Resolution	-	-	10	-	Bits	
Differential Llinearity Error	DLE	-	-	±1.0	LSB	
Integral Linearity Error	ILE	-	±2	-	LSB	
Offset Voltage Error(Top)	EOT	-	±2.0	-	LSB	
Offset Voltage Error(Bottom)	EOB	-	±2.0	-	LSB	
Conversion Rate	fAD	250	-	-	KSPS	
Conversion Time	tAD	4	-	-	us	
Dynamic Supply Current	Is	-	1.2	2	mA	Conversion Mode
Power Dissipation	Pd	-	2.2	3.6	mW	Conversion Mode

NOTES

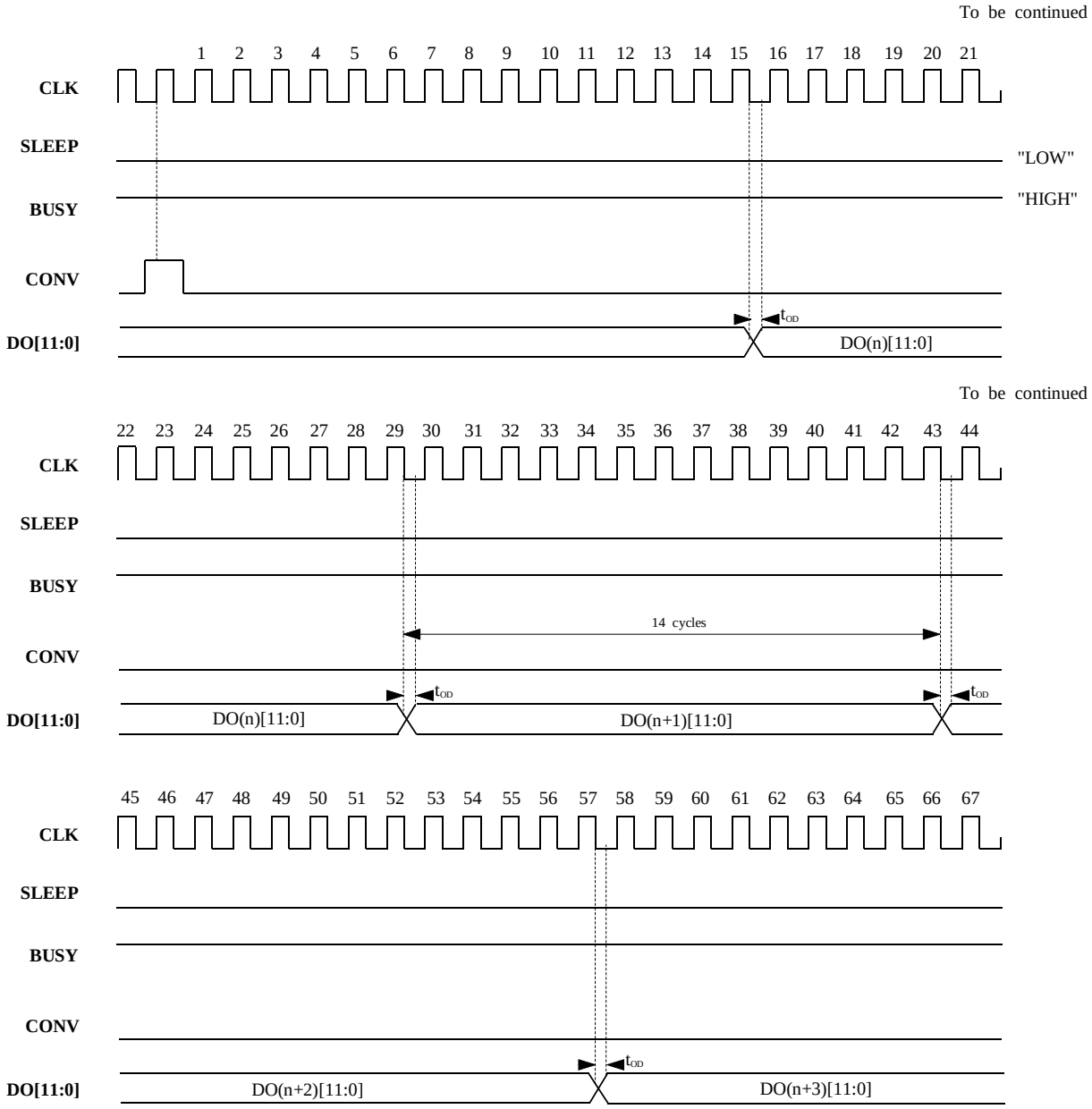
1. Converter Specifications (unless otherwise specified)
   VDD18A1=1.8V VDD18A2=1.8V VDD18A3=1.8V
   VSS18A1=GND VSS18A2=GND VSS18A3=GND
   VBBA1=GND VBBA2=GND
   REFT=1.35V REFB=0.45V
   Ta=25° C
2. TBD : To Be Determined

TIMING SPECIFICATIONS

Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Clock High Time	t_{pwh}	130	-	-	ns	
Clock Low Time	t_{pwl}	130	-	-	ns	
BUSY Signal Output Delay	t_{BD}	10				Output load capacitor = 5pF
ADC Output Delay	t_{OD}	10	-	-	ns	Output load capacitor = 5pF

TIMING DIAGRAM

Conversion Timing



FUNCTIONAL DESCRIPTION

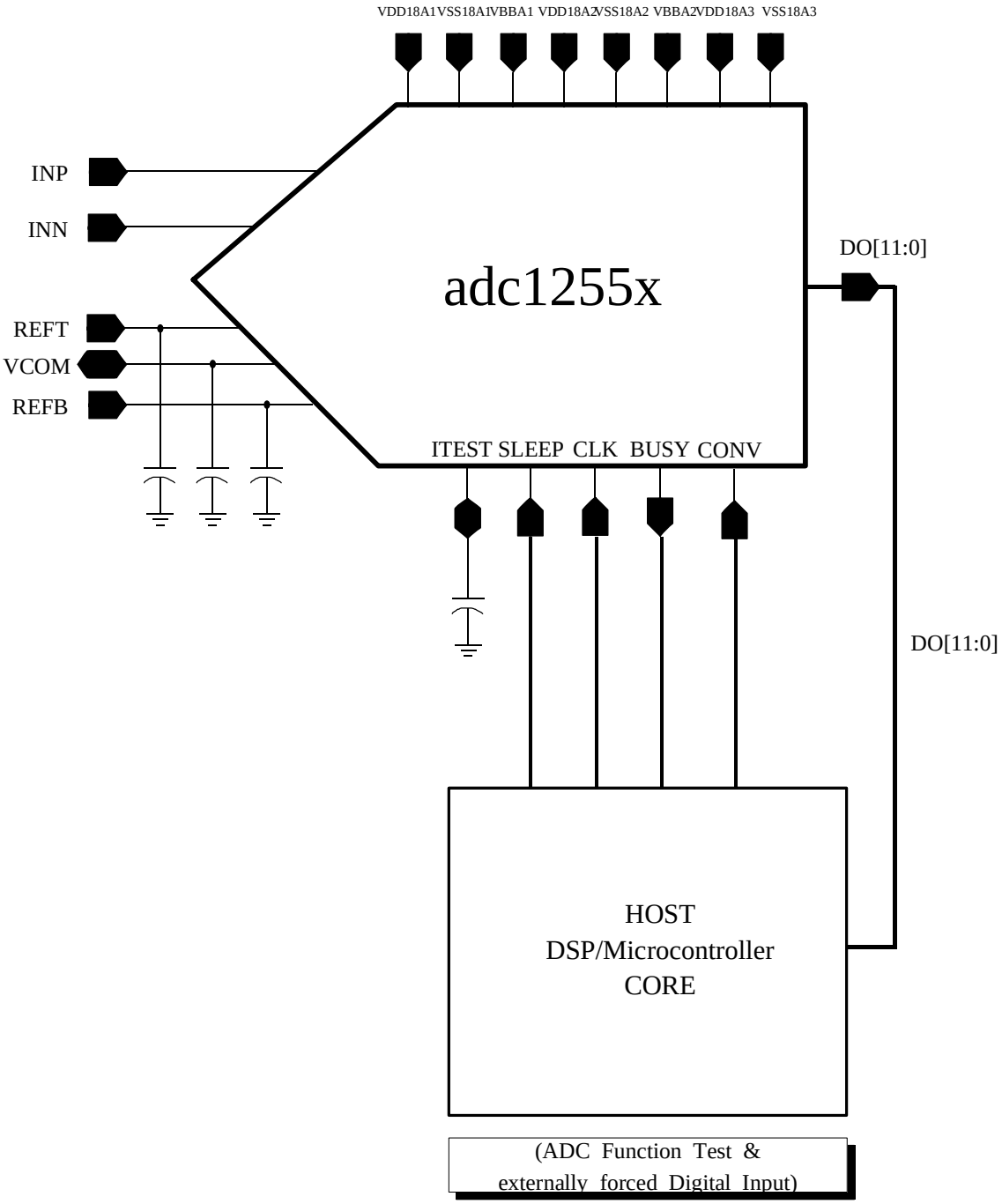
The ADC1255X is a 10-bit analog-to-digital converter including successive approximation register, and parallel output port. The ADC1255X employs a successive approximation technique to determine the value of the analog input voltage. An array of binary-weighted capacitors subdivides the input value to perform the analog to digital conversion.

The conversion of the ADC1255X is controlled by two signals, CONV and CLK. When CONV is taken "HIGH" on the rising edge of CLK, the ADC1255X is internally reset after next two clock cycles, the BUSY pin is driven "HIGH". The CONV pin should be held "HIGH" for at least one CLK cycle. The number of conversion cycles to generate an output data is 14 except the first conversion after the CONV pin is asserted.

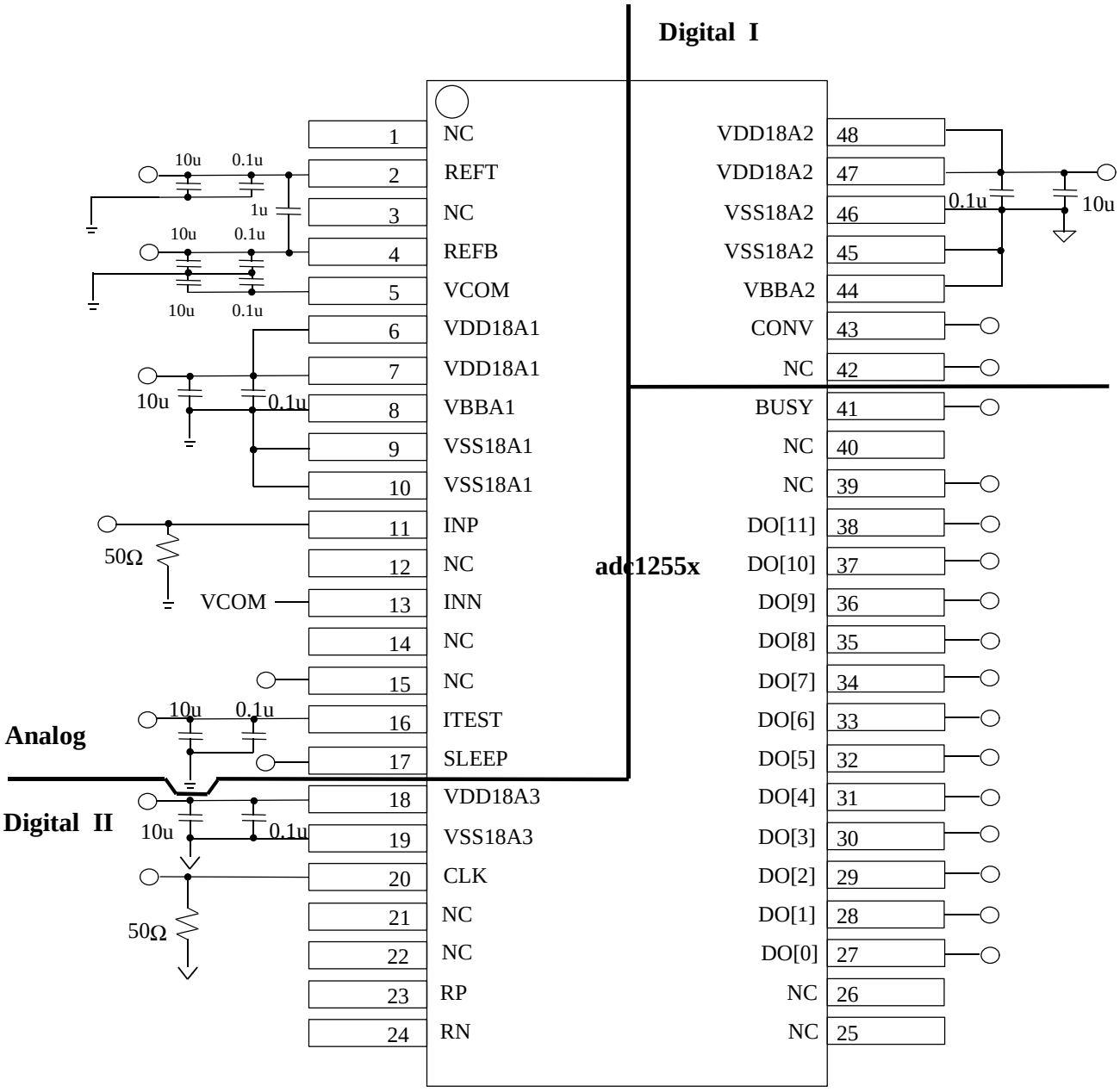
DO[11:2] are actual 10-bit output data with 1.8V power supply. There are extra least significant bits, DO[1:0] for 12-bit resolution when the part is operating with 2.5V power supply.

CORE EVALUATION GUIDE

The reference voltages should be asserted externally through REFT and REFB pins



PACKAGE CONFIGURATION



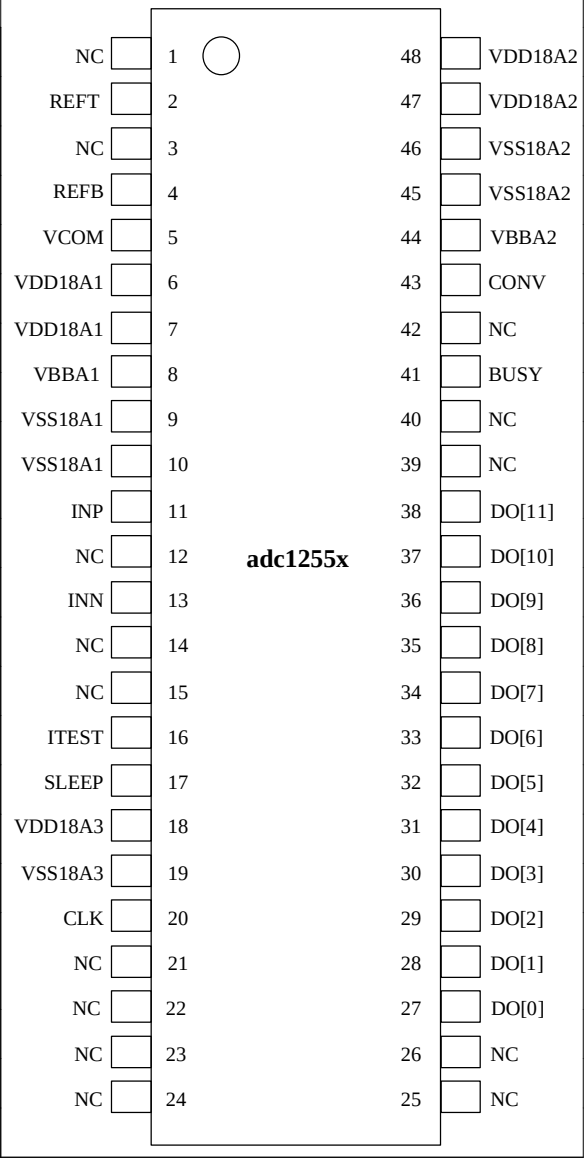
NOTES

1. ESD (Electro Static Discharge) sensitive device. Although the digital control inputs are diode protected, permanent damage may occur on devices subjected to high electrostatic discharges. It is recommended that unused devices be stored in conductive foam or shunts to avoid performance degradation or loss of functionality. The protective foam should be discharged to the destination socket before devices are inserted.
2. NC denotes "No Connection".

PACKAGE PIN DESCRIPTION

No.	NAME	I/O TYPE	PIN DESCRIPTION
2	REFT	AI	Reference Top Voltage
4	REFB	AI	Reference Bottom Voltage
5	VCOM	AB	Reference Middle Voltage
6, 7	VDD18A1	AP	Analog Power
8	VBBA1	AG	Analog Bulk
9, 10	VSS18A1	AG	Analog Ground
11	INP	AI	Analog Input (+)
13	INN	AI	Analog Input (-)
16	ITEST	AB	open; use internal bias circuit
17	SLEEP	DI	Sleep; Power Saving Mode (Active High)
18	VDD18A3	PP	Output Buffer Power
19	VSS18A3	PG	Output Buffer Ground
20	CLK	DI	Master Clock Input
27,28	DO[0:1]	DO	Extra Digital Output
29	DO[2]	DO	Digital Output (LSB)
30~37	DO[3:10]	DO	Digital Output
38	DO[11]	DO	Digital Output (MSB)
41	BUSY	DO	Conversion in Process
43	CONV	DI	Conversion Control Pin (Active High)
44	VBBA2	DG	Digital Bulk
45, 46	VSS18A2	DG	Digital Ground
47, 48	VDD18A2	DP	Digital Power

CONFIGURATION



NOTES

1. I/O TYPE PP and PG denote PAD Power and PAD Ground respectively

USER GUIDE

1. Power Saving Mode
   When the overall system is in sleep, as SLEEP pin goes "HIGH", power consumption of the ADC1255X can be reduced a lot.

2. Power Consumption Optimization
   Yon can optimize power consumption, as the ITEST voltage level is controlled precisely.

3. Analog Input Range
   The analog input range is concerned with the difference voltage, REFT - REFB. In case that the INN pin is connected with VCOM pin, the analog input range of INP pin is equal to 2*(REFT - REFB).

4. Conversion Control
   To operate the ADC1255X in conversion mode, the CONV pin should be set to "HIGH" for more than one clock cycle.

5. Digital Output Data
   DO[11:2] are actual 10-bit output data with 1.8V power supply.

Phantom Cell Information

- Pins of the core can be assigned externally(Package pins) or internally(internal ports) depending on design methods.
  The term "external" implies that the pins should be assigned externally like power pins.
  The term "internal/external" implies that these pins are user dependant

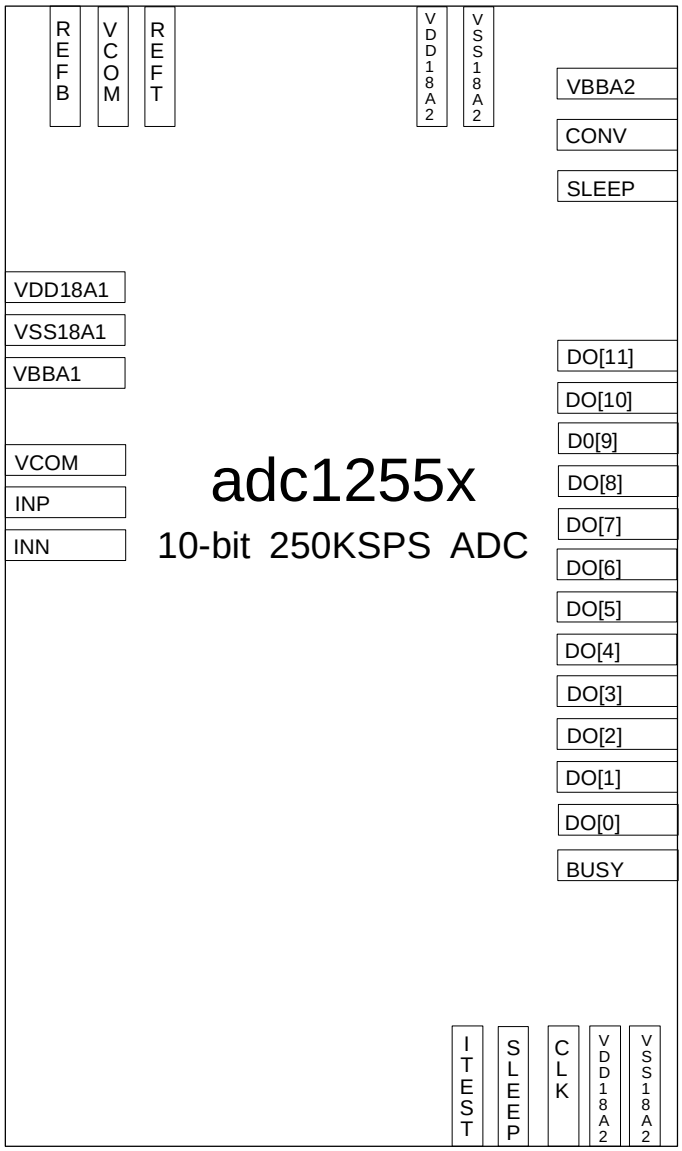


Figure 1. Phantom cell feature

Pin Name	Pin Usage	Pin Layout Guide
VDD18A1	External	- Dedicated power/ground pins - Power cuts are required to provide on-chip isolation - Use good power and source on board
VSS18A1	External	
VBBA1	External	
VDD18A2	External	
VSS18A2	External	
VBBA2	External	
VDD18A3	External	
VSS18A3	External	
REFT	External	- Use good power source - Locate as close as possible to pad - Metal line width should be larger than 10um
VCOM	External	
REFB	External	
INP	External	- Locate as close as possible to pad
INN	External/Internal	- Locate as close as possible to pad - Using this pin internally, INN should be connected to "VCOM" pad directly
ITEST	External/Internal	- It is O.K that ITEST is floating.
CLK	External/Internal	- Don't cross over other signals as possible as it can
CONV	External/Internal	
SLEEP	External/Internal	
DO[11:0]	External/Internal	

Table 1. Pin Layout Guide

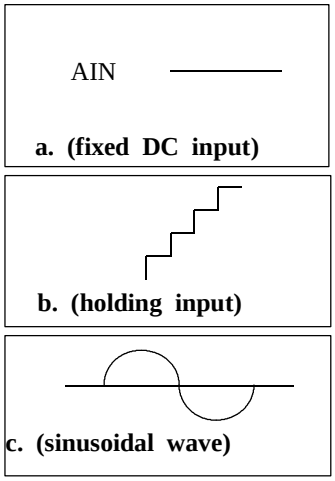
FEEDBACK REQUEST

It should be quite helpful to ADC core development if you specify your system requirements on ADC in the following characteristic checking table and fill out the additional questions.
We appreciate your interest in our products.

Characteristic	Min	Typ	Max	Unit	Remarks
Analog Power Supply Voltage				V	
Digital Power Supply Voltage				V	
Resolution				Bits	
Reference Input Voltage				V	
Analog Input Voltage				Vpp	
Number of Analog Input Channel					
Operating Temperature				ºC	
Integral Linearity Error				LSB	
Differential Linearity Error				LSB	
Bottom Offset Voltage Error				mV	
Top Offset Voltage Error				mV	
Conversion Rate				KSPS	
Conversion Time				us	
Dynamic Supply Current				mA	
Power Dissipation				mW	
Power Dissipation at Power Down				uW	
Digital Output Format (Provide detailed description & timing diagram)					

FEEDBACK REQUEST (To be continued)

1. We want to know the detail of the analog input waveform because sample & hold amplifier is not included in the ADC1255X. Which one is adequate for your analog input waveform among the a, b, and c below. If none of the three is adequate, please describe the analog input waveform to be used. If your analog input signal is a sinusoidal wave as c, please let me know what is the maximum frequency of the analog input signal ? It may be necessary to add a external sample & hold amplifier in any case.



2. Which one is suitable for your system between single ended input and differential input configurations and why ?

3. Please, mention on the internal/external pin configurations and draw the timing diagram as desired.

4. Freely list those functions you want to be implemented in ADC, if any.

HISTORY CARD

Version	Date	Modified Items	Comments
ver 1.0		Original version published (preliminary)	
ver 1.1	2000.01	Release the formal datasheet	