CY7C1471V33
CY7C1473V33
CY7C1475V33

72-Mbit (2M x 36/4M x 18/1M x 72) Flow-Through SRAM with NoBL™ Architecture

Features

- No Bus Latency™ (NoBL™) architecture eliminates dead cycles between write and read cycles
- Supports up to 133 MHz bus operations with zero wait states
- Data is transferred on every clock
- Pin compatible and functionally equivalent to ZBT™ devices
- Internally self timed output buffer control to eliminate the need to use $\overline{OE}$
- Registered inputs for flow through operation
- Byte Write capability
- 3.3V/2.5V IO supply (V_{DDQ})
- Fast clock-to-output times
  - — 6.5 ns (for 133-MHz device)
- Clock Enable ($\overline{CEN}$) pin to enable clock and suspend operation
- Synchronous self timed writes
- Asynchronous Output Enable ($\overline{OE}$)
- CY7C1471V33, CY7C1473V33 available in JEDEC-standard Pb-free 100-Pin TQFP, Pb-free and non-Pb-free 165-Ball FBGA package. CY7C1475V33 available in Pb-free and non-Pb-free 209-Ball FBGA package
- Three Chip Enables ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) for simple depth expansion
- Automatic power down feature available using ZZ mode or CE deselect
- IEEE 1149.1 JTAG Boundary Scan compatible
- Burst Capability — linear or interleaved burst order
- Low standby power

Functional Description [1]

The CY7C1471V33, CY7C1473V33 and CY7C1475V33 are 3.3V, 2M x 36/4M x 18/1M x 72 synchronous flow through burst SRAMs designed specifically to support unlimited true back-to-back read or write operations without the insertion of wait states. The CY7C1471V33, CY7C1473V33 and CY7C1475V33 are equipped with the advanced No Bus Latency (NoBL) logic required to enable consecutive read or write operations with data being transferred on every clock cycle. This feature dramatically improves the throughput of data through the SRAM, especially in systems that require frequent write-read transitions.

All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock input is qualified by the Clock Enable ($\overline{CEN}$) signal, which when deasserted suspends operation and extends the previous clock cycle.Maximum access delay from the clock rise is 6.5 ns (133-MHz device).

Write operations are controlled by two or four Byte Write Select ($\overline{BW}_X$) and a Write Enable ($\overline{WE}$) input. All writes are conducted with on-chip synchronous self timed write circuitry.

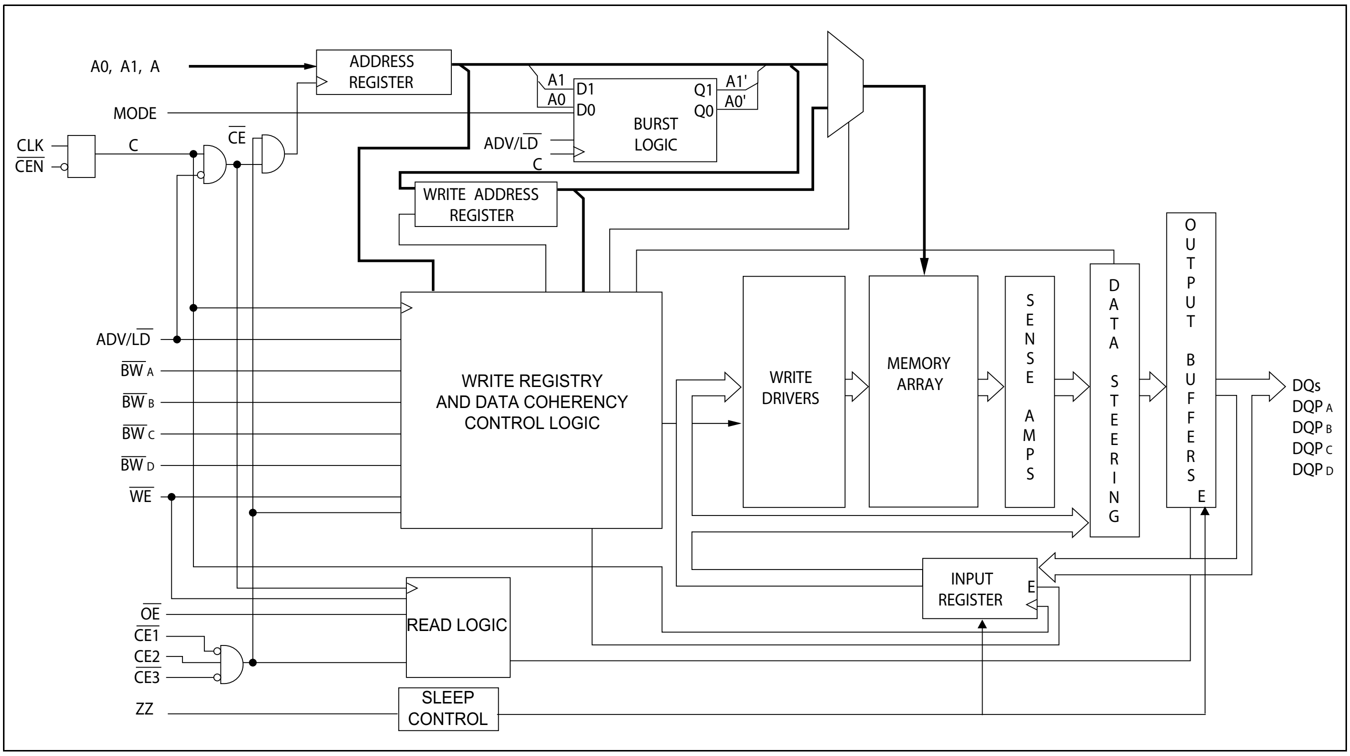
Three synchronous Chip Enables ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous Output Enable ($\overline{OE}$) provide for easy bank selection and output tri-state control. To avoid bus contention, the output drivers are synchronously tri-stated during the data portion of a write sequence.

Selection Guide

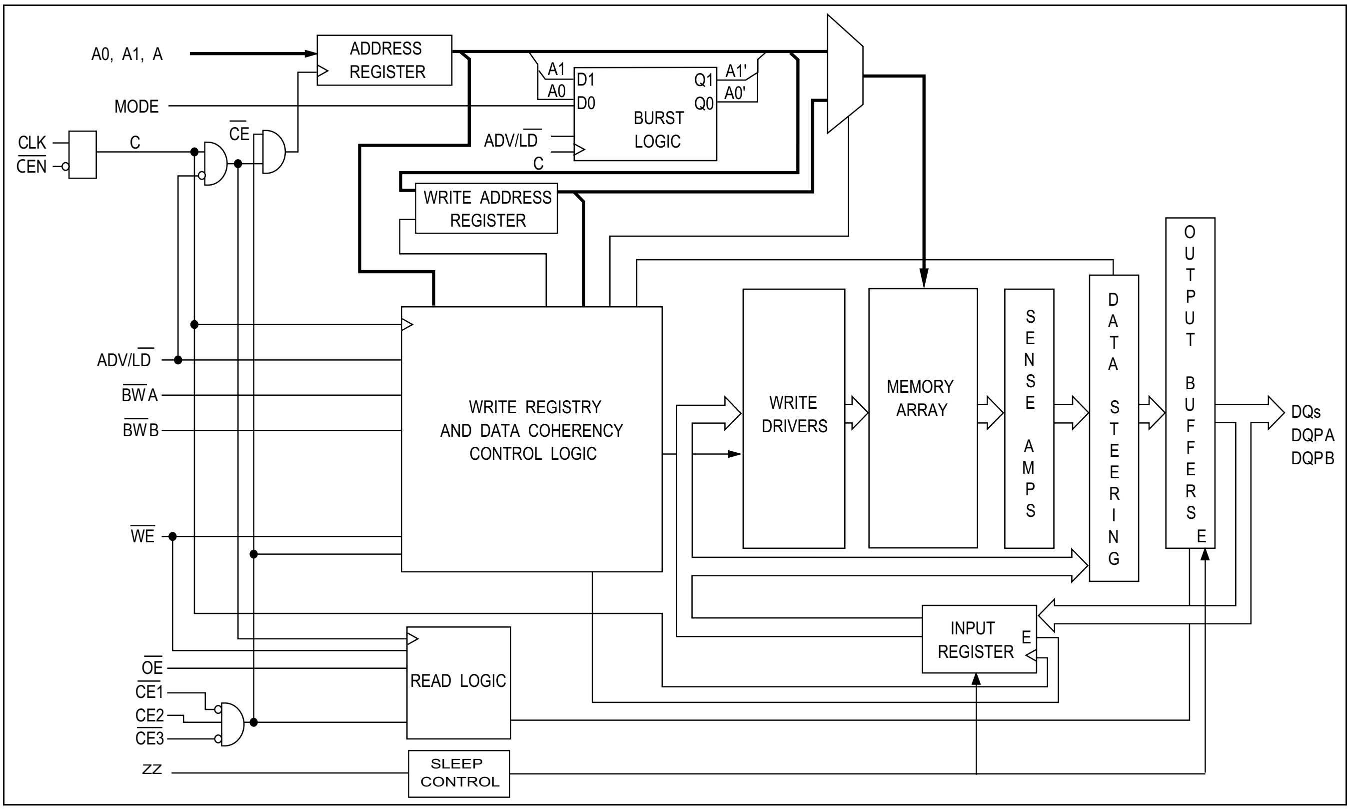
	133 MHz	117 MHz	Unit
Maximum Access Time	6.5	8.5	ns
Maximum Operating Current	305	275	mA
Maximum CMOS Standby Current	120	120	mA

Note
1. For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.

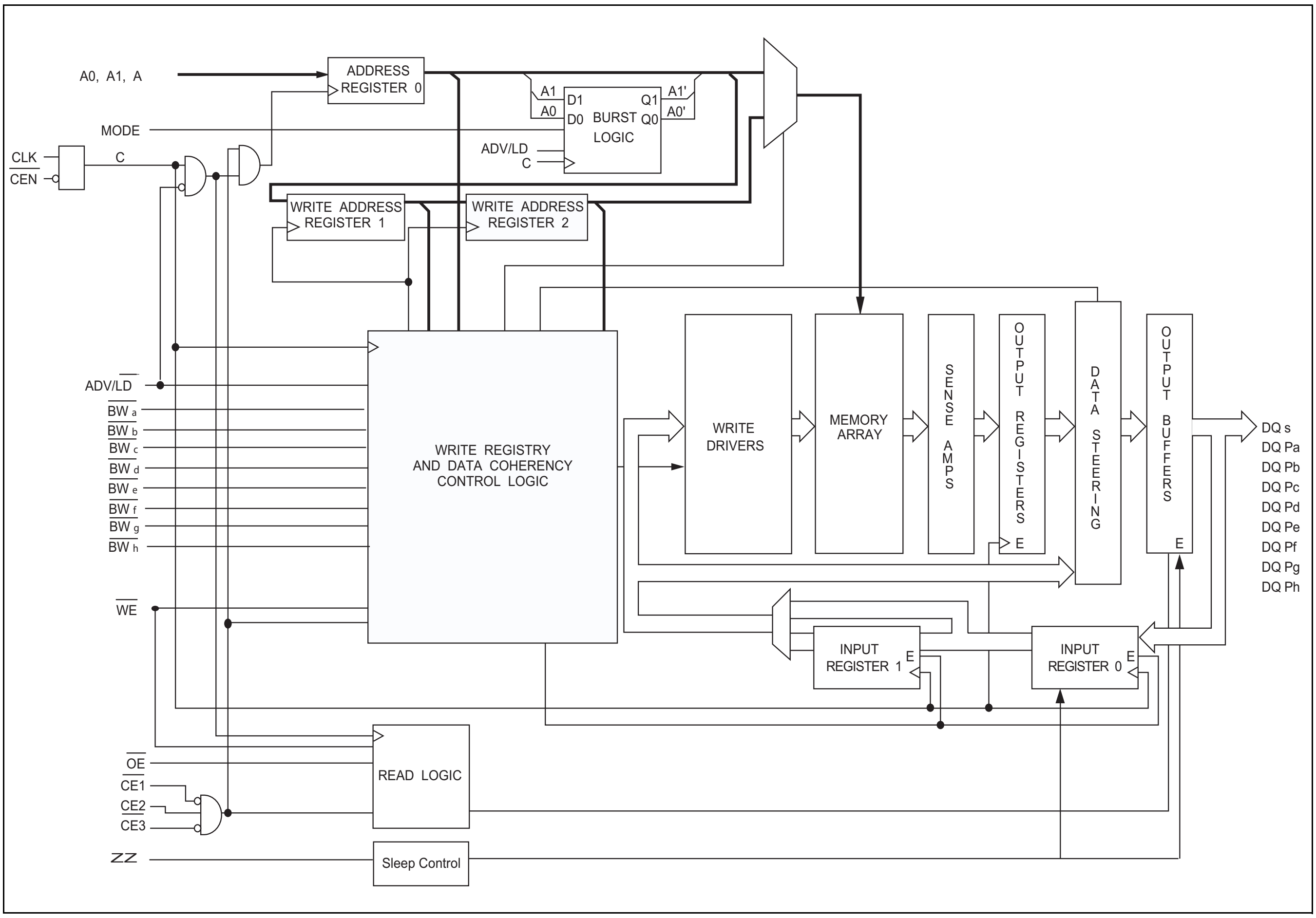
Logic Block Diagram – CY7C1471V33 (2M x 36)



Logic Block Diagram – CY7C1473V33 (4M x 18)

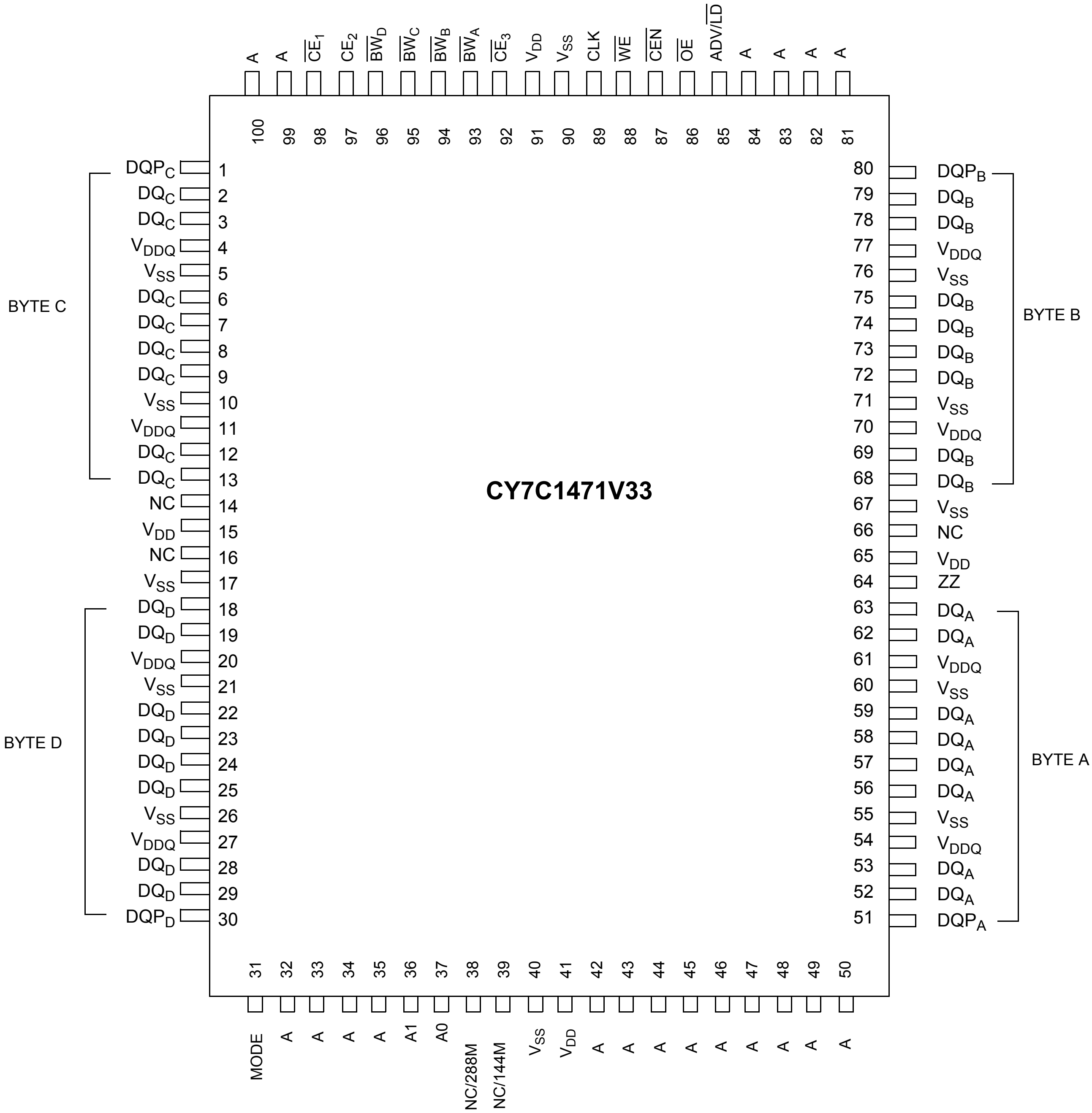


Logic Block Diagram – CY7C1475V33 (1M x 72)



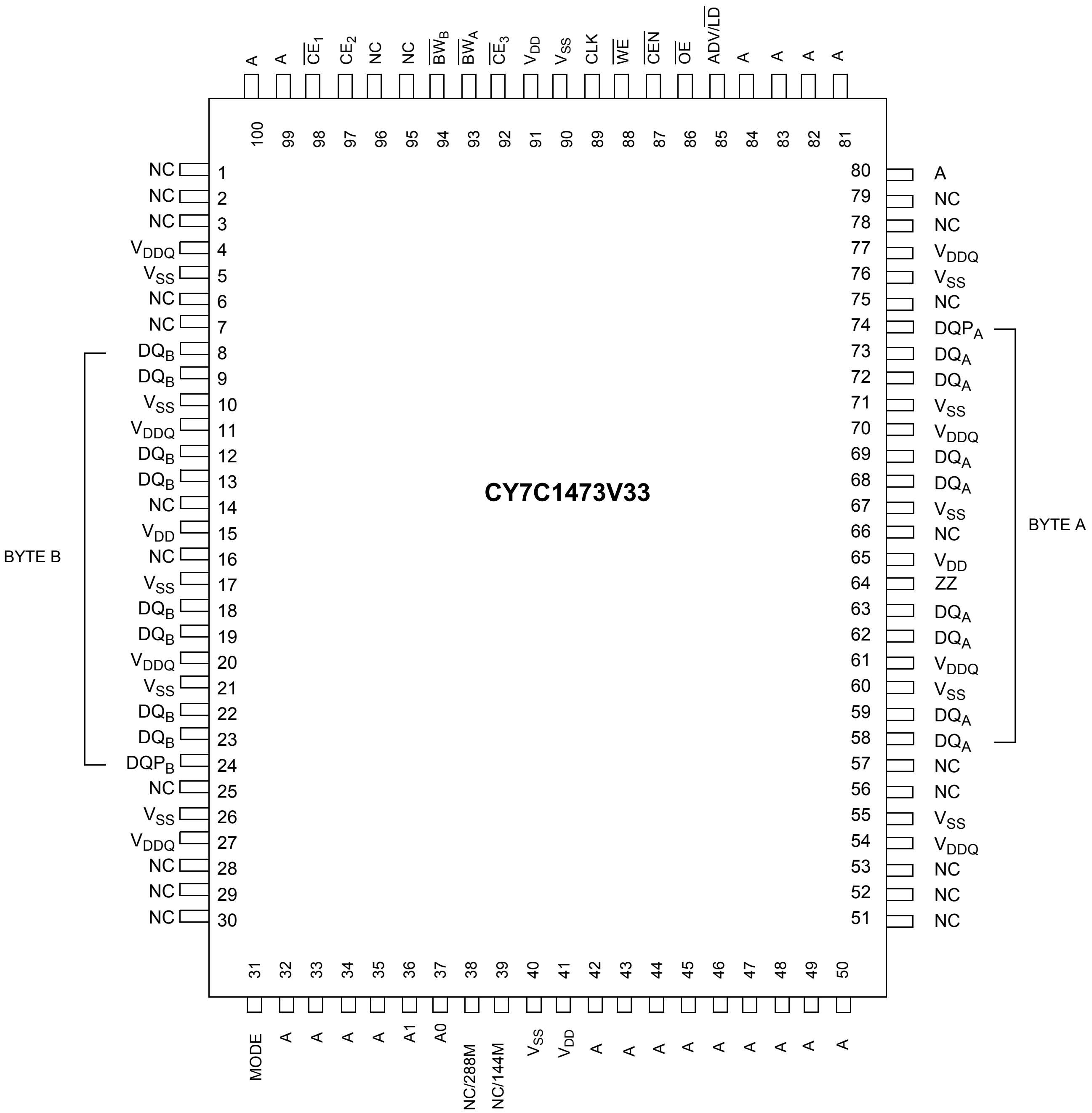
Pin Configurations

100-Pin TQFP Pinout



Pin Configurations (continued)

100-Pin TQFP Pinout



Pin Configurations (continued)

165-Ball FBGA (15 x 17 x 1.4 mm) Pinout

CY7C1471V33 (2M x 36)

	1	2	3	4	5	6	7	8	9	10	11
A	NC/576M	A	$\overline{CE}_1$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{CE}_3$	$\overline{CEN}$	ADV/$\overline{LD}$	A	A	NC
B	NC/1G	A	CE2	$\overline{BW}_D$	$\overline{BW}_A$	CLK	$\overline{WE}$	$\overline{OE}$	A	A	NC
C	DQP_C	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQP_B
D	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
E	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
F	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
G	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
K	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
L	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
M	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
N	DQP_D	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	DQP_A
P	NC/144M	A	A	A	TDI	A1	TDO	A	A	A	NC/288M
R	MODE	A	A	A	TMS	A0	TCK	A	A	A	A

CY7C1473V33 (4M x 18)

	1	2	3	4	5	6	7	8	9	10	11
A	NC/576M	A	$\overline{CE}_1$	$\overline{BW}_B$	NC	$\overline{CE}_3$	$\overline{CEN}$	ADV/$\overline{LD}$	A	A	A
B	NC/1G	A	CE2	NC	$\overline{BW}_A$	CLK	$\overline{WE}$	$\overline{OE}$	A	A	NC
C	NC	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQP_A
D	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A
E	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A
F	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A
G	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC
K	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC
L	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC
M	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC
N	DQP_B	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	NC
P	NC/144M	A	A	A	TDI	A1	TDO	A	A	A	NC/288M
R	MODE	A	A	A	TMS	A0	TCK	A	A	A	A

Pin Configurations (continued)

209-Ball FBGA (14 x 22 x 1.76 mm) Pinout

CY7C1475V33 (1M × 72)

	1	2	3	4	5	6	7	8	9	10	11
A	DQg	DQg	A	CE_2	A	ADV/$\overline{LD}$	A	$\overline{CE}_3$	A	DQb	DQb
B	DQg	DQg	$\overline{BWS}_c$	$\overline{BWS}_g$	NC	$\overline{WE}$	A	$\overline{BWS}_b$	$\overline{BWS}_f$	DQb	DQb
C	DQg	DQg	$\overline{BWS}_h$	$\overline{BWS}_d$	NC/576M	$\overline{CE}_1$	NC	$\overline{BWS}_e$	$\overline{BWS}_a$	DQb	DQb
D	DQg	DQg	V_{SS}	NC	NC/1G	$\overline{OE}$	NC	NC	V_{SS}	DQb	DQb
E	DQPg	DQPc	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	DQPf	DQPb
F	DQc	DQc	V_{SS}	V_{SS}	V_{SS}	NC	V_{SS}	V_{SS}	V_{SS}	DQf	DQf
G	DQc	DQc	V_{DDQ}	V_{DDQ}	V_{DD}	NC	V_{DD}	V_{DDQ}	V_{DDQ}	DQf	DQf
H	DQc	DQc	V_{SS}	V_{SS}	V_{SS}	NC	V_{SS}	V_{SS}	V_{SS}	DQf	DQf
J	DQc	DQc	V_{DDQ}	V_{DDQ}	V_{DD}	NC	V_{DD}	V_{DDQ}	V_{DDQ}	DQf	DQf
K	NC	NC	CLK	NC	V_{SS}	$\overline{CEN}$	V_{SS}	NC	NC	NC	NC
L	DQh	DQh	V_{DDQ}	V_{DDQ}	V_{DD}	NC	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	DQa
M	DQh	DQh	V_{SS}	V_{SS}	V_{SS}	NC	V_{SS}	V_{SS}	V_{SS}	DQa	DQa
N	DQh	DQh	V_{DDQ}	V_{DDQ}	V_{DD}	NC	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	DQa
P	DQh	DQh	V_{SS}	V_{SS}	V_{SS}	ZZ	V_{SS}	V_{SS}	V_{SS}	DQa	DQa
R	DQPd	DQPh	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	DQPa	DQPe
T	DQd	DQd	V_{SS}	NC	NC	MODE	NC	NC	V_{SS}	DQe	DQe
U	DQd	DQd	NC/144M	A	A	A	A	A	NC/288M	DQe	DQe
V	DQd	DQd	A	A	A	A1	A	A	A	DQe	DQe
W	DQd	DQd	TMS	TDI	A	A0	A	TDO	TCK	DQe	DQe

Pin Definitions

Name	IO	Description
A_0, A_1, A	Input-Synchronous	**Address Inputs used to select one of the address locations**. Sampled at the rising edge of the CLK. $A_{[1:0]}$ are fed to the two-bit burst counter.
$\overline{BW}_A$, $\overline{BW}_B$, $\overline{BW}_C$, $\overline{BW}_D$, $\overline{BW}_E$, $\overline{BW}_F$, BW_G, BW_H	Input-Synchronous	**Byte Write Inputs, Active LOW**. Qualified with $\overline{WE}$ to conduct writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{WE}$	Input-Synchronous	**Write Enable Input, Active LOW**. Sampled on the rising edge of CLK if $\overline{CEN}$ is active LOW. This signal must be asserted LOW to initiate a write sequence.
ADV/$\overline{LD}$	Input-Synchronous	**Advance/Load Input**. Advances the on-chip address counter or loads a new address. When HIGH (and $\overline{CEN}$ is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After being deselected, ADV/$\overline{LD}$ should must driven LOW to load a new address.
CLK	Input-Clock	**Clock Input**. Used to capture all synchronous inputs to the device. CLK is qualified with $\overline{CEN}$. CLK is only recognized if $\overline{CEN}$ is active LOW.
$\overline{CE}_1$	Input-Synchronous	**Chip Enable 1 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select or deselect the device.
CE_2	Input-Synchronous	**Chip Enable 2 Input, Active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select or deselect the device.
$\overline{CE}_3$	Input-Synchronous	**Chip Enable 3 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select or deselect the device.
$\overline{OE}$	Input-Asynchronous	**Output Enable, Asynchronous Input, Active LOW**. Combined with the synchronous logic block inside the device to control the direction of the IO pins. When LOW, the IO pins are enabled to behave as outputs. When deasserted HIGH, IO pins are tri-stated, and act as input data pins. $\overline{OE}$ is masked during the data portion of a write sequence, during the first clock when emerging from a deselected state, when the device is deselected.
$\overline{CEN}$	Input-Synchronous	**Clock Enable Input, Active LOW**. When asserted LOW the Clock signal is recognized by the SRAM. When deasserted HIGH the Clock signal is masked. Since deasserting $\overline{CEN}$ does not deselect the device, use $\overline{CEN}$ to extend the previous cycle when required.
ZZ	Input-Asynchronous	**ZZ "Sleep" Input**. This active HIGH input places the device in a non-time critical "sleep" condition with data integrity preserved. During normal operation, this pin must be LOW or left floating. ZZ pin has an internal pull down.
DQ_s	IO-Synchronous	**Bidirectional Data IO Lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQ_s and DQP_X are placed in a tri-state condition.The outputs are automatically tri-stated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$.
DQP_X	IO-Synchronous	**Bidirectional Data Parity IO Lines.** Functionally, these signals are identical to DQ_s. During write sequences, DQP_X is controlled by $\overline{BW}_X$ correspondingly.
MODE	Input Strap Pin	**Mode Input. Selects the burst order of the device.** When tied to Gnd selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence.
V_{DD}	Power Supply	**Power supply inputs to the core of the device**.
V_{DDQ}	IO Power Supply	**Power supply for the IO circuitry**.
V_{SS}	Ground	**Ground for the device**.

Pin Definitions (continued)

Name	IO	Description
TDO	JTAG serial output Synchronous	**Serial data-out to the JTAG circuit**. Delivers data on the negative edge of TCK. If the JTAG feature is not used, this pin must be left unconnected. This pin is not available on TQFP packages.
TDI	JTAG serial input Synchronous	**Serial data-In to the JTAG circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not used, this pin can be left floating or connected to V_{DD} through a pull up resistor. This pin is not available on TQFP packages.
TMS	JTAG serial input Synchronous	**Serial data-In to the JTAG circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not used, this pin can be disconnected or connected to V_{DD}. This pin is not available on TQFP packages.
TCK	JTAG -Clock	**Clock input to the JTAG circuitry**. If the JTAG feature is not used, this pin must be connected to V_{SS}. This pin is not available on TQFP packages.
NC	-	**No Connects**. Not internally connected to the die. 144M, 288M, 576M, and 1G are address expansion pins and are not internally connected to the die.

Functional Overview

The CY7C1471V33, CY7C1473V33, and CY7C1475V33 are synchronous flow through burst SRAMs designed specifically to eliminate wait states during write-read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the Clock Enable input signal ($\overline{CEN}$). If $\overline{CEN}$ is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with $\overline{CEN}$. Maximum access delay from the clock rise (t_{CDV}) is 6.5 ns (133-MHz device).

Accesses can be initiated by asserting all three Chip Enables ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) active at the rising edge of the clock. If ($\overline{CEN}$) is active LOW and ADV/$\overline{LD}$ is asserted LOW, the address presented to the device is latched. The access can either be a read or write operation, depending on the status of the Write Enable ($\overline{WE}$). Byte Write Select ($\overline{BW}_X$) can be used to conduct Byte Write operations.

Write operations are qualified by the Write Enable ($\overline{WE}$). All writes are simplified with on-chip synchronous self timed write circuitry.

Three synchronous Chip Enables ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous Output Enable ($\overline{OE}$) simplify depth expansion. All operations (reads, writes, and deselects) are pipelined. ADV/$\overline{LD}$ must be driven LOW after the device is deselected to load a new address for the next operation.

Single Read Accesses

A read access is initiated when these conditions are satisfied at clock rise:

- $\overline{CEN}$ is asserted LOW
- $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are ALL asserted active
- $\overline{WE}$ is deasserted HIGH
- ADV/$\overline{LD}$ is asserted LOW.

The address presented to the address inputs is latched into the Address Register and presented to the memory array and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the output buffers. The data is available within 6.5 ns (133-MHz device) provided $\overline{OE}$ is active LOW. After the first clock of the read access, the output buffers are controlled by $\overline{OE}$ and the internal control logic. $\overline{OE}$ must be driven LOW to drive out the requested data. On the subsequent clock, another operation (read/write/deselect) can be initiated. When the SRAM is deselected at clock rise by one of the chip enable signals, output is be tri-stated immediately.

Burst Read Accesses

The CY7C1471V33, CY7C1473V33 and CY7C1475V33 have an on-chip burst counter that enables the user to supply a single address and conduct up to four reads without reasserting the address inputs. ADV/$\overline{LD}$ must be driven LOW to load a new address into the SRAM, as described in the Single Read Access section. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence, and wraps around when incremented sufficiently. A HIGH input on ADV/$\overline{LD}$ increments the internal burst counter regardless of the state of chip enable inputs or $\overline{WE}$. $\overline{WE}$ is latched at the beginning of a burst cycle. Therefore, the type of access (read or write) is maintained throughout the burst sequence.

Single Write Accesses

Write accesses are initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are ALL asserted active, and (3) $\overline{WE}$ is asserted LOW. The address presented to the address bus is loaded into the Address Register. The Write signals are latched into the Control Logic block. The data lines are automatically tri-stated regardless of the state of the $\overline{OE}$ input signal. This allows the external logic to present the data on DQs and DQP_X.

On the next clock rise the data presented to DQs and DQP_X (or a subset for Byte Write operations, see "Truth Table for Read/Write" on page 12 for details) inputs is latched into the device and the write is complete. Additional accesses (read/write/deselect) can be initiated on this cycle.

The data written during the write operation is controlled by BW_X signals. The CY7C1471V33, CY7C1473V33, and CY7C1475V33 provides Byte Write capability that is described in the "Truth Table for Read/Write" on page 12. The input WE with the selected BW_X input selectively writes to only the desired bytes. Bytes not selected during a Byte Write operation remain unaltered. A synchronous self timed write mechanism has been provided to simplify the write operations. Byte write capability is included to greatly simplify read/modify/write sequences, which can be reduced to simple byte write operations.

Because the CY7C1471V33, CY7C1473V33, and CY7C1475V33 are common IO devices, data must not be driven into the device while the outputs are active. The Output Enable (OE) can be deasserted HIGH before presenting data to the DQs and DQP_X inputs. Doing so tri-states the output drivers. As a safety precaution, DQs and DQP_X are automatically tri-stated during the data portion of a write cycle, regardless of the state of OE.

Burst Write Accesses

The CY7C1471V33, CY7C1473V33, and CY7C1475V33 have an on-chip burst counter that enables the user to supply a single address and conduct up to four write operations without reasserting the address inputs. ADV/LD must be driven LOW to load the initial address, as described in the Single Write Access section. When ADV/LD is driven HIGH on the subsequent clock rise, the Chip Enables (CE_1, CE_2, and CE_3) and WE inputs are ignored and the burst counter is incremented. The correct BW_X inputs must be driven in each cycle of the burst write to write the correct bytes of data.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation "sleep" mode. Two clock cycles are required to enter into or exit from this "sleep" mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the "sleep" mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected before entering the "sleep" mode. CE_1, CE_2, and CE_3, must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Address Table (MODE = Floating or V_{DD})

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table (MODE = GND)

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	$ZZ \geq V_{DD} - 0.2V$		120	mA
t_{ZZS}	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2V$		$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	$ZZ \leq 0.2V$	$2t_{CYC}$		ns
t_{ZZI}	ZZ active to sleep current	This parameter is sampled		$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit sleep current	This parameter is sampled	0		ns

Truth Table

The truth table for CY7C1471V33, CY7C1473V33, CY7C1475V33 follows.[2, 3, 4, 5, 6, 7, 8]

Operation	Address Used	$\overline{CE_1}$	CE_2	$\overline{CE_3}$	ZZ	ADV/$\overline{LD}$	$\overline{WE}$	$\overline{BW_X}$	$\overline{OE}$	$\overline{CEN}$	CLK	DQ
Deselect Cycle	None	H	X	X	L	L	X	X	X	L	L->H	Tri-State
Deselect Cycle	None	X	X	H	L	L	X	X	X	L	L->H	Tri-State
Deselect Cycle	None	X	L	X	L	L	X	X	X	L	L->H	Tri-State
Continue Deselect Cycle	None	X	X	X	L	H	X	X	X	L	L->H	Tri-State
Read Cycle (Begin Burst)	External	L	H	L	L	L	H	X	L	L	L->H	Data Out (Q)
Read Cycle (Continue Burst)	Next	X	X	X	L	H	X	X	L	L	L->H	Data Out (Q)
NOP/Dummy Read (Begin Burst)	External	L	H	L	L	L	H	X	H	L	L->H	Tri-State
Dummy Read (Continue Burst)	Next	X	X	X	L	H	X	X	H	L	L->H	Tri-State
Write Cycle (Begin Burst)	External	L	H	L	L	L	L	L	X	L	L->H	Data In (D)
Write Cycle (Continue Burst)	Next	X	X	X	L	H	X	L	X	L	L->H	Data In (D)
NOP/Write Abort (Begin Burst)	None	L	H	L	L	L	L	H	X	L	L->H	Tri-State
Write Abort (Continue Burst)	Next	X	X	X	L	H	X	H	X	L	L->H	Tri-State
Ignore Clock Edge (Stall)	Current	X	X	X	L	X	X	X	X	H	L->H	-
Sleep Mode	None	X	X	X	H	X	X	X	X	X	X	Tri-State

Notes
2. X = "Don't Care." H = Logic HIGH, L = Logic LOW. $\overline{BW_X}$ = L signifies at least one Byte Write Select is active, $\overline{BW_X}$ = Valid signifies that the desired Byte Write Selects are asserted, see "Truth Table for Read/Write" on page 12 for details.
3. Write is defined by $\overline{BW_X}$, and $\overline{WE}$. See "Truth Table for Read/Write" on page 12.
4. When a Write cycle is detected, all IOs are tri-stated, even during Byte Writes.
5. The DQs and DQP_X pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
6. $\overline{CEN}$ = H, inserts wait states.
7. Device powers up deselected with the IOs in a tri-state condition, regardless of $\overline{OE}$.
8. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle DQs and DQP_X = tri-state when $\overline{OE}$ is inactive or when the device is deselected, and DQs and DQP_X = data when $\overline{OE}$ is active.

Truth Table for Read/Write

The read-write truth table for CY7C1471V33 follows.[2, 3, 9]

Function	$\overline{WE}$	$\overline{BW}_A$	$\overline{BW}_B$	$\overline{BW}_C$	$\overline{BW}_D$
Read	H	X	X	X	X
Write No bytes written	L	H	H	H	H
Write Byte A – (DQ_A and DQP_A)	L	L	H	H	H
Write Byte B – (DQ_B and DQP_B)	L	H	L	H	H
Write Byte C – (DQ_C and DQP_C)	L	H	H	L	H
Write Byte D – (DQ_D and DQP_D)	L	H	H	H	L
Write All Bytes	L	L	L	L	L

Truth Table for Read/Write

The read-write truth table for CY7C1473V33 follows.[2, 3, 9]

Function	$\overline{WE}$	$\overline{BW}_b$	$\overline{BW}_a$
Read	H	X	X
Write – No Bytes Written	L	H	H
Write Byte a – (DQ_a and DQP_a)	L	H	L
Write Byte b – (DQ_b and DQP_b)	L	L	H
Write Both Bytes	L	L	L

Truth Table for Read/Write

The read-write truth table for CY7C1475V33 follows.[2, 3, 9]

Function	$\overline{WE}$	$\overline{BW}_x$
Read	H	X
Write – No Bytes Written	L	H
Write Byte X – (DQ_x and DQP_x)	L	L
Write All Bytes	L	All $\overline{BW}$ = L

Note
9. Table only lists a partial listing of the byte write combinations. Any combination of $\overline{BW}_X$ is valid. Appropriate write is based on which byte write is active.

IEEE 1149.1 Serial Boundary Scan (JTAG)

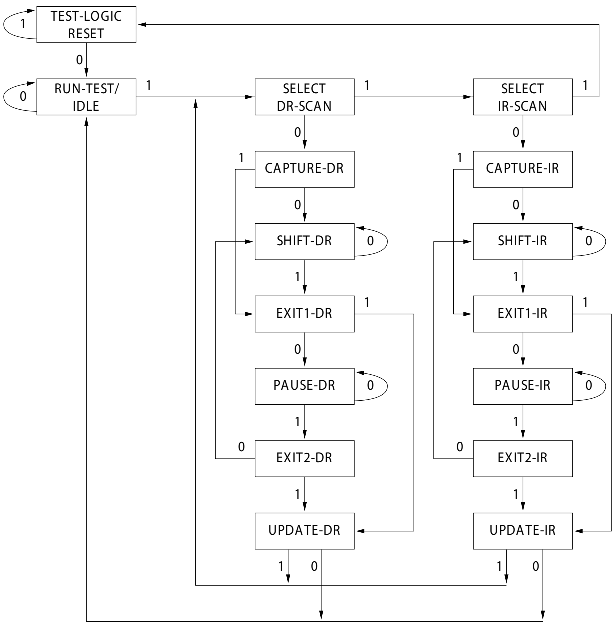
The CY7C1471V33, CY7C1473V33, and CY7C1475V33 incorporate a serial boundary scan test access port (TAP). This port operates in accordance with IEEE Standard 1149.1-1990 but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC-standard 3.3V or 2.5V IO logic levels.

The CY7C1471V33, CY7C1473V33, and CY7C1475V33 contain a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull up resistor. TDO must be left unconnected. During power up, the device comes up in a reset state, which does not interfere with the operation of the device.

TAP Controller State Diagram



The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

Test Access Port (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test MODE SELECT (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

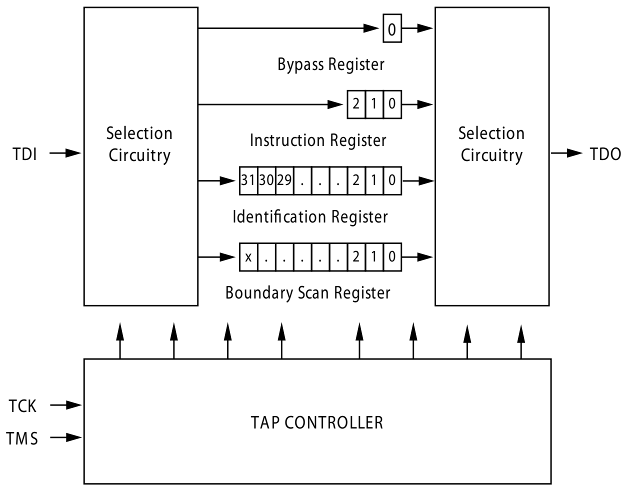
Test Data-In (TDI)

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information about loading the instruction register, see the TAP Controller State Diagram. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register. (See TAP Controller Block Diagram.)

Test Data-Out (TDO)

The TDO output ball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. (See TAP Controller State Diagram.)

TAP Controller Block Diagram



Performing a TAP Reset

A RESET is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

During power up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

TAP Registers

Registers are connected between the TDI and TDO balls and enable data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

nstruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in the “TAP Controller Block Diagram” on page 13. During power up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary ‘01’ pattern to enable fault isolation of the board-level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM.

The boundary scan register is loaded with the contents of the RAM IO ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the IO ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in “Identification Register Definitions” on page 18.

TAP Instruction Set

Overview

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in “Identification Codes” on page 18. Three of these instructions are listed as RESERVED and must not be used. The other five instructions are described in detail below.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented.

The TAP controller cannot be used to load address data or control signals into the SRAM and cannot preload the IO buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather, it performs a capture of the IO ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction after it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in this SRAM TAP controller, and therefore this device is not compliant to 1149.1. The TAP controller does recognize an all-0 instruction.

When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between the two instructions. Unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High-Z state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and enables the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register during power up or whenever the TAP controller is in a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO balls when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the device TAP controller is not fully 1149.1 compliant.

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and bidirectional balls is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output may undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that is captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time (t_{CS} plus t_{CH}).

The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CLK captured in the boundary scan register.

After the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO balls.

Note that since the PRELOAD part of the command is not implemented, putting the TAP to the Update-DR state while performing a SAMPLE/PRELOAD instruction has the same effect as the Pause-DR command.

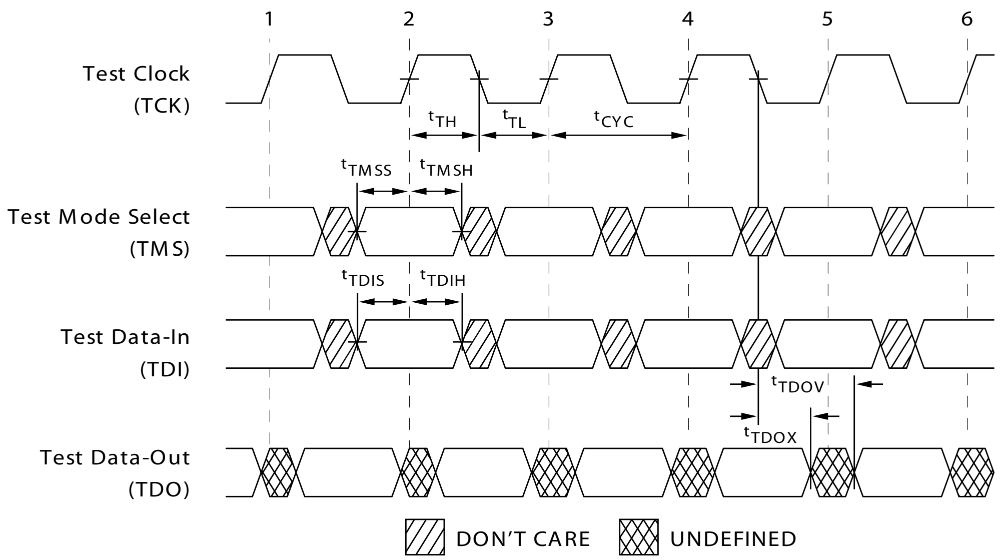
BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO balls. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Timing



TAP AC Switching Characteristics

Over the Operating Range[10, 11]

Parameter	Description	Min	Max	Unit
Clock				
t_{TCYC}	TCK Clock Cycle Time	50		ns
t_{TF}	TCK Clock Frequency		20	MHz
t_{TH}	TCK Clock HIGH time	20		ns
t_{TL}	TCK Clock LOW time	20		ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO Valid		5	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0		ns
Setup Times				
t_{TMSS}	TMS Setup to TCK Clock Rise	5		ns
t_{TDIS}	TDI Setup to TCK Clock Rise	5		ns
t_{CS}	Capture Setup to TCK Rise	5		ns
Hold Times				
t_{TMSH}	TMS Hold after TCK Clock Rise	5		ns
t_{TDIH}	TDI Hold after Clock Rise	5		ns
t_{CH}	Capture Hold after Clock Rise	5		ns

Notes

10. t_{CS} and t_{CH} refer to the setup and hold time requirements of latching data from the boundary scan register.
11. Test conditions are specified using the load in TAP AC Test Conditions. t_R/t_F = 1 ns.

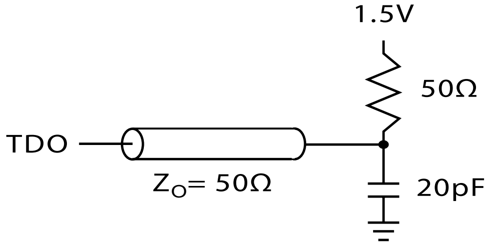
3.3V TAP AC Test Conditions

Input pulse levels .... V_{SS} to 3.3V
Input rise and fall times .... 1 ns
Input timing reference levels 1.5V
Output reference levels..1.5V
Test load termination supply voltage 1.5V

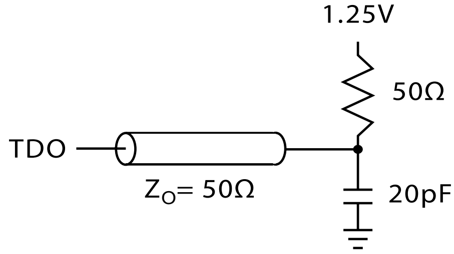
2.5V TAP AC Test Conditions

Input pulse levels...V_{SS} to 2.5V
Input rise and fall time ....1 ns
Input timing reference levels.. 1.25V
Output reference levels 1.25V
Test load termination supply voltage 1.25V

3.3V TAP AC Output Load Equivalent



2.5V TAP AC Output Load Equivalent



TAP DC Electrical Characteristics And Operating Conditions

(0°C < T_A < +70°C; V_{DD} = 3.3V ±0.165V unless otherwise noted)[12]

Parameter	Description	Test Conditions		Min	Max	Unit
V_{OH1}	Output HIGH Voltage	I_{OH} = –4.0 mA, V_{DDQ} = 3.3V		2.4		V
		I_{OH} = –1.0 mA, V_{DDQ} = 2.5V		2.0		V
V_{OH2}	Output HIGH Voltage	I_{OH} = –100 µA	V_{DDQ} = 3.3V	2.9		V
			V_{DDQ} = 2.5V	2.1		V
V_{OL1}	Output LOW Voltage	I_{OL} = 8.0 mA	V_{DDQ} = 3.3V		0.4	V
		I_{OL} = 1.0 mA	V_{DDQ} = 2.5V		0.4	V
V_{OL2}	Output LOW Voltage	I_{OL} = 100 µA	V_{DDQ} = 3.3V		0.2	V
			V_{DDQ} = 2.5V		0.2	V
V_{IH}	Input HIGH Voltage		V_{DDQ} = 3.3V	2.0	V_{DD} + 0.3	V
			V_{DDQ} = 2.5V	1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		V_{DDQ} = 3.3V	–0.3	0.8	V
			V_{DDQ} = 2.5V	–0.3	0.7	V
I_X	Input Load Current	GND ≤ V_{IN} ≤ V_{DDQ}		–5	5	µA

Note
12. All voltages refer to V_{SS} (GND).

Identification Register Definitions

Instruction Field	CY7C1471V33 (2Mx36)	CY7C1473V33 (4Mx18)	CY7C1475V33 (1Mx72)	Description
Revision Number (31:29)	000	000	000	Describes the version number
Device Depth (28:24)[13]	01011	01011	01011	Reserved for internal use
Architecture/Memory Type(23:18)	001001	001001	001001	Defines memory type and architecture
Bus Width/Density(17:12)	100100	010100	110100	Defines width and density
Cypress JEDEC ID Code (11:1)	00000110100	00000110100	00000110100	Enables unique identification of SRAM vendor
ID Register Presence Indicator (0)	1	1	1	Indicates the presence of an ID register

Scan Register Sizes

Register Name	Bit Size (x36)	Bit Size (x18)	Bit Size (x72)
Instruction	3	3	3
Bypass	1	1	1
ID	32	32	32
Boundary Scan Order – 165FBGA	71	52	-
Boundary Scan Order – 209BGA	-	-	110

Identification Codes

Instruction	Code	Description
EXTEST	000	Captures IO ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM outputs to High-Z state. This instruction is not 1149.1-compliant.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures IO ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures IO ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation. This instruction does not implement 1149.1 preload function and is therefore not 1149.1 compliant.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

Note

13. Bit #24 is “1” in the ID Register Definitions for both 2.5V and 3.3V versions of this device.

Boundary Scan Exit Order (2M x 36)

Bit #	165-Ball ID	Bit #	165-Ball ID	Bit #	165-Ball ID	Bit #	165-Ball ID
1	C1	21	R3	41	J11	61	B7
2	D1	22	P2	42	K10	62	B6
3	E1	23	R4	43	J10	63	A6
4	D2	24	P6	44	H11	64	B5
5	E2	25	R6	45	G11	65	A5
6	F1	26	R8	46	F11	66	A4
7	G1	27	P3	47	E11	67	B4
8	F2	28	P4	48	D10	68	B3
9	G2	29	P8	49	D11	69	A3
10	J1	30	P9	50	C11	70	A2
11	K1	31	P10	51	G10	71	B2
12	L1	32	R9	52	F10		
13	J2	33	R10	53	E10		
14	M1	34	R11	54	A9		
15	N1	35	N11	55	B9		
16	K2	36	M11	56	A10		
17	L2	37	L11	57	B10		
18	M2	38	M10	58	A8		
19	R1	39	L10	59	B8		
20	R2	40	K11	60	A7		

Boundary Scan Exit Order (4M x 18)

Bit #	165-Ball ID	Bit #	165-Ball ID	Bit #	165-Ball ID	Bit #	165-Ball ID
1	D2	14	R4	27	L10	40	B10
2	E2	15	P6	28	K10	41	A8
3	F2	16	R6	29	J10	42	B8
4	G2	17	R8	30	H11	43	A7
5	J1	18	P3	31	G11	44	B7
6	K1	19	P4	32	F11	45	B6
7	L1	20	P8	33	E11	46	A6
8	M1	21	P9	34	D11	47	B5
9	N1	22	P10	35	C11	48	A4
10	R1	23	R9	36	A11	49	B3
11	R2	24	R10	37	A9	50	A3
12	R3	25	R11	38	B9	51	A2
13	P2	26	M10	39	A10	52	B2

Boundary Scan Exit Order (1M x 72)

Bit #	209-Ball ID	Bit #	209-Ball ID	Bit #	209-Ball ID	Bit #	209-Ball ID
1	A1	29	T1	57	U10	85	B11
2	A2	30	T2	58	T11	86	B10
3	B1	31	U1	59	T10	87	A11
4	B2	32	U2	60	R11	88	A10
5	C1	33	V1	61	R10	89	A7
6	C2	34	V2	62	P11	90	A5
7	D1	35	W1	63	P10	91	A9
8	D2	36	W2	64	N11	92	U8
9	E1	37	T6	65	N10	93	A6
10	E2	38	V3	66	M11	94	D6
11	F1	39	V4	67	M10	95	K6
12	F2	40	U4	68	L11	96	B6
13	G1	41	W5	69	L10	97	K3
14	G2	42	V6	70	P6	98	A8
15	H1	43	W6	71	J11	99	B4
16	H2	44	V5	72	J10	100	B3
17	J1	45	U5	73	H11	101	C3
18	J2	46	U6	74	H10	102	C4
19	L1	47	W7	75	G11	103	C8
20	L2	48	V7	76	G10	104	C9
21	M1	49	U7	77	F11	105	B9
22	M2	50	V8	78	F10	106	B8
23	N1	51	V9	79	E10	107	A4
24	N2	52	W11	80	E11	108	C6
25	P1	53	W10	81	D11	109	B7
26	P2	54	V11	82	D10	110	A3
27	R2	55	V10	83	C11		
28	R1	56	U11	84	C10		

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ....–65°C to +150°C

Ambient Temperature with
Power Applied..–55°C to +125°C

Supply Voltage on V_{DD} Relative to GND........ –0.5V to +4.6V

Supply Voltage on V_{DDQ} Relative to GND ...... –0.5V to $+V_{DD}$

DC Voltage Applied to Outputs
in Tri-State.. –0.5V to V_{DDQ} + 0.5V

DC Input Voltage ....–0.5V to V_{DD} + 0.5V

Current into Outputs (LOW)... 20 mA

Static Discharge Voltage.. >2001V
(MIL-STD-883, Method 3015)

Latch Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	3.3V –5%/+10%	2.5V – 5% to V_{DD}
Industrial	–40°C to +85°C		

Electrical Characteristics

Over the Operating Range[14, 15]

Parameter	Description	Test Conditions		Min	Max	Unit
V_{DD}	Power Supply Voltage			3.135	3.6	V
V_{DDQ}	IO Supply Voltage	For 3.3V IO		3.135	V_{DD}	V
		For 2.5V IO		2.375	2.625	V
V_{OH}	Output HIGH Voltage	For 3.3V IO, I_{OH} = –4.0 mA		2.4		V
		For 2.5V IO, I_{OH} = –1.0 mA		2.0		V
V_{OL}	Output LOW Voltage	For 3.3V IO, I_{OL} = 8.0 mA			0.4	V
		For 2.5V IO, I_{OL} = 1.0 mA			0.4	V
V_{IH}	Input HIGH Voltage[14]	For 3.3V IO		2.0	V_{DD} + 0.3V	V
		For 2.5V IO		1.7	V_{DD} + 0.3V	V
V_{IL}	Input LOW Voltage[14]	For 3.3V IO		–0.3	0.8	V
		For 2.5V IO		–0.3	0.7	V
I_X	Input Leakage Current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input Current of MODE	Input = V_{SS}		–30		µA
		Input = V_{DD}			5	µA
	Input Current of ZZ	Input = V_{SS}		–5		µA
		Input = V_{DD}			30	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ $V_{DD,}$ Output Disabled		–5	5	µA
I_{DD}	V_{DD} Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$	7.5 ns cycle, 133 MHz		305	mA
			10 ns cycle, 117 MHz		275	mA
I_{SB1}	Automatic CE Power Down Current—TTL Inputs	V_{DD} = Max, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL} f = f_{MAX}, inputs switching	7.5 ns cycle, 133 MHz		200	mA
			10 ns cycle, 117 MHz		200	mA
I_{SB2}	Automatic CE Power Down Current—CMOS Inputs	V_{DD} = Max, Device Deselected, V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DD} – 0.3V, f = 0, inputs static	All speeds		120	mA
I_{SB3}	Automatic CE Power Down Current—CMOS Inputs	V_{DD} = Max, Device Deselected, or V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} – 0.3V f = f_{MAX}, inputs switching	7.5 ns cycle, 133 MHz		200	mA
			10 ns cycle, 117 MHz		200	mA
I_{SB4}	Automatic CE Power Down Current—TTL Inputs	V_{DD} = Max, Device Deselected, V_{IN} ≥ V_{DD} – 0.3V or V_{IN} ≤ 0.3V, f = 0, inputs static	All Speeds		165	mA

Notes
14. Overshoot: V_{IH}(AC) < V_{DD} +1.5V (pulse width less than t_{CYC}/2). Undershoot: V_{IL}(AC) > –2V (pulse width less than t_{CYC}/2).
15. $T_{Power-up}$: assumes a linear ramp from 0V to V_{DD}(min.) within 200 ms. During this time V_{IH} < V_{DD} and V_{DDQ} ≤ V_{DD}.

Capacitance

Tested initially and after any design or process change that may affect these parameters.

Parameter	Description	Test Conditions	100 TQFP Package	165 FBGA Package	209 BGA Package	Unit
$C_{ADDRESS}$	Address Input Capacitance	$T_A = 25°C$, f = 1 MHz, $V_{DD} = 3.3V$ $V_{DDQ} = 2.5V$	6	6	6	pF
C_{DATA}	Data Input Capacitance		5	5	5	pF
C_{CTRL}	Control Input Capacitance		8	8	8	pF
C_{CLK}	Clock Input Capacitance		6	6	6	pF
C_{IO}	Input/Output Capacitance		5	5	5	pF

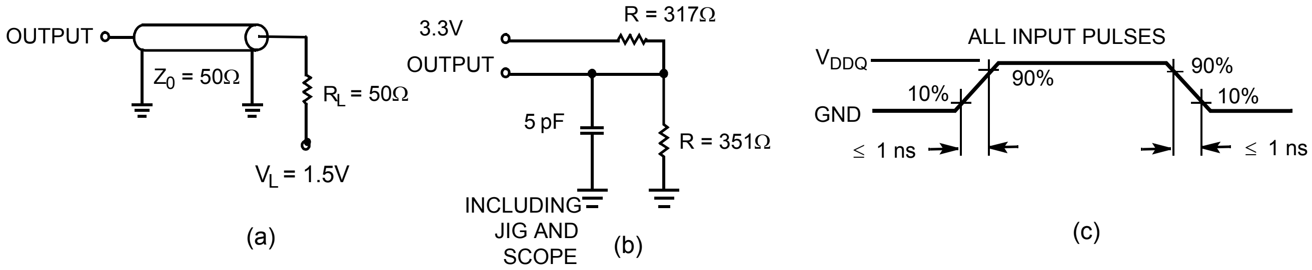
Thermal Resistance

Tested initially and after any design or process change that may affect these parameters.

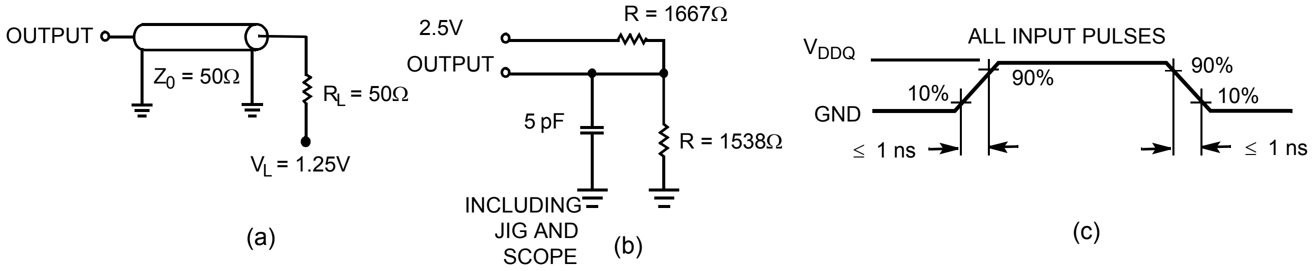
Parameter	Description	Test Conditions	100 TQFP Max	165 FBGA Max	209 FBGA Max	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, according to EIA/JESD51.	24.63	16.3	15.2	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		2.28	2.1	1.7	°C/W

AC Test Loads and Waveforms

3.3V IO Test Load



2.5V IO Test Load



Switching Characteristics

Over the Operating Range. Unless otherwise noted in the following table, timing reference level is 1.5V when V_{DDQ} = 3.3V and is 1.25V when V_{DDQ} = 2.5V. Test conditions shown in (a) of "AC Test Loads and Waveforms" on page 22 unless otherwise noted.

Parameter	Description	133 MHz		117 MHz		Unit
		Min	Max	Min	Max	
t_{POWER} [16]		1		1		ms
Clock						
t_{CYC}	Clock Cycle Time	7.5		10		ns
t_{CH}	Clock HIGH	2.5		3.0		ns
t_{CL}	Clock LOW	2.5		3.0		ns
Output Times						
t_{CDV}	Data Output Valid After CLK Rise		6.5		8.5	ns
t_{DOH}	Data Output Hold After CLK Rise	2.5		2.5		ns
t_{CLZ}	Clock to Low-Z [17, 18, 19]	3.0		3.0		ns
t_{CHZ}	Clock to High-Z [17, 18, 19]		3.8		4.5	ns
t_{OEV}	$\overline{OE}$ LOW to Output Valid		3.0		3.8	ns
t_{OELZ}	$\overline{OE}$ LOW to Output Low-Z [17, 18, 19]	0		0		ns
t_{OEHZ}	$\overline{OE}$ HIGH to Output High-Z [17, 18, 19]		3.0		4.0	ns
Setup Times						
t_{AS}	Address Setup Before CLK Rise	1.5		1.5		ns
t_{ALS}	ADV/$\overline{LD}$ Setup Before CLK Rise	1.5		1.5		ns
t_{WES}	$\overline{WE}$, $\overline{BW}_X$ Setup Before CLK Rise	1.5		1.5		ns
t_{CENS}	$\overline{CEN}$ Setup Before CLK Rise	1.5		1.5		ns
t_{DS}	Data Input Setup Before CLK Rise	1.5		1.5		ns
t_{CES}	Chip Enable Setup Before CLK Rise	1.5		1.5		ns
Hold Times						
t_{AH}	Address Hold After CLK Rise	0.5		0.5		ns
t_{ALH}	ADV/$\overline{LD}$ Hold After CLK Rise	0.5		0.5		ns
t_{WEH}	$\overline{WE}$, $\overline{BW}_X$ Hold After CLK Rise	0.5		0.5		ns
t_{CENH}	$\overline{CEN}$ Hold After CLK Rise	0.5		0.5		ns
t_{DH}	Data Input Hold After CLK Rise	0.5		0.5		ns
t_{CEH}	Chip Enable Hold After CLK Rise	0.5		0.5		ns

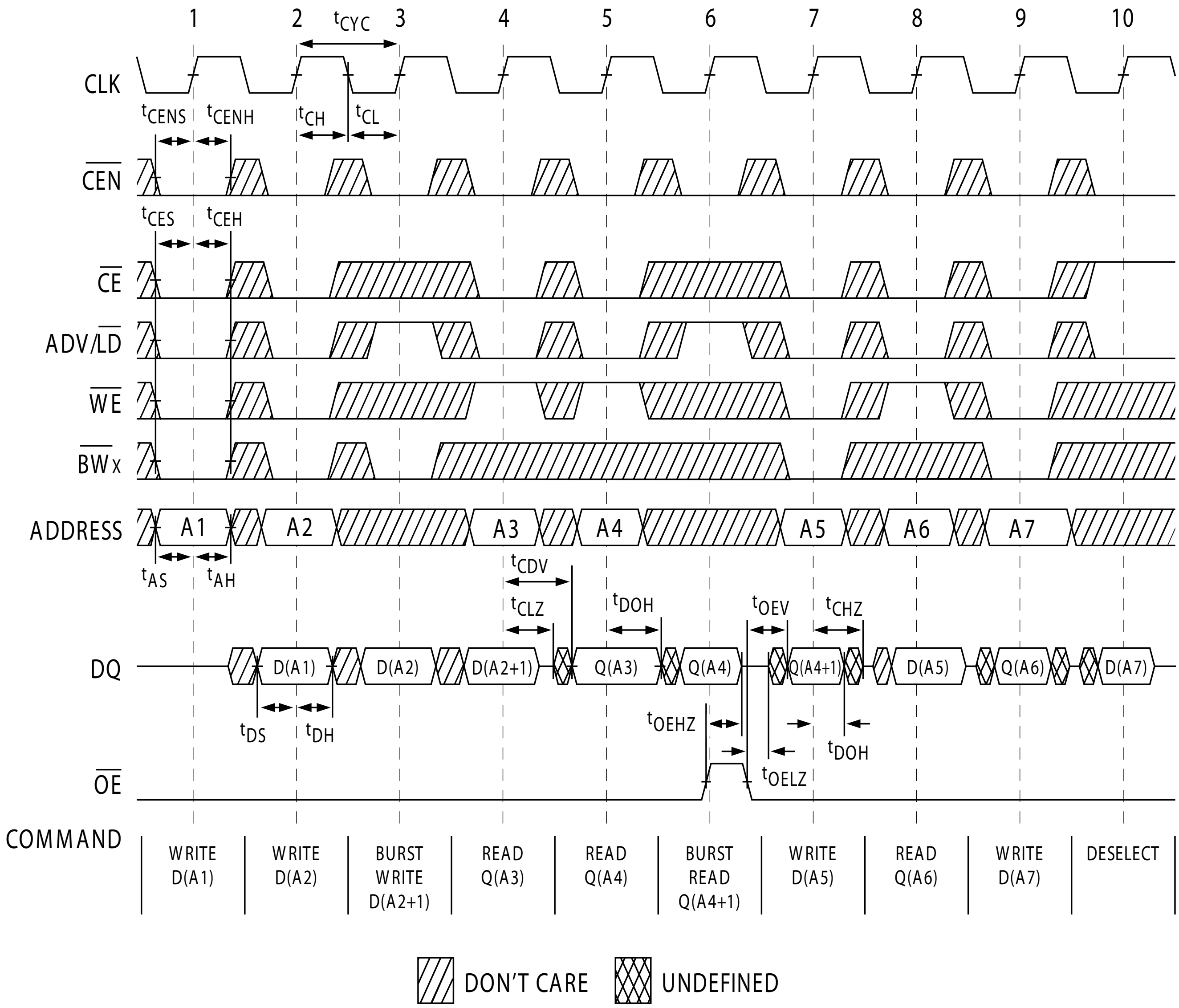
Notes

16. This part has an internal voltage regulator; t_{POWER} is the time that the power needs to be supplied above V_{DD}(minimum) initially, before a read or write operation can be initiated.
17. t_{CHZ}, t_{CLZ}, t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of "AC Test Loads and Waveforms" on page 22. Transition is measured ±200 mV from steady-state voltage.
18. At any supplied voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z before Low-Z under the same system conditions.
19. This parameter is sampled and not 100% tested.

Switching Waveforms

Figure 1 shows read-write timing waveform.[20, 21, 22]

Figure 1. Read/Write Timing

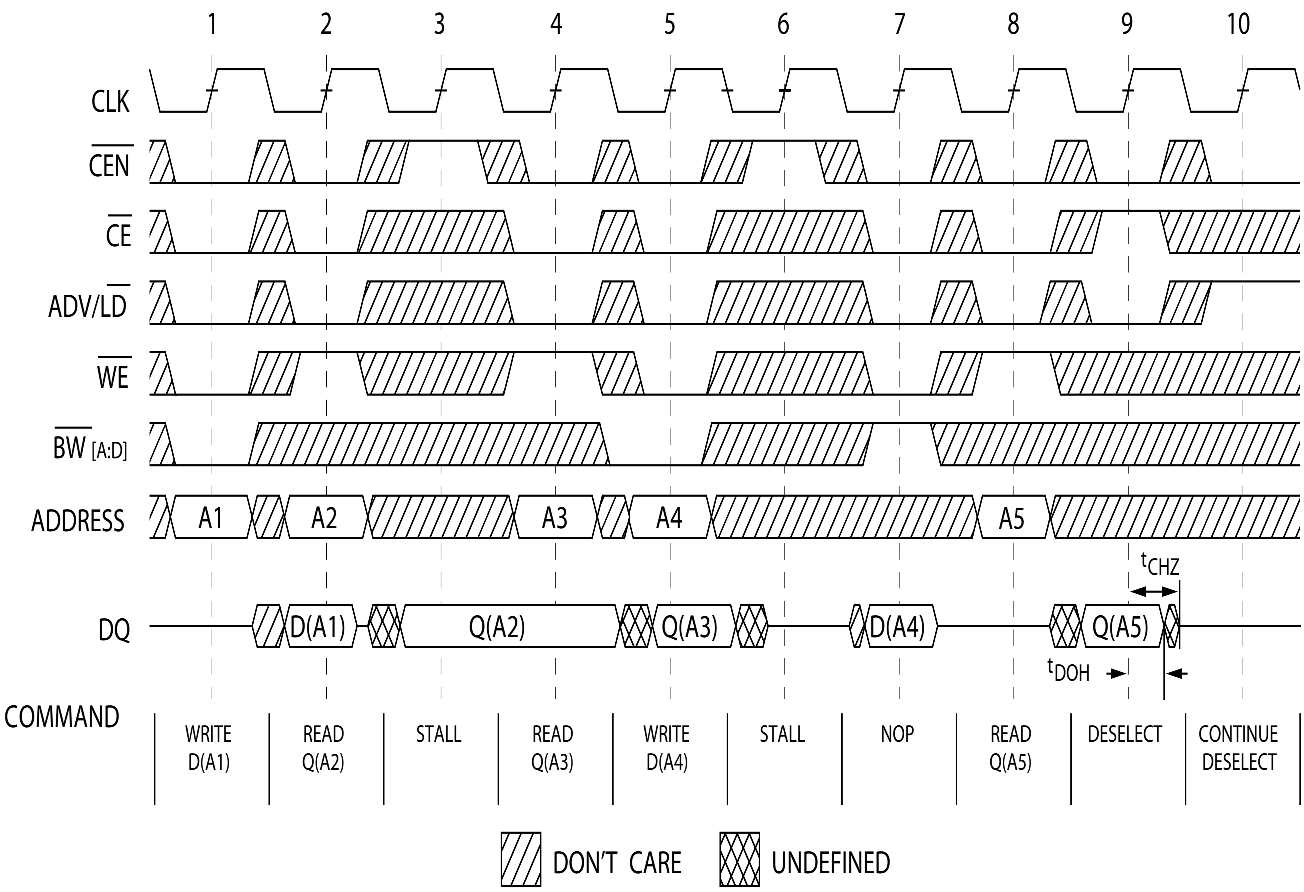


Notes
20. For this waveform ZZ is tied LOW.
21. When $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH, and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH, CE_2 is LOW or $\overline{CE}_3$ is HIGH.
22. Order of the Burst sequence is determined by the status of the MODE (0 = Linear, 1 = Interleaved). Burst operations are optional.

Switching Waveforms (continued)

Figure 2 shows NOP, STALL and DESELECT Cycles waveform.[20, 21, 23]

Figure 2. NOP, STALL and DESELECT Cycles



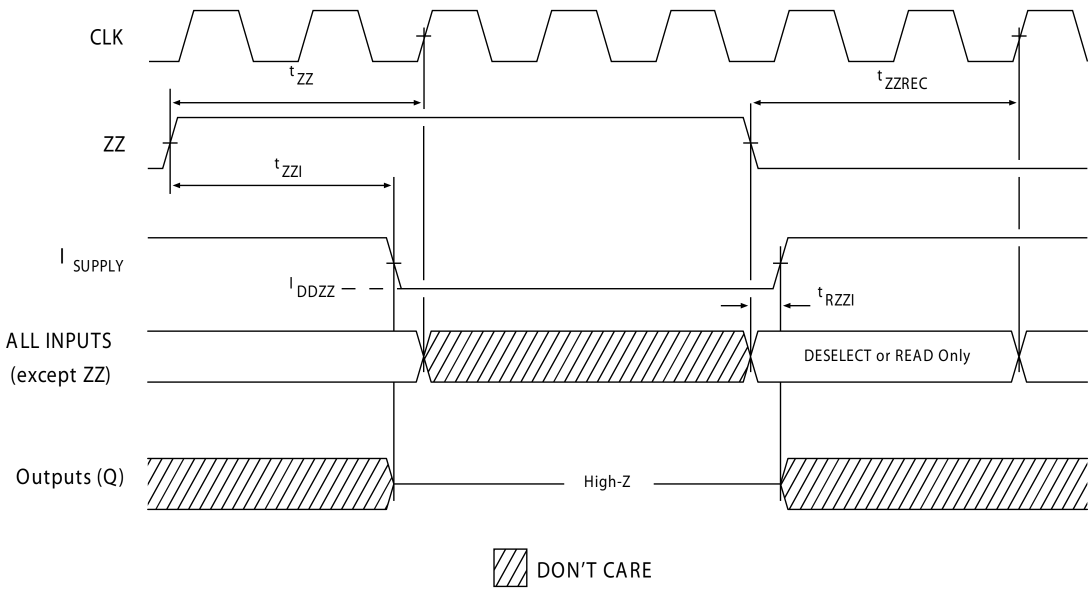
Note

23. The IGNORE CLOCK EDGE or STALL cycle (Clock 3) illustrates $\overline{CEN}$ being used to create a pause. A write is not performed during this cycle.

Switching Waveforms (continued)

Figure 3 shows ZZ Mode timing waveform.[24, 25]

Figure 3. ZZ Mode Timing



Notes

24. Device must be deselected when entering ZZ mode. See "Truth Table" on page 11 for all possible signal conditions to deselect the device.
25. DQs are in high-Z when exiting ZZ sleep mode.

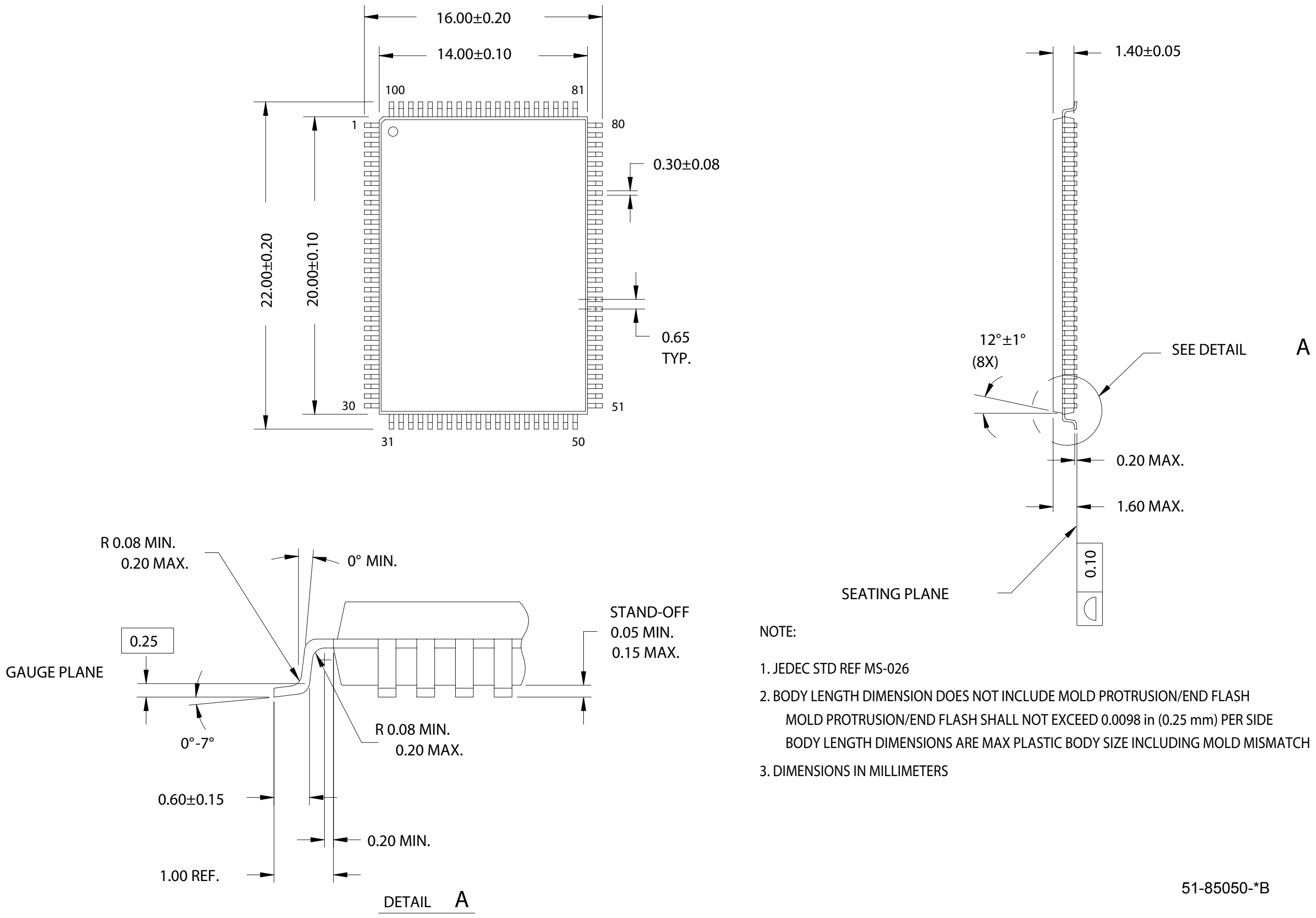
Ordering Information

Not all of the speed, package and temperature ranges are available. Please contact your local sales representative or visit www.cypress.com for actual products offered.

Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
133	CY7C1471V33-133AXC	51-85050	100-Pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Commercial
	CY7C1473V33-133AXC			
	CY7C1471V33-133BZC	51-85165	165-Ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm)	
	CY7C1473V33-133BZC			
	CY7C1471V33-133BZXC	51-85165	165-Ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free	
	CY7C1473V33-133BZXC			
	CY7C1475V33-133BGC	51-85167	209-Ball Fine-Pitch Ball Grid Array (14 × 22 × 1.76 mm)	
	CY7C1475V33-133BGXC		209-Ball Fine-Pitch Ball Grid Array (14 × 22 × 1.76 mm) Pb-Free	
	CY7C1471V33-133AXI	51-85050	100-Pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Industrial
	CY7C1473V33-133AXI			
	CY7C1471V33-133BZI	51-85165	165-Ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm)	
	CY7C1473V33-133BZI			
	CY7C1471V33-133BZXI	51-85165	165-Ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free	
	CY7C1473V33-133BZXI			
	CY7C1475V33-133BGI	51-85167	209-Ball Fine-Pitch Ball Grid Array (14 × 22 × 1.76 mm)	
	CY7C1475V33-133BGXI		209-Ball Fine-Pitch Ball Grid Array (14 × 22 × 1.76 mm) Pb-Free	
117	CY7C1471V33-117AXC	51-85050	100-Pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Commercial
	CY7C1473V33-117AXC			
	CY7C1471V33-117BZC	51-85165	165-Ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm)	
	CY7C1473V33-117BZC			
	CY7C1471V33-117BZXC	51-85165	165-Ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free	
	CY7C1473V33-117BZXC			
	CY7C1475V33-117BGC	51-85167	209-Ball Fine-Pitch Ball Grid Array (14 × 22 × 1.76 mm)	
	CY7C1475V33-117BGXC		209-Ball Fine-Pitch Ball Grid Array (14 × 22 × 1.76 mm) Pb-Free	
	CY7C1471V33-117AXI	51-85050	100-Pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Industrial
	CY7C1473V33-117AXI			
	CY7C1471V33-117BZI	51-85165	165-Ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm)	
	CY7C1473V33-117BZI			
	CY7C1471V33-117BZXI	51-85165	165-Ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free	
	CY7C1473V33-117BZXI			
	CY7C1475V33-117BGI	51-85167	209-Ball Fine-Pitch Ball Grid Array (14 × 22 × 1.76 mm)	
	CY7C1475V33-117BGXI		209-Ball Fine-Pitch Ball Grid Array (14 × 22 × 1.76 mm) Pb-Free	

Package Diagrams

Figure 4. 100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm), 51-85050



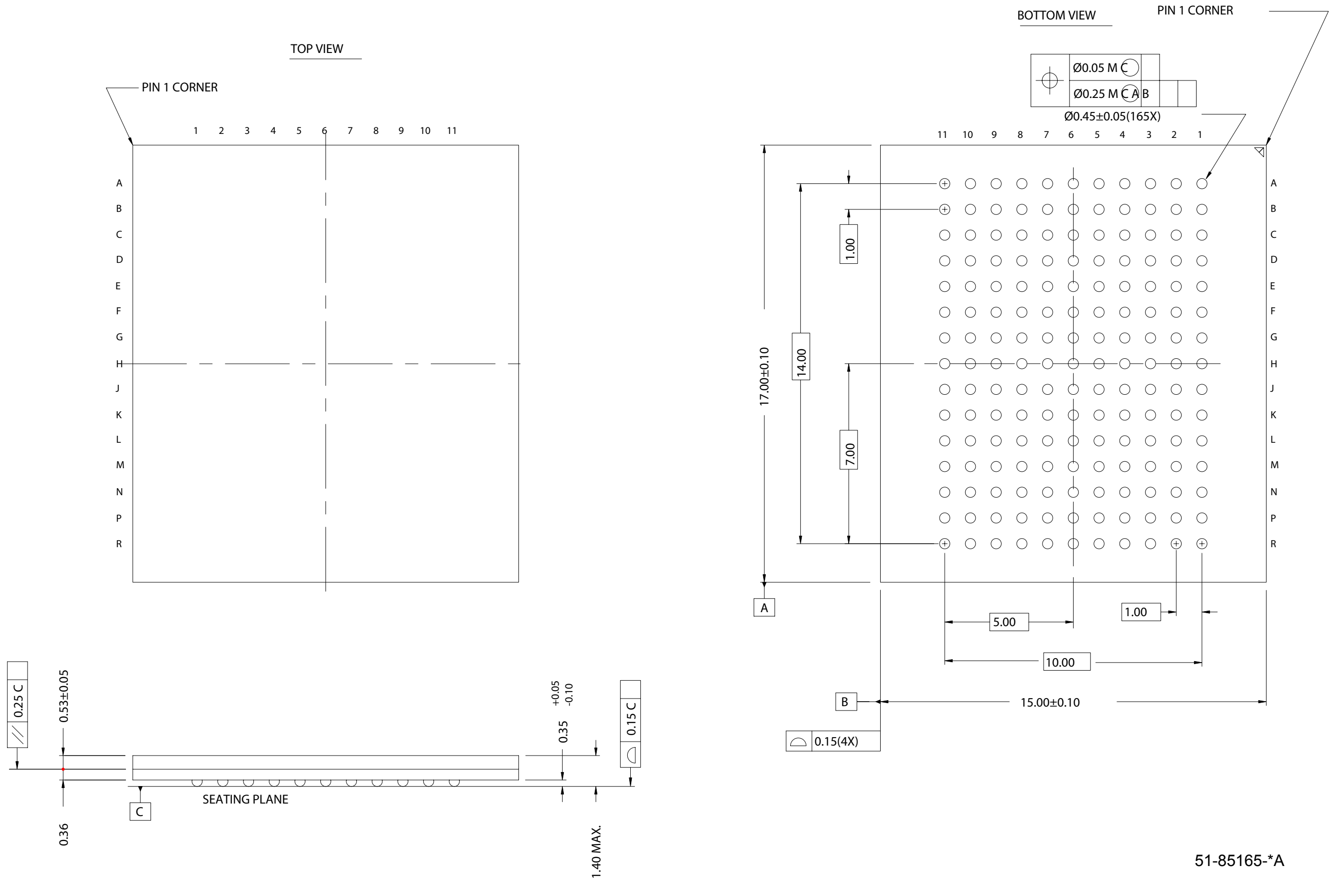
NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85050-*B

Package Diagrams (continued)

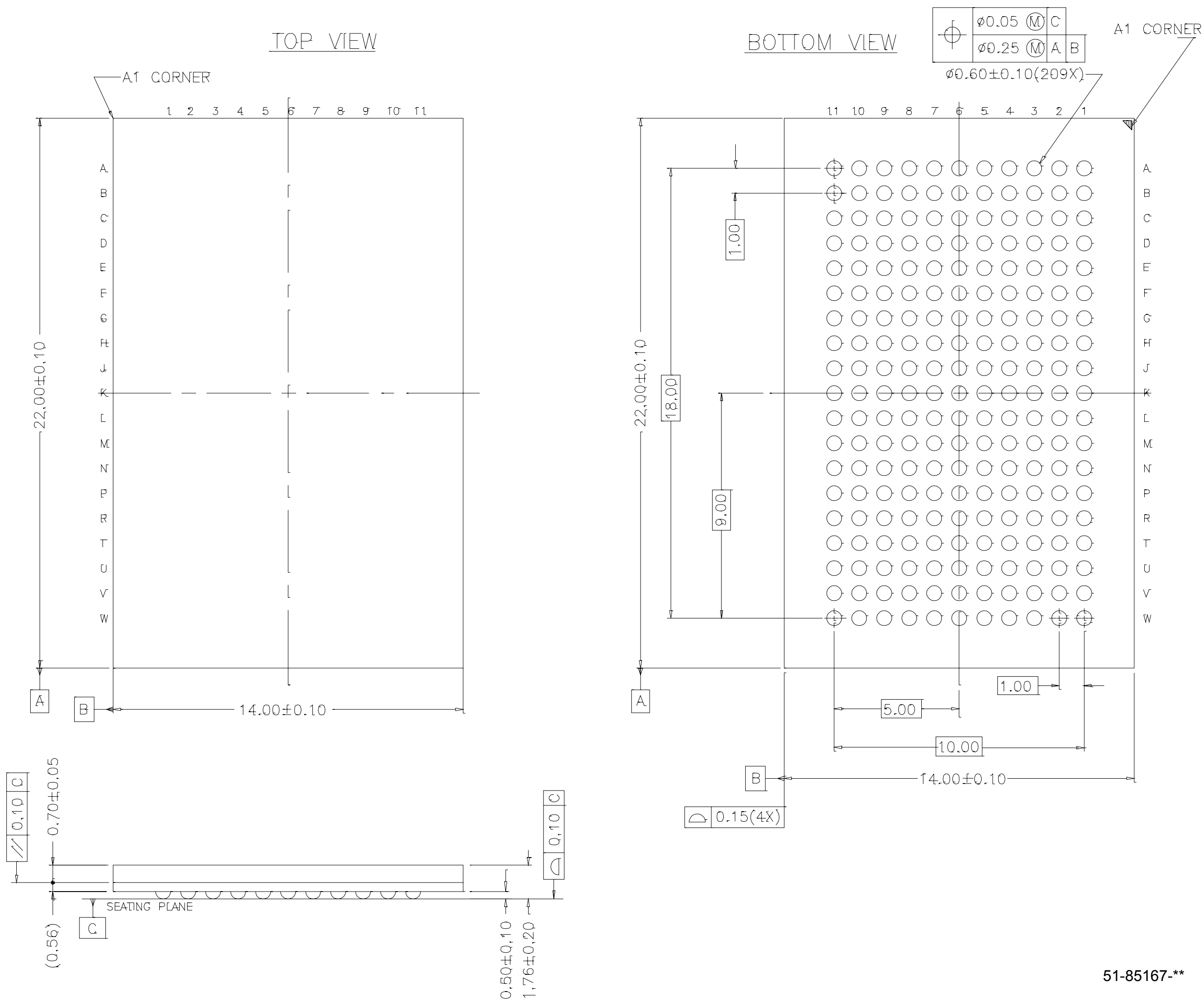
Figure 5. 165-Ball FBGA (15 x 17 x 1.4 mm), 51-85165



51-85165-*A

Package Diagrams (continued)

Figure 6. 209-Ball FBGA (14 x 22 x 1.76 mm), 51-85167



NoBL and No Bus Latency are trademarks of Cypress Semiconductor Corporation. ZBT is a trademark of Integrated Device Technology, Inc. All product and company names mentioned in this document are the trademarks of their respective holders.

Document History Page

Document Title: CY7C1471V33/CY7C1473V33/CY7C1475V33, 72-Mbit (2M x 36/4M x 18/1M x 72) Flow-Through SRAM with NoBL™ Architecture Document Number: 38-05288				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	114675	08/06/02	PKS	New Data Sheet
*A	121521	02/07/03	CJM	Updated features for package offering Updated ordering information Changed Advanced Information to Preliminary
*B	223721	See ECN	NJY	Changed timing diagrams Changed logic block diagrams Modified Functional Description Modified “Functional Overview” section Added boundary scan order for all packages Included thermal numbers and capacitance values for all packages Removed 150-MHz speed grade offering Included ISB and IDD values Changed package outline for 165FBGA package and 209-Ball BGA package Removed 119-BGA package offering
*C	235012	See ECN	RYQ	Minor Change: The data sheets do not match on the spec system and external web
*D	243572	See ECN	NJY	Changed ball H2 from V_{DD} to NC in the 165-Ball FBGA package in page 6 Modified capacitance values on page 21
*E	299511	See ECN	SYT	Removed 117-MHz Speed Bin Changed Θ_{JA} from 16.8 to 24.63 °C/W and Θ_{JC} from 3.3 to 2.28 °C/W for 100 TQFP Package on Page # 21 Added Pb-free information for 100-Pin TQFP, 165 FBGA and 209 BGA Packages Added comment of ‘Pb-free BG packages availability’ below the Ordering Information
*F	320197	See ECN	PCI	Corrected part number typos in the logic block diagram on page# 2
*G	331513	See ECN	PCI	Address expansion pins/balls in the pinouts for all packages are modified as per JEDEC standard Added Address Expansion pins in the Pin Definitions Table Added Industrial Operating Range Modified V_{OL}, V_{OH} Test Conditions Updated Ordering Information Table
*H	416221	See ECN	RXU	Converted from Preliminary to Final Changed address of Cypress Semiconductor Corporation on Page# 1 from “3901 North First Street” to “198 Champion Court” Removed 100MHz Speed bin & Added 117MHz Speed bin Changed the description of I_X from Input Load Current to Input Leakage Current on page# 19 Changed the I_X current values of MODE on page # 19 from –5 μA and 30 μA to –30 μA and 5 μA Changed the I_X current values of ZZ on page # 19 from –30 μA and 5 μA to –5 μA and 30 μA Changed $V_{IH} \leq V_{DD}$ to $V_{IH} < V_{DD}$ on page # 19 Replaced Package Name column with Package Diagram in the Ordering Information table Updated the Ordering Information Table

Document Title: CY7C1471V33/CY7C1473V33/CY7C1475V33, 72-Mbit (2M x 36/4M x 18/1M x 72) Flow-Through SRAM with NoBL™ Architecture Document Number: 38-05288				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
*I	472335	See ECN	VKN	Corrected the typo in the pin configuration for 209-Ball FBGA pinout (Corrected the ball name for H9 to V_{SS} from V_{SSQ}). Added the Maximum Rating for Supply Voltage on V_{DDQ} Relative to GND. Changed t_{TH}, t_{TL} from 25 ns to 20 ns and t_{TDOV} from 5 ns to 10 ns in TAP AC Switching Characteristics table. Updated the Ordering Information table.
*J	1274732	See ECN	VKN/AESA	Corrected typo in the “NOP, STALL and DESELECT Cycles” waveform