TRI-STATE® Programmable Decade/Binary Counters

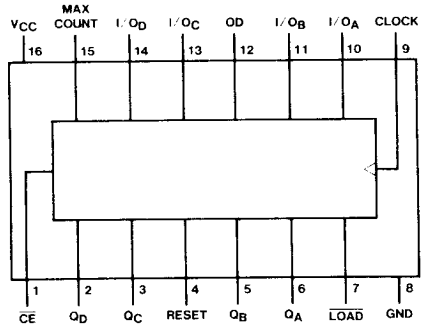
General Description

These circuits are synchronous, edge-sensitive, fully-programmable 4-bit counters. The counters feature both conventional totem-pole and TRI-STATE outputs; such that when the outputs are in the high-impedance mode, they can be used to enter data from the bus lines. In addition, the clear input operates completely independent of all other inputs. During the programming operation, data is loaded into the flip-flops on the positive-going edge of the clock pulse. To facilitate cascading of these counters, the MAX COUNT output can be tied directly into the count enable input of the next counter.

Features

- DM7555/8555—Decade counter
- DM7556/8556—Binary counter
- Typical clock frequency 35 MHz
- TRI-STATE outputs
- Fully independent clear
- Synchronous loading
- Cascading circuitry provided internally

Connection Diagram



7555 (J,W)
7556 (J,W)

8555 (N)
8556 (N)

Truth Table

Control Inputs					I/O Ports				Active Outputs			
$\overline{LOAD}$	$\overline{CE}$	CLK	OD	Reset	I/O_A	I/O_B	I/O_C	I/O_D	Q_A	Q_B	Q_C	Q_D
H	X	X	L	H	L	L	L	L	L	L	L	L
H	X	X	H	H	Z	Z	Z	Z	L	L	L	L
H	X	L	L	L	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	X	L	H	L	Z	Z	Z	Z	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	H	↑	L	L	a	b	c	d	A	B	C	D
H	L	↑	L	L			COUNT				COUNT	
H	L	↑	H	L	Z	Z	Z	Z			COUNT	

The I/O pins are used as inputs when they are TRI-STATED, and the $\overline{LOAD}$ input is Low. They are outputs and active when $\overline{LOAD}$ input is High and OD is Low.

H = High Level (Steady State)

L = Low Level (Steady State)

X = Don't Care including transitions

a, b, c, d = The level of the steady state input at inputs A, B, C, D respectively

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, Q_D repectively, before the indicated steady state input conditions were established.

7

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Conditions		DM75/85						Units
				55			56			
				Min	Typ (1)	Max	Min	Typ (1)	Max	
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5			−1.5	V
I_{OH}	High Level Output Current		DM75			−2.0			−2.0	mA
			DM85			−5.2			−5.2	
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = Max		2.4			2.4			V
I_{OL}	Low Level Output Current					16			16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.4			0.4			V
$I_{O(OFF)}$	Off State (High Impedance State) Output Current	V_{CC} = Max, V_{IH} = 2 V, V_{IL} = Max	V_O = 0.4 V			−40			−40	μA
			V_O = 2.4 V			40			40	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5 V				1			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4 V				40			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4 V				−1.6			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (2)		−25		−70	−25		−70	mA
I_{CC}	Supply Current	V_{CC} = Max			80	110		75	100	mA

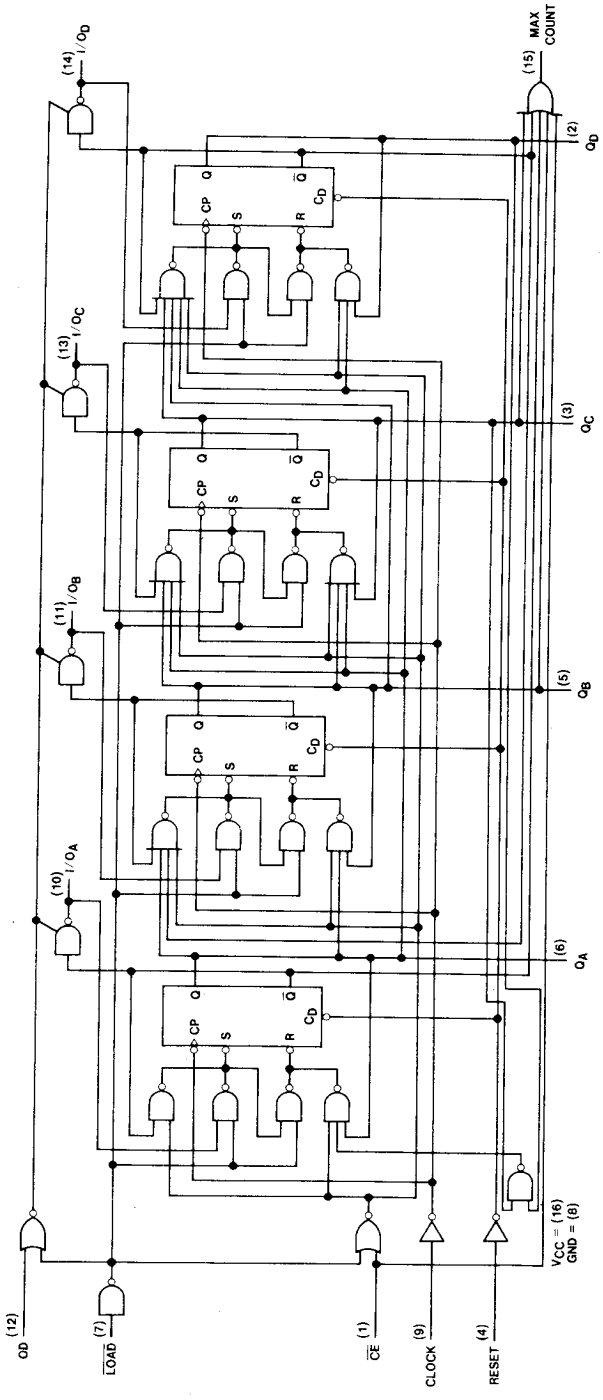
Note 1: All typical values are at V_{CC} = 5 V, T_A = 25°C.
Note 2: Not more than one output should be shorted at a time.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C.

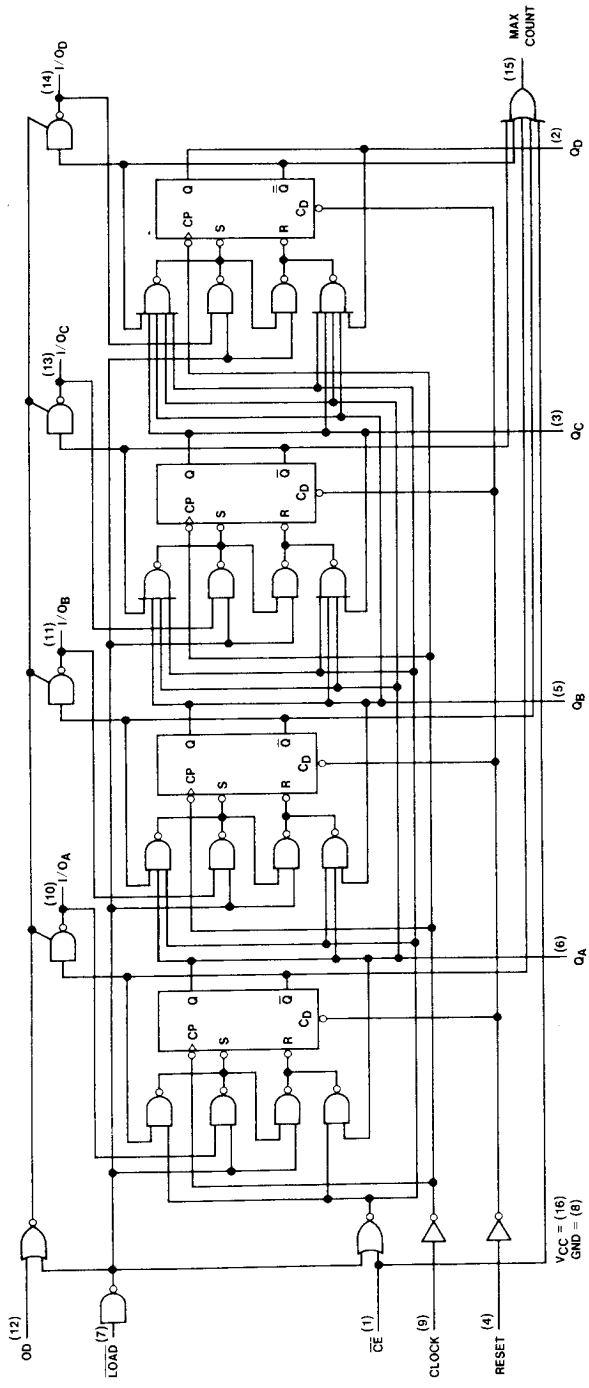
Parameter			From	To	Conditions	DM75/8555, 56 Min	DM75/8555, 56 Typ	DM75/8555, 56 Max	Units
f_{MAX}	Maximum Clock Frequency				C_L = 50 pF, R_L = 400 Ω	25	35		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clock	Output			15	22	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Clock	Output			34	44	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clock	Max Count			23	33	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Clock	Max Count			23	33	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Reset	Output			30	44	ns
t_{ZH}	Output Enable Time to High Level		OD	Output			13	20	ns
t_{ZL}	Output Enable Time to Low Level		OD	Output			14	20	ns
t_{HZ}	Output Disable Time from High Level		OD	Output	C_L = 5 pF, R_L = 400 Ω		6	12	ns
t_{LZ}	Output Disable Time from Low Level		OD	Output			12	20	ns
t_W	Minimum Pulse Width	Clock				25			ns
		Clear				20			
		Load				30			
$t_{\overline{CE}}$	Count Enable Time	Setup				30			ns
		Hold				−30			
$t_{SETUP(1)}$	Setup Time—High Logic Level	Data				25			ns
		Load				30			
$t_{HOLD(1)}$	Hold Time—High Logic Level	Data				5			ns
		Load				−10			
$t_{SETUP(0)}$	Setup Time—Low Logic Level	Data				30			ns
		Load				25			
$t_{HOLD(0)}$	Hold Time—Low Logic Level	Data				5			ns
		Load				−10			

7

Logic Diagrams



Logic Diagrams (Continued)



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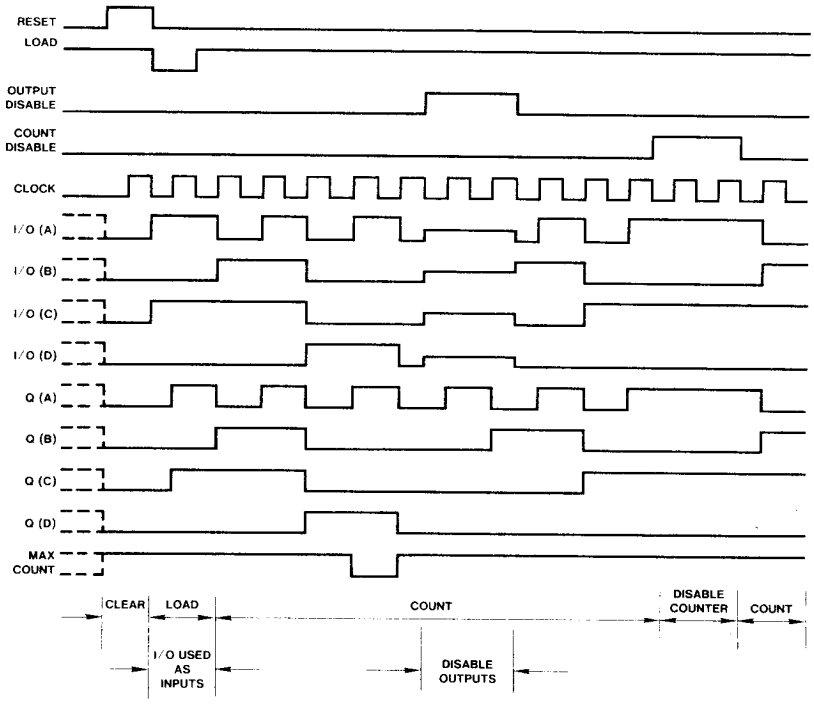
Timing Diagrams

55 Typical Clear, Preset, Count, Inhibit Sequence

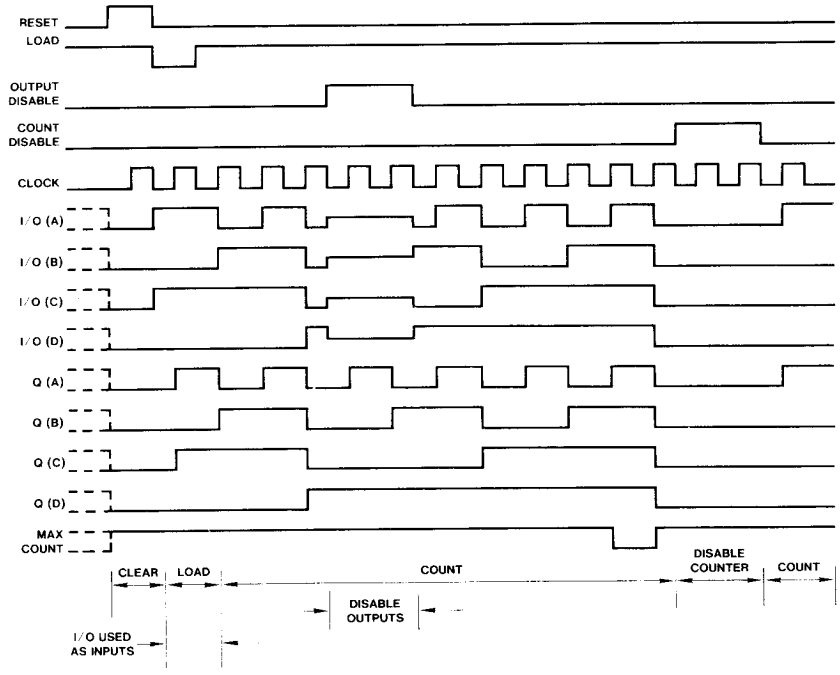


Sequence

(1) Clear to zero.
(2) Load BCD five.
(3) Count six, seven, eight, nine, zero, one, two, three, four.
(4) Disable TRI-STATE outputs.
(5) Disable counter.
(6) Count to six.

Timing Diagrams (Continued)

56 Typical Clear, Preset, Count, Inhibit Sequence



Sequence

(1) Clear to zero.
(2) Load binary five.
(3) Count six, seven, eight, nine, ten, eleven, twelve, thirteen, fourteen, fifteen, zero.
(4) Disable TRI-STATE outputs.
(5) Disable counter.
(6) Count to one.

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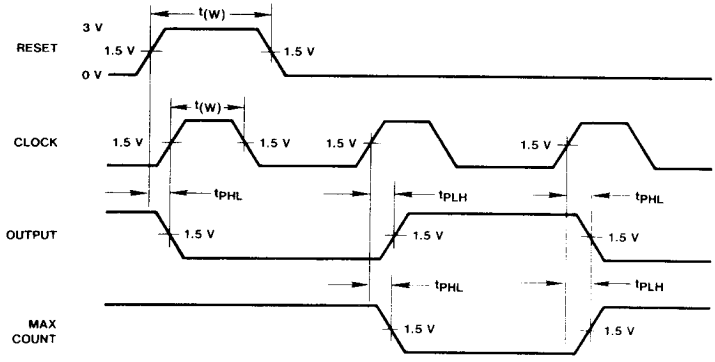
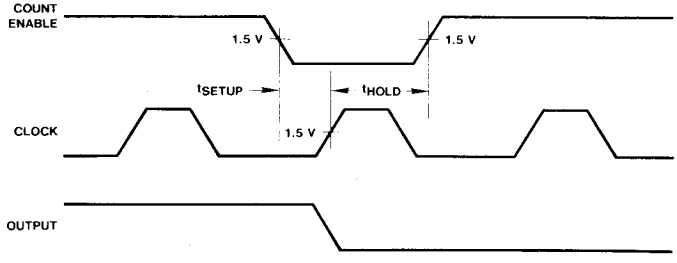
Switching Time Waveforms

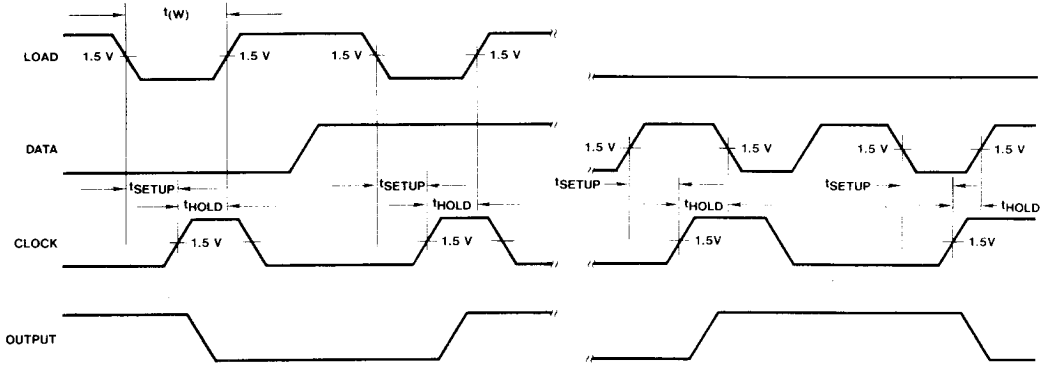
Clock and Reset Voltage



Count Enable and Clock



Load, Data and Clock



Output Disable