SA58635

2 × 25 mW class-G stereo headphone driver with I²C-bus volume control

Rev. 01 — 26 March 2010 Product data sheet

1. General description

The SA58635 is a stereo, class-G headphone driver with I²C-bus volume control. The I²C-bus control allows maximum flexibility with digital volume control, independent channel enable and mute control.

The output of the SA58635 is referenced around true ground zero. It is designed to operate at the low supply current of 1.5 mA making it battery friendly. A unique power management technique provides class-G power efficiency by using a buck converter to step down the battery supply from a typical lithium ion battery (4.8 V to 2.3 V). Efficiency is further increased by allowing the output amplifier/driver to operate at multiple voltage rails based on the output/input swing.

The SA58635 delivers 2 × 25 mW minimum into 16 Ω and 32 Ω loads. The SA58635 provides thermal shutdown and self limiting current protection.

The SA58635 is a high fidelity HP driver amplifier with a S/N of 100 dB minimum. An excellent PSRR of more than 100 dB, differential input circuit topology allows for maximum noise immunity in the noisy mobile phone environment.

The SA58635 is available in a 16-bump WLCSP (Wafer Level Chip-Size Package) making it ideal choice for cellular handsets and portable media players.

2. Features

- Power supply range: 2.3 V to 5.5 V
- High efficiency employing class-G dynamic power management
- 2 × 25 mW into 16 Ω or 32 Ω at THD+N = 1 %
- Very low THD+N at 0.02 % at V_O of $0.7V_{o(RMS)}$ and R_L of 47 Ω
- Integrated charge pump to eliminate DC blocking capacitors, reduce cost and PCB space while improving low frequency audio fidelity
- Excellent PSRR: > 100 dB
- S/N performance of 100 dB minimum
- Low supply current: 1.5 mA typical
- Low shutdown current: 5 μA maximum
- I²C-bus interface for −59 dB to ±4 dB volume control, independent channel enable, mute and software shutdown
- Self limiting current with thermal protection and ground loop noise suppression
- Pop-and-click suppression
- Available in 1.7 mm × 1.7 mm 16-bump WLCSP

3. Applications

- Wireless and cellular handsets
- Portable media players
- Portable DVD player
- Notebook PC
- High fidelity applications

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
SA58635UK	WLCSP16	wafer level chip-size package; 16 balls; 1.7 × 1.7 × 0.56 mm	SA58635UK

5. Block diagram

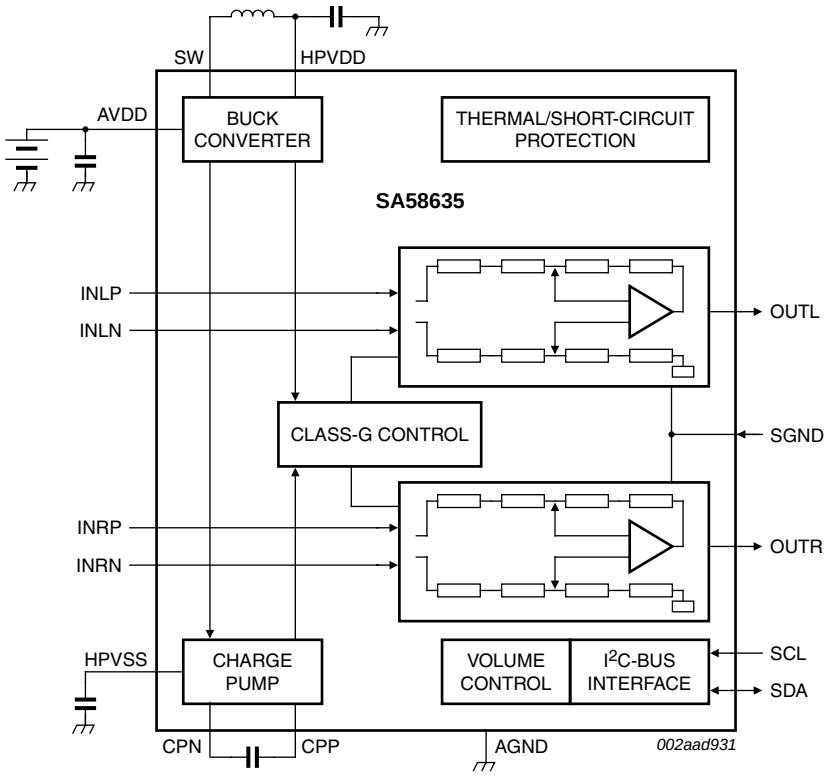


Fig 1. Block diagram of SA58635

6. Pinning information

6.1 Pinning

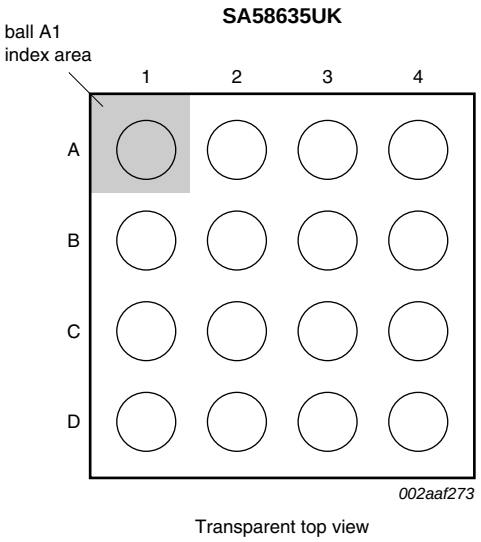


Fig 2. Pin configuration for WLCSP16

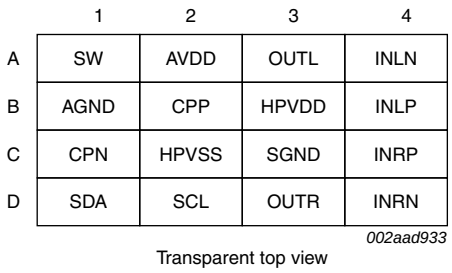


Fig 3. Ball mapping for WLCSP16

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
SW	A1	buck converter switching mode
AVDD	A2	analog supply; same as battery
OUTL	A3	headphone left channel output
INLN	A4	left channel negative differential input
AGND	B1	analog supply ground
CPP	B2	charge pump positive capacitor
HPVDD	B3	buck converter output voltage
INLP	B4	left channel positive differential input
CPN	C1	charge pump negative capacitor
HPVSS	C2	charge pump negative output voltage
SGND	C3	ground sense; connect to headphone jack ground
INRP	C4	right channel positive differential input
SDA	D1	I^2C-bus serial data
SCL	D2	I^2C-bus serial clock
OUTR	D3	headphone right channel output
INRN	D4	right channel negative differential input

7. Functional description

Refer to Figure 1 “Block diagram of SA58635”.

7.1 Device address

Following a START condition, the bus master must output the address of the slave it is accessing.

The SA58635 responds to two slave addresses: 1100 000xb for standard accesses and the General Call writes (0000 0000b) for software reset. The last bit of the address byte defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

When a reset of the I^2C-bus needs to be performed by the master, the master will write to the General Call address followed by a write of the reset command (0000 0110b). When a General Call reset command is sent by the master, the SA58635 will respond with an acknowledge and execute a reset to the digital logic. This will return the register set and the volume controls to the Power-On Reset (POR) values.

7.2 Control register

Following the successful acknowledgement of the slave address, the bus master will send a byte to the SA58635, which will be stored in the Control register.

The lowest 3 bits are used as a pointer to determine which register will be accessed (D[2:0]). The remaining bits are not used and are ignored.

7.3 Register definitions

Table 3. Register summary

Register number (hex)	Name	Type	Function
00	-	-	Reserved; this address is empty and will be NACKed.
01	MODE1	read/write	Contains the left and right channel amplifier enable bits, thermal status and the software shutdown bit.
02	VOLCTL	read/write	Volume setting and mute left and right bits.
03	HIZ	read/write	High-impedance controls for left and right channel.
04	ID	read only	Vendor Identification and chip version number.
05	-	-	Reserved; this address is empty and will be NACKed.
06	TEST1	read/write	This register is for manufacturing test.
07	-	read/write	Reserved; this register is empty and will be NACKed.

7.3.1 MODE1 register, MODE1

Table 4. MODE1 - Mode register 1 (address 01h) bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	HP_EN_L	R/W	0*	Left channel inactive. A zero will turn off the left channel.
			1	Left channel active.
6	HP_EN_R	R/W	0*	Right channel inactive. A zero will turn off the right channel.
			1	Right channel active.
5	-	read only	0*	Reserved; always reads back as a 0.
4	-	read only	0*	Reserved; always reads back as a 0.
3	-	read only	0*	Reserved; always reads back as a 0.
2	-	read only	0*	Reserved; always reads back as a 0.
1	THERMAL	read only	0*	Device is operating normally.
			1	Device is in thermal shutdown.
0	SWS	R/W	0*	Device is enabled.
			1	Software shutdown; charge pump is disabled.

7.3.2 Volume control register, VOLCTL

Table 5. VOLCTL - Volume control register (address 02h) bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	MUTEL	R/W	0	A zero indicates that the left channel is not muted.
			1*	Left channel is muted.
6	MUTER	R/W	0	A zero indicates that the right channel is not muted.
			1*	Right channel is muted.
5 to 1	VOL[4:0]	R/W	0*	These bits indicate the volume on the outputs per the gain table shown in Table 9.
0	-	read only	0*	This bit is reserved and will always return a zero.

7.3.3 High-impedance register, HIZ

Table 6. HIZ - High-impedance register (address 03h) bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7 to 2	-	read only	0*	Unused; always returns 0.
1	HIZL	R/W	0*	Device outputs are not in high-impedance.
			1	Device outputs are in high-impedance.
0	HIZR	R/W	0*	Device outputs are not in high-impedance.
			1	Device outputs are in high-impedance.

7.3.4 Chip identification register, ID

Table 7. ID - Chip identification register (address 04h) bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7 to 6	SUPPLIER	read only	11b*	This is the supplier identification for this device, indicating that this device is manufactured by NXP Semiconductors.
5 to 4	-	read only	00b*	Unused; always returns 0.
3 to 0	VER[3:0]	read only	0000b	These bits indicate the version number for this device. Initial silicon will be set to 0h.

7.3.5 Test register 1, TEST1

Table 8. TEST1 - Test register 1 (address 06h) bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7 to 0	-	R/W	00h*	Software should refrain from writing to this register. Software should write only 0's to this register. Values other than 0 may cause the part to not function as expected.

7.4 Volume control

Volume levels are set in the VOLCTL register (register 02h) as described in Section 7.3.2. As the volume is changed including muting and un-muting, the SA58635, will step to the new value at an incremental (or decremental) rate of approximately one millisecond per step. A full sweep from 00h to 1Fh will take roughly 32 milliseconds. The VOLCTL register values represent a gain on the output channels as indicated in Table 9.

Table 9. Volume and gain control

Volume control word	Gain ± 0.5 (dB)
0000 000x	−59
0000 001x	−55
0000 010x	−51
0000 011x	−47
0000 100x	−43
0000 101x	−39
0000 110x	−35
0000 111x	−31
0001 000x	−27
0001 001x	−25
0001 010x	−23
0001 011x	−21
0001 100x	−19
0001 101x	−17
0001 110x	−15
0001 111x	−13
0010 000x	−11
0010 001x	−10
0010 010x	−9
0010 011x	−8
0010 100x	−7
0010 101x	−6
0010 110x	−5
0010 111x	−4
0011 000x	−3
0011 001x	−2
0011 010x	−1
0011 011x	0
0011 100x	+1
0011 101x	+2
0011 110x	+3
0011 111x	+4
1xxx xxxx	Mute Left active
x1xx xxxx	Mute Right active

7.5 Power-on reset

When power is applied to AVDD, an internal power-on reset holds the SA58635 in a reset condition until AVDD has reached V_{POR}. At this point, the reset condition is released and the SA58635 registers and I²C-bus state machine are initialized to their default states (all zeroes) causing all the channels to be deselected. Thereafter, AVDD must be lowered below 0.2 V to reset the device.

8. Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

8.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 4).

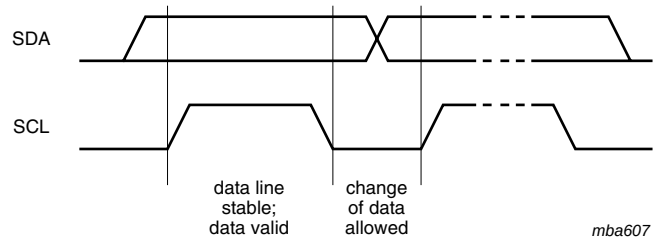


Fig 4. Bit transfer

8.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 5).

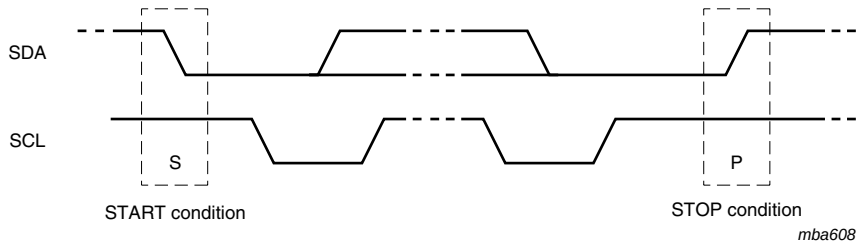


Fig 5. Definition of START and STOP conditions

8.2 System configuration

A device generating a message is a ‘transmitter’; a device receiving is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’ (see Figure 6).

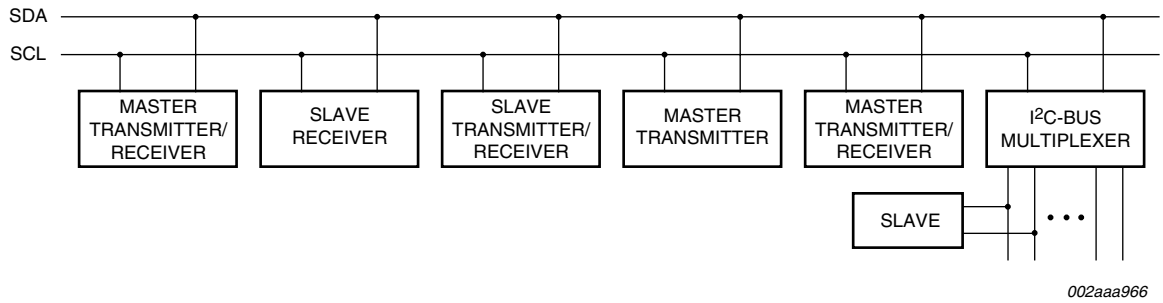


Fig 6. System configuration

8.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up time and hold time must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

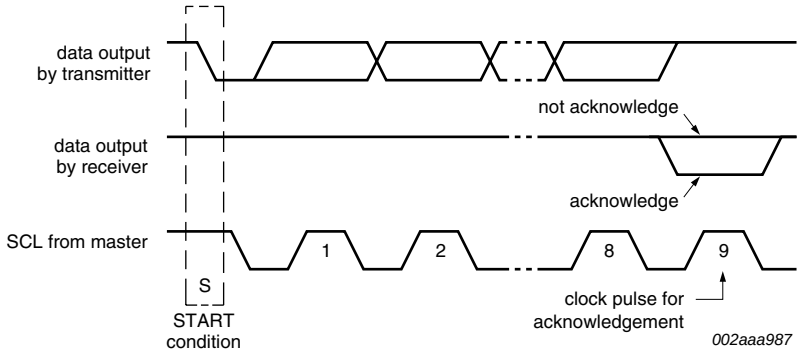
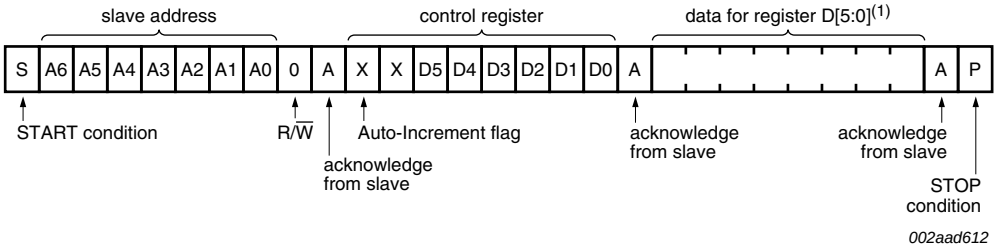


Fig 7. Acknowledgement on the I2C-bus

9. Bus transactions



(1) See Table 3 for register definition.

Fig 8. Write to a specific register

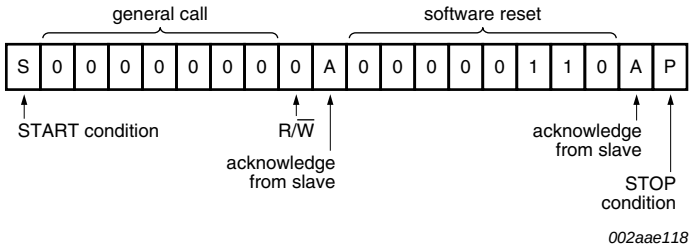


Fig 9. Software reset

10. Limiting values

Table 10. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage	Active mode		−0.3	+6.0	V
		Shutdown mode		−0.3	+6.0	V
V_I	input voltage	INRN, INRP, INLN, INLP		−0.3	2.1	V
V_{IO}	input/output voltage	SCL, SDA		V_{AGND} − 0.5	V_{DD}	V
I_{BR}	breakdown current	continuous	[2]	-	200	mA
P	power dissipation	WLCSP16; derating factor 10 mW/K				
		T_{amb} = 25 °C		-	1000	mW
		T_{amb} = 70 °C		-	550	mW
		T_{amb} = 85 °C		-	400	mW
T_{amb}	ambient temperature	operating in free air		−40	+85	°C
T_j	junction temperature	operating		−40	+85	°C
T_{stg}	storage temperature			−65	+150	°C
V_{ESD}	electrostatic discharge voltage	human body model		±4000	-	V
		machine model		±300	-	V
		charged-device model		±750	-	V
		device use level:				
		IEC61000-4-2 level 4, contact	[3]	±30	-	kV
		IEC61000-4-2 level 4, air discharge	[3]	±30	-	kV

[1] V_{DD} is the supply voltage on pin AVDD.

[2] Breakdown current of output protection diodes.

[3] ESD shock needs to be conducted to the connector pins (see Figure 10).

All functions of a device/system perform as designed during and after exposure to a disturbance.

Remark: External ESD suppressor ASIP protects the amplifier outputs. Suppressor is between amplifier and connector; 15 Ω serial resistance + 5 nF capacitor and Zener diodes (14 V breakdown voltage) connected to the ground. In addition, there is a ferrite bead in series between suppressor and connector (see Figure 10).

Remark: Air discharge test can be ignored if contact discharge test range is increased to corresponding same voltages as air discharge (reason: contact discharge is more stable and repeatable test than air discharge).

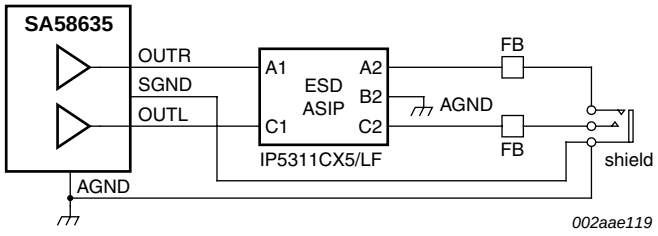


Fig 10. ESD suppressor ASIP

11. Static characteristics

Table 11. Static characteristics

V_{DD} = 3.6 V; R_L = 15 Ω + 32 Ω; two channels in phase; T_{amb} = 25 °C, unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage	continuous	2.3	-	5.5	V
I_{DD}	supply current	both channels enabled; no audio signal	-	1.5	-	mA
$I_{DD(sd)}$	shutdown mode supply current	I²C-bus in operation	-	1	5	μA
$V_{i(cm)}$	common-mode input voltage	differential	−1.3	-	+1.3	V
V_{POR}	power-on reset voltage		-	2.1	-	V
$\lvert V_{O(offset)}\rvert$	output offset voltage	absolute value; both channels enabled	-	0.5	3	mV
PSRR	power supply rejection ratio	G_v = 0 dB	100	-	-	dB
Z_i	input impedance	differential	20	-	-	kΩ
Z_o	output impedance	high-impedance mode				
		<40 kHz	10	-	-	kΩ
		6 MHz	500	-	-	Ω
		36 MHz	75	-	-	Ω
I²C-bus pins (SCL, SDA)						
I_{OL}	LOW-level output current	SDA output; V_{OL} = 0.4 V; V_{DD} = 3.6 V	3	-	-	mA
I_{LI}	input leakage current	SCL, SDA	−1	-	+1	μA
C_i	input capacitance	SCL, SDA	-	-	10	pF
V_{IH}	HIGH-level input voltage	SCL, SDA	1.2	-	-	V
V_{IL}	LOW-level input voltage	SCL, SDA	-	-	0.6	V

[1] V_{DD} is the supply voltage on pin AVDD.

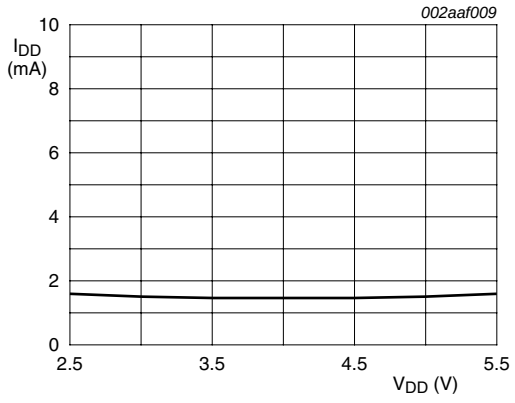


Fig 11. Supply current versus supply voltage

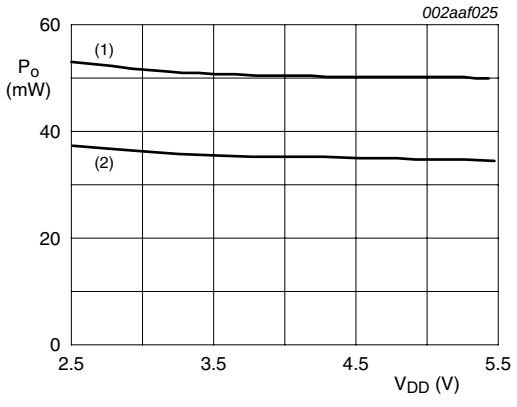
12. Dynamic characteristics

Table 12. Dynamic characteristics

V_{DD} = 3.6 V; R_L = 15 Ω + 32 Ω; two channels in phase; T_{amb} = 25 °C; unless otherwise specified.[1]

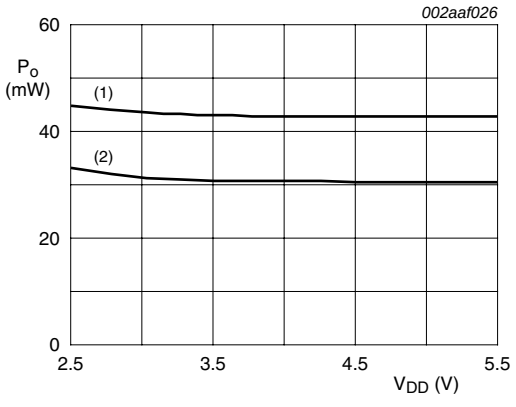
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_o	output power	stereo; f = 1 kHz; THD+N = 1 %	2 × 25	-	-	mW
I_{DD}	supply current	output 2 × 100 μW at 3 dB crest factor	-	2.5	3.5	mA
		output 2 × 500 μW at 3 dB crest factor	-	4.5	5.5	mA
		output 2 × 1 mW at 3 dB crest factor	-	6.5	7.5	mA
$V_{o(RMS)}$	RMS output voltage	amplifier				
		R_L = 16 Ω; THD+N = 1 %; L + R in phase	0.63	-	-	V
		R_L = 32 Ω; THD+N = 1 %; L + R in phase	0.89	-	-	V
THD+N	total harmonic distortion-plus-noise	f = 1 kHz; V_O = 700 mV (RMS)	-	-	0.02	%
SVRR	supply voltage ripple rejection	G_v = 4 dB; f = 217 Hz	75	-	-	dB
$\alpha_{ct(ch)}$	channel crosstalk	P_o = 15 mW; f = 1 kHz	90	-	-	dB
		line out > 10 kΩ	80	-	-	dB
$V_{n(o)(RMS)}$	RMS output noise voltage	G_v = 4 dB; A-weight	-	7	-	μV
$t_{d(sd-startup)}$	delay time from shutdown to start-up		-	-	15	ms
S/N	signal-to-noise ratio	V_O = 1 V (RMS); f = 1 kHz	100	-	-	dB
T_{off}	switch-off temperature	threshold	-	180	-	°C
		hysteresis	-	35	-	°C

[1] V_{DD} is the supply voltage on pin AVDD.



(1) THD+N = 10 %
(2) THD+N = 1 %

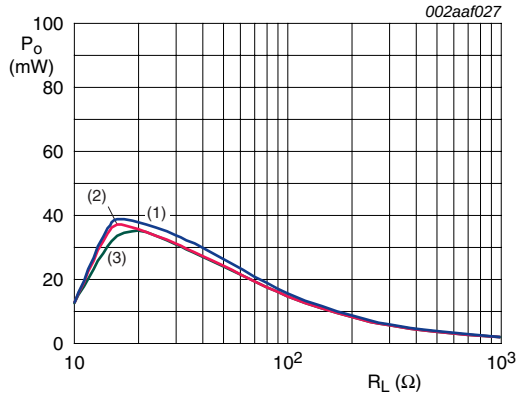
a. R_L = 16 Ω; in phase



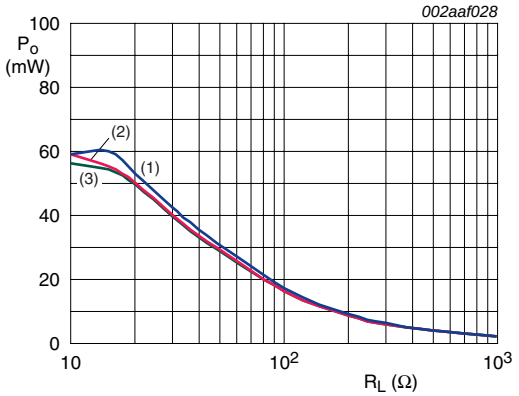
(1) THD+N + 10 %
(2) THD+N + 1 %

b. R_L = 32 Ω; in phase

Fig 12. Output power per channel versus supply voltage



a. THD+N = 1 %; in phase



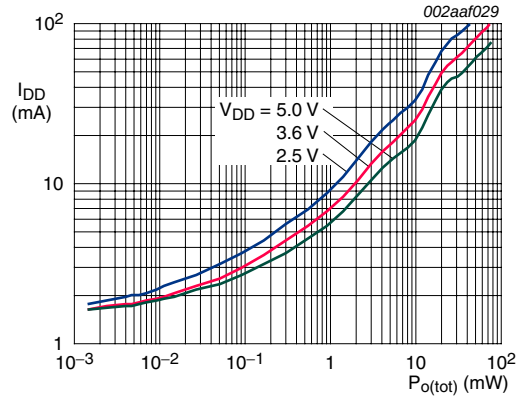
b. THD+N = 1 %; out of phase

(1) V_{DD} = 2.5 V

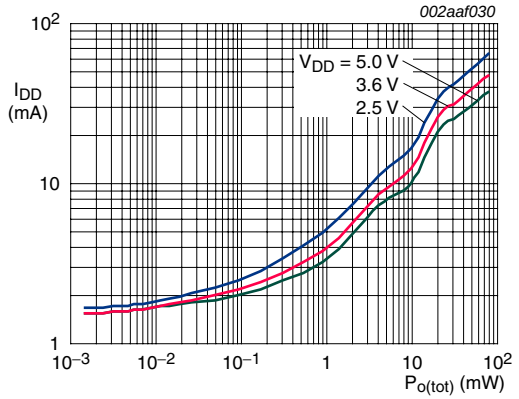
(2) V_{DD} = 3.6 V

(3) V_{DD} = 5 V

Fig 13. Output power per channel versus load resistance

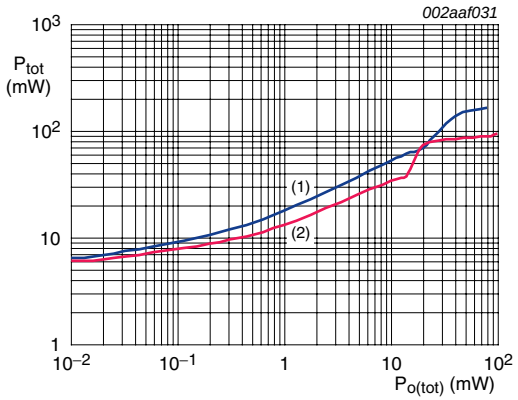


a. f = 1 kHz; R_L = 16 Ω



b. f = 1 kHz; R_L = 32 Ω

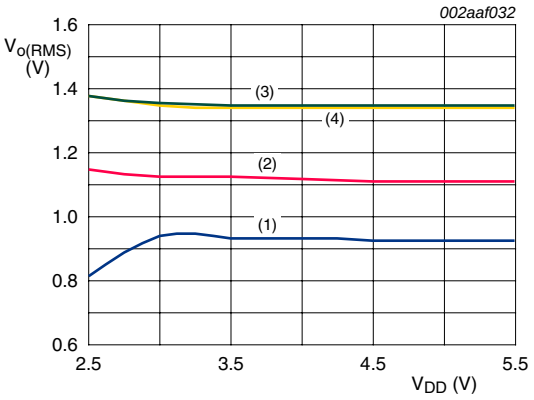
Fig 14. Supply current versus total output power



(1) R_L = 16 Ω

(2) R_L = 32 Ω

Fig 15. Total power dissipation versus total output power



f = 1 kHz; THD+N = 1 %

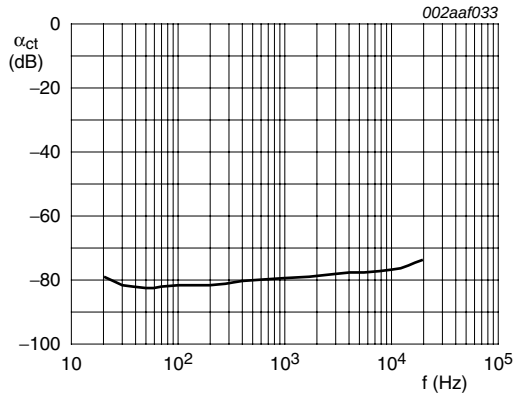
(1) R_L = 16 Ω

(2) R_L = 32 Ω

(3) R_L = 600 Ω

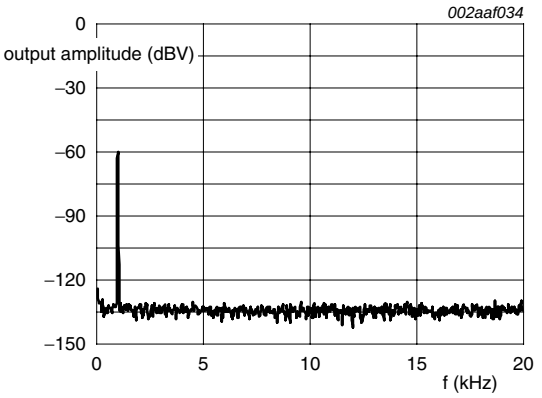
(4) R_L 1000 Ω

Fig 16. RMS output voltage versus supply voltage



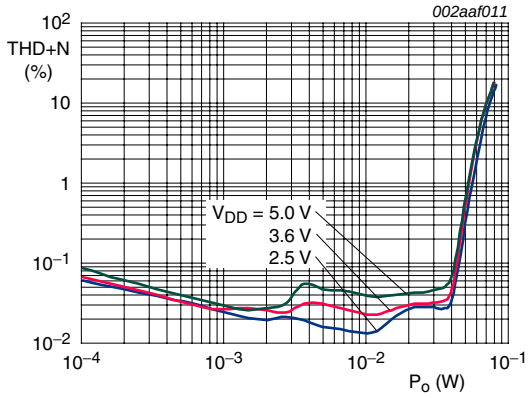
R_L = 16 Ω; P_o = 15 mW

Fig 17. Crosstalk versus frequency

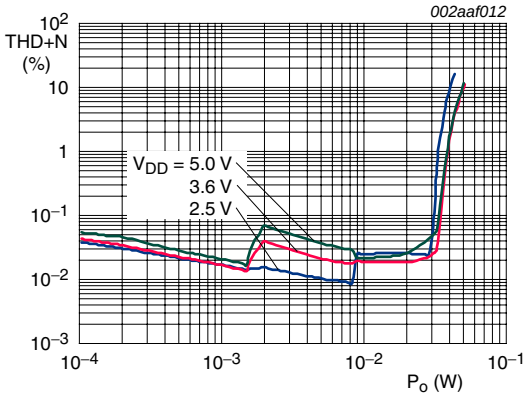


R_L = 16 Ω

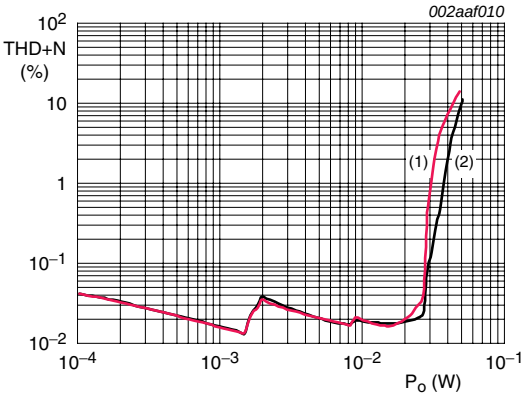
Fig 18. Output amplitude versus frequency



a. f = 1 kHz; R_L = 16 Ω



b. f = 1 kHz; R_L = 32 Ω

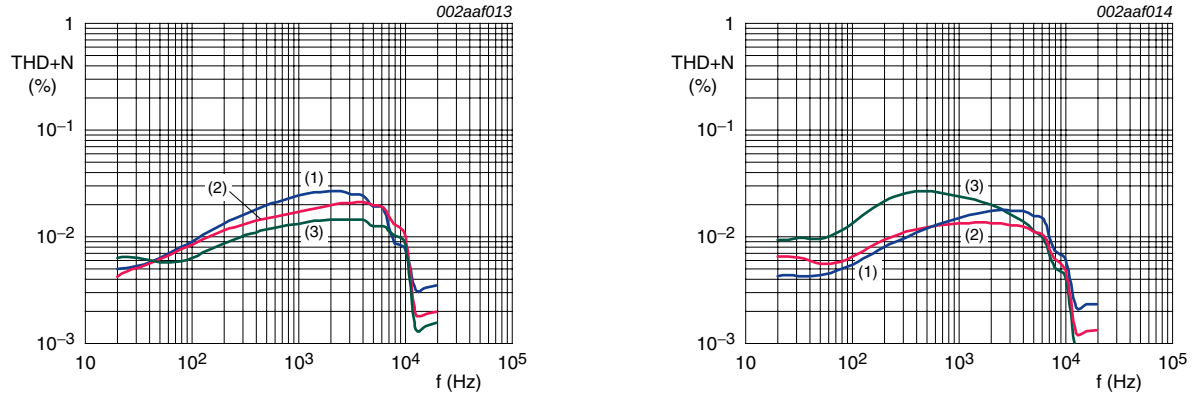


(1) In phase.

(2) Out of phase.

c. f = 1 kHz; R_L = 32 Ω; V_{DD} = 3.6 V

Fig 19. Total harmonic distortion-plus-noise versus output power



a. R_L = 16 Ω

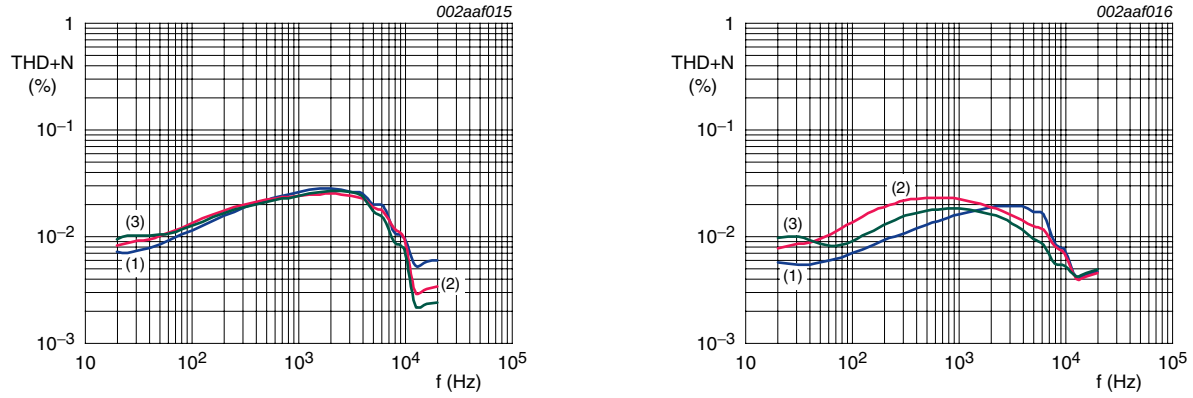
b. R_L = 32 Ω

(1) P_o = 1 mW / channel

(2) P_o = 4 mW / channel

(3) P_o = 10 mW / channel

Fig 20. Total harmonic distortion-plus-noise versus frequency (V_{DD} = 2.5 V)



a. R_L = 16 Ω

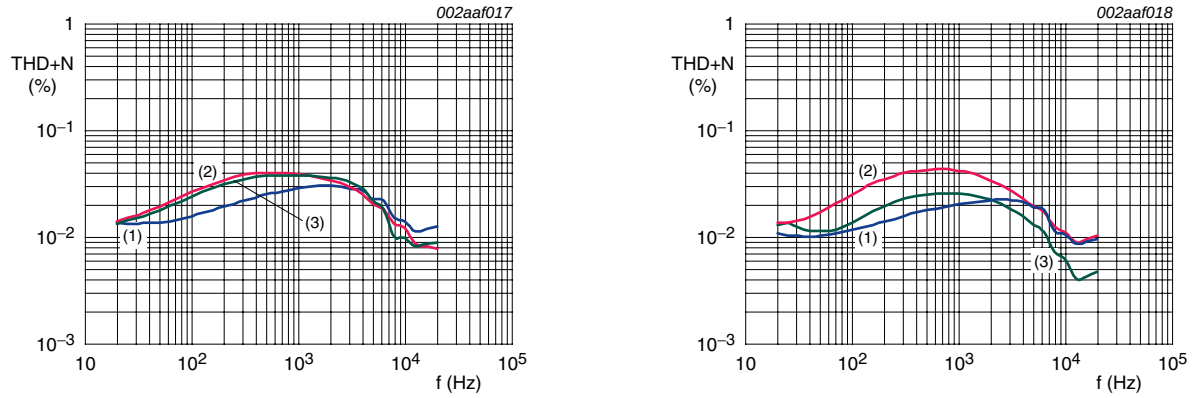
b. R_L = 32 Ω

(1) P_o = 1 mW / channel

(2) P_o = 10 mW / channel

(3) P_o = 15 mW / channel

Fig 21. Total harmonic distortion-plus-noise versus frequency (V_{DD} = 3.6 V)



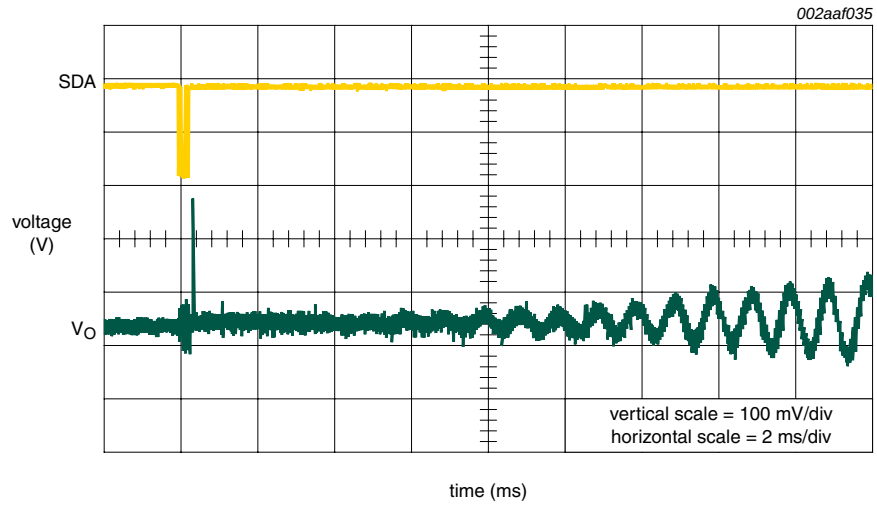
(1) P_o = 1 mW / channel
(2) P_o = 10 mW / channel
(3) P_o = 15 mW / channel

a. R_L = 16 Ω

(1) P_o = 1 mW / channel
(2) P_o = 10 mW / channel
(3) P_o = 20 mW / channel

b. R_L = 32 Ω

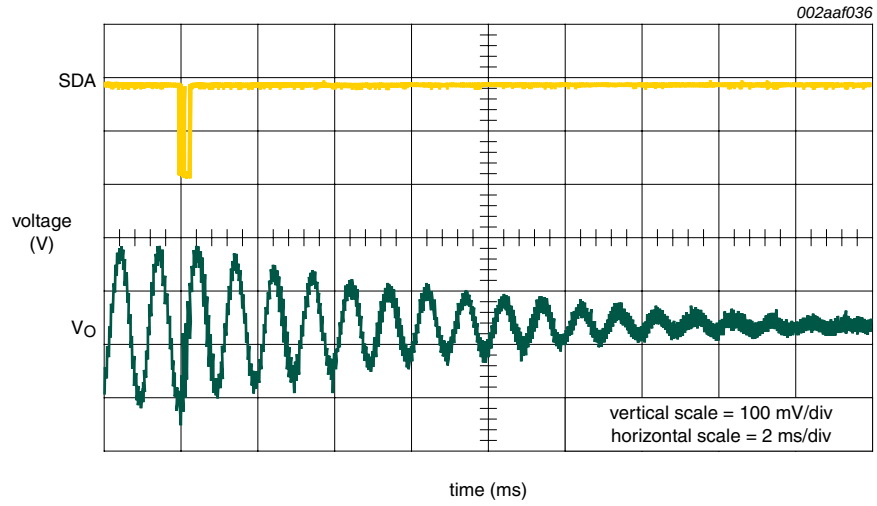
Fig 22. Total harmonic distortion-plus-noise versus frequency (V_{DD} = 5 V)



R_L = 32 Ω; f = 1 kHz; $V_{i(p-p)}$ = 200 mV.

Based on single channel 1 demo board only.

Fig 23. Start-up waveform



R_L = 32 Ω; f = 1 kHz; $V_{i(p-p)}$ = 200 mV; G_v = 4 dB.

Based on single channel 1 demo board only.

Fig 24. Shutdown waveform

Table 13. Dynamic characteristics for I²C-bus

Symbol	Parameter	Conditions	Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	0.6	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	µs
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	µs
$t_{HD;DAT}$	data hold time		0	-	0	-	ns
$t_{VD;ACK}$	data valid acknowledge time	[1]	0.3	3.45	0.1	0.9	µs
$t_{VD;DAT}$	data valid time	[2]	0.3	3.45	0.1	0.9	µs
$t_{SU;DAT}$	data set-up time		250	-	100	-	ns
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	µs
t_f	fall time of both SDA and SCL signals	[3][4]	-	300	$20 + 0.1C_b$ [5]	300	ns
t_r	rise time of both SDA and SCL signals		-	1000	$20 + 0.1C_b$ [5]	300	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter	[6]	-	50	-	50	ns

[1] $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.

[2] $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.

[3] A master device must internally provide a hold time of at least 300 ns for the SDA signal (refer to the V_{IL} of the SCL signal) in order to bridge the undefined region of SCL's falling edge.

[4] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time (t_f) for the SDA output stage is specified at 250 ns. This allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[5] C_b = total capacitance of one bus line in pF.

[6] Input filters on the SDA and SCL inputs suppress noise spikes less than 50 ns.

13. Application information

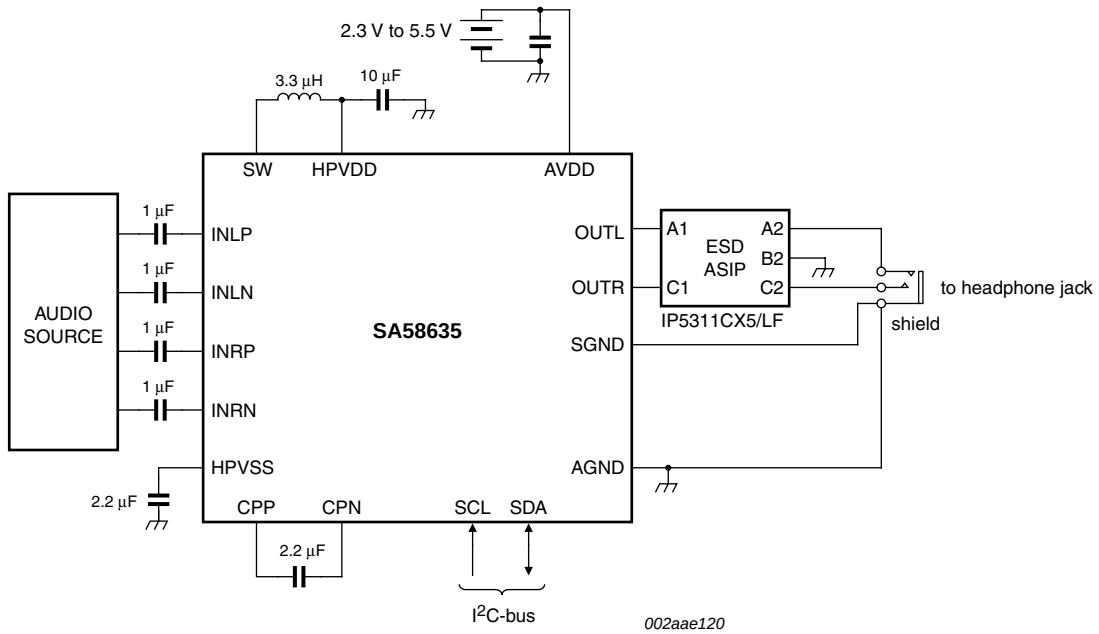


Fig 25. Typical application

13.1 Power supply decoupling considerations

The SA58635 is a stereo class-G headphone driver amplifier that requires proper power supply decoupling to ensure the rated performance for THD+N and power efficiency. To decouple high frequency transients, power supply spikes and digital noise on the power bus line, a low Equivalent Series Resistance (ESR) capacitor, of typically 1 µF is placed as close as possible to the AVDD terminals of the device. It is important to place the decoupling capacitor at the power pins of the device because any resistance or inductance in the PCB trace between the device and the capacitor can cause a loss in efficiency. 10 µF or greater capacitors are usually not required due to high PSRR of the SA58635.

13.2 Input capacitor selection

The SA58635 does not require input coupling capacitors when used with a differential audio source that is biased from −1.3 V to +1.3 V. In other words, the input signal must be biased within the common-mode input voltage range. If high-pass filtering is required or if it is driven using a single-ended source, input coupling capacitors are required.

The 3 dB cut-off frequency is created by the input coupling capacitors and the input resistance of the SA58635. C_i is the value of the input coupling capacitors. The input resistance (R_i) of the SA58635 is a function of amplifier gain; it will vary from approximately 11.06 kΩ (minimum) to 28.47 kΩ (maximum) (see Table 14).

Table 14. Input resistance as a function of amplifier gain

Steps	R_i (kΩ)	Gain (dB)
0	28.468	−58.986
1	28.450	−55.185
2	28.421	−51.083
3	28.375	−47.117
4	28.298	−42.942
5	28.177	−38.819
6	27.995	−34.884
7	27.697	−30.758
8	27.302	−27.155
9	26.982	−24.997
10	26.587	−22.858
11	26.163	−20.981
12	25.550	−18.751
13	24.910	−16.826
14	24.183	−14.967
15	23.264	−12.953
16	22.173	−10.893
17	21.560	−9.846
18	20.947	−8.861
19	20.334	−7.925
20	19.607	−6.868
21	18.880	−5.857
22	18.267	−5.034
23	17.420	−3.930
24	16.572	−2.857
25	15.725	−1.804
26	14.998	−0.913
27	14.207	0.052
28	13.480	0.939
29	12.754	1.831
30	11.906	2.884
31	11.058	3.958

The 3 dB cut-off frequency is calculated by Equation 1:

$$f_{-3dB} = \frac{1}{2\pi \times R_i \times C_i} \quad (1)$$

Since the values of the input coupling capacitor and the input resistor affects the low frequency performance of the audio amplifier, it is important to consider in the system design.

For a required 3 dB cut-off frequency, Equation 2 is used to determine C_i:

$$C_i = \frac{1}{2\pi \times R_i \times f_{-3dB}} \quad (2)$$

For C_i = 1 μF, the 3 dB cut-off frequency will vary with gain settings. For gain setting of 4 dB, the SA58635 input resistance, R_i is 11.06 kΩ (refer to Table 14). Substituting R_i and C_i in Equation 1 yields f_{-3dB} = 14.4 Hz.

13.3 PCB layout considerations

Component location is very important for performance of the SA58635. Place all external components very close to the device. Placing decoupling capacitors directly at the power supply pins increases efficiency because the resistance and inductance in the trace between the device power supply pins and the decoupling capacitor causes a loss in power efficiency.

The trace width and routing are also very important for power output and noise considerations.

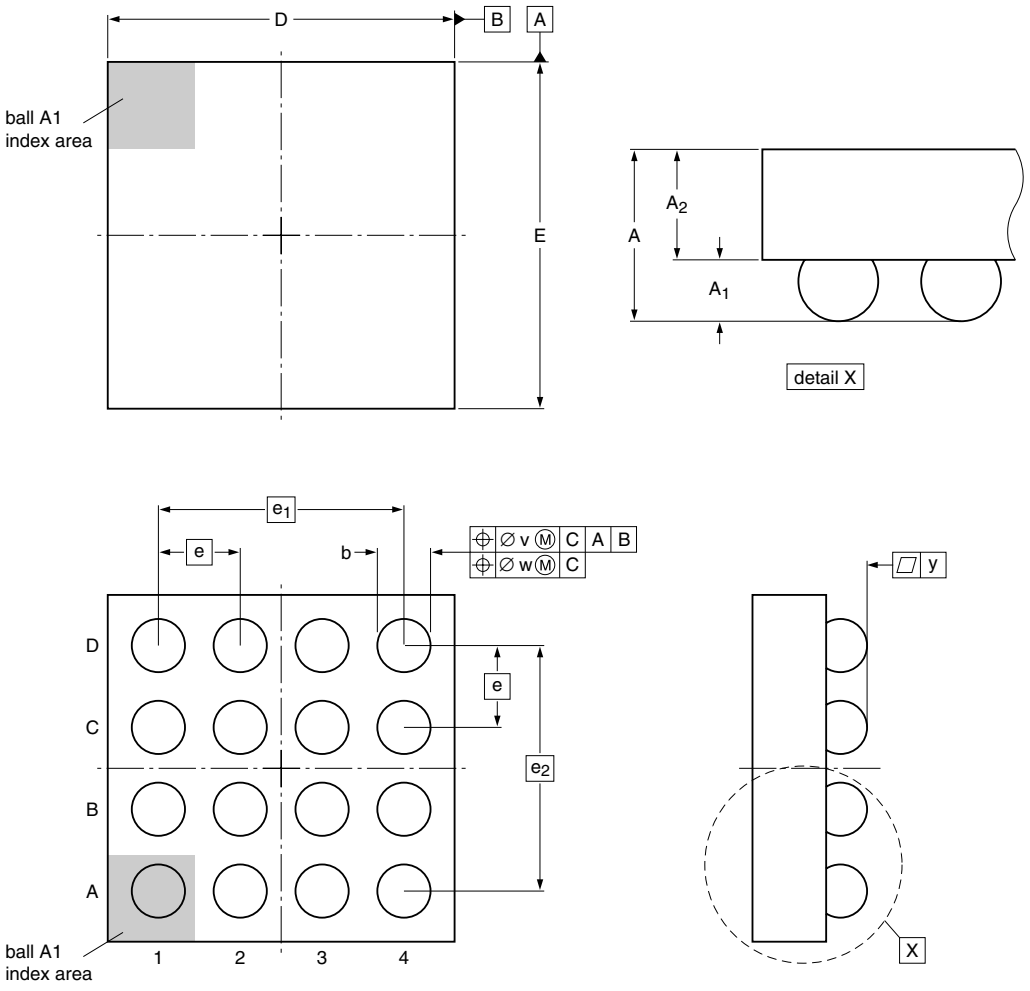
For the input pins (INLP, INLN, INRP, INRN), the traces must be symmetrical and run side-by-side to maximize common-mode cancellation.

13.4 Thermal information

The SA58635 16-bump WLCSP package ground bumps are soldered directly to the PCB heat spreader. The heat spreader is the PCB ground plane or special heat sinking layer designed into the PCB. The thickness and area of the heat spreader may be maximized to optimize heat transfer and achieve lower package thermal resistance.

14. Package outline

WLCSP16: wafer level chip-size package; 16 balls; 1.7 x 1.7 x 0.56 mm **SA58635UK**



Dimensions

Unit	A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
max	0.615	0.23	0.385	0.29	1.725	1.725						
mm nom	0.560	0.20	0.360	0.26	1.695	1.695	0.4	1.2	1.2	0.02	0.01	0.03
min	0.505	0.17	0.335	0.23	1.665	1.665						

sa58635uk_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SA58635UK						~~10-01-18~~ 10-01-19

Fig 26. Package outline SA58635UK (WLCSP16)

15. Soldering of WLCSP packages

15.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note *AN10439 "Wafer Level Chip Scale Package"* and in application note *AN10365 "Surface mount reflow soldering description"*.

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

15.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

15.3 Reflow soldering

Key characteristics in reflow soldering are:

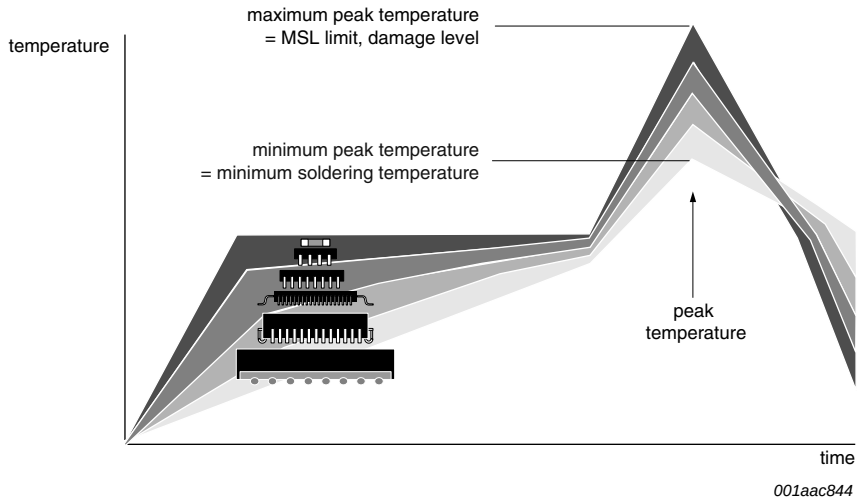
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 27) than a PbSn process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 15.

Table 15. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 27.



MSL: Moisture Sensitivity Level

Fig 27. Temperature profiles for large and small components

For further information on temperature profiles, refer to application note *AN10365 "Surface mount reflow soldering description"*.

15.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

15.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

15.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note *AN10365 "Surface mount reflow soldering description"*.

15.3.4 Cleaning

Cleaning can be done after reflow soldering.

16. Abbreviations

Table 16. Abbreviations

Acronym	Description
ASIP	Application Specific Instruction-set Processor
DVD	Digital Versatile Disk
ESD	ElectroStatic Discharge
ESR	Equivalent Series Resistance
FB	FeedBack
HP	HeadPhone
I^2C-bus	Inter-integrated Circuit bus
PC	Personal Computer
PCB	Printed-Circuit Board

17. Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SA58635_1	20100326	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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20. Contents

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