GigaBit Logic **10G046**

T-68-21-51

Quad 4:1 or Dual 8:1 Data Multiplexer
1.5 GHz /600 ps Propagation Delay
10G PicoLogic™ Family

FEATURES

- Dual 8:1 or quad 4:1 configurations controlled by Mode input
- Data paths controlled by 3 common select lines
- Common output enable control
- 150 ps typical output rise, fall times
- ECL and PicoLogic compatible I/O
- Temperature and voltage compensated using VBB threshold reference input
- On-chip VBBS reference voltage supply supply
- Output wire - OR capability for expansion to 16:1 MUX
- Available in C - leaded or leadless chip carrier or die form

APPLICATIONS

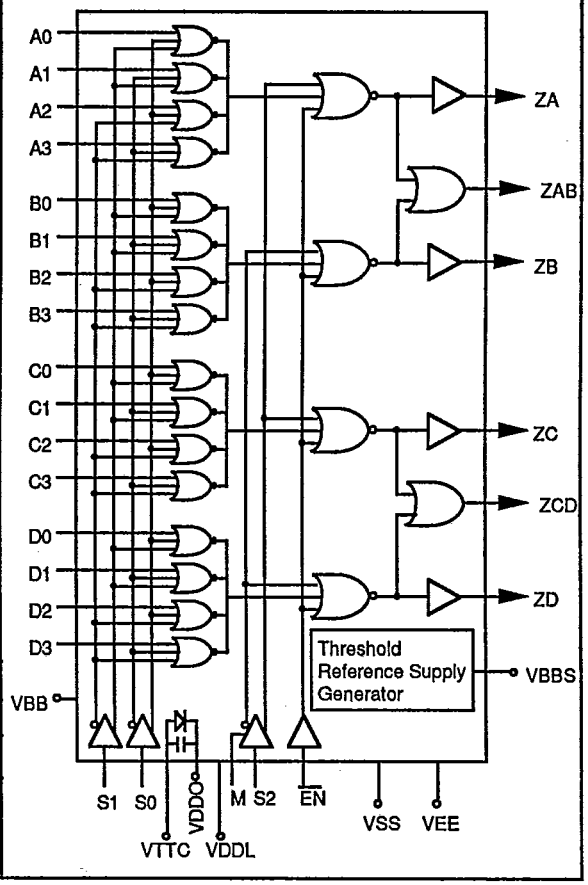
- High speed test equipment
- General purpose multiplexing
- High speed word generation

FUNCTIONAL DESCRIPTION

The 10G046 is a high speed dual 8:1 or quad 4:1 data multiplexer with three common select lines and a common output enable. A dc mode control (M), strapable to VDDL or VSS, is provided to select between 8:1 or 4:1 operating modes. The 10G046 has16 data inputs, A0...A3, B0...B3, C0...C3 and D0...D3. When M is high (=VDDL), S0 and S1 provide a common 4:1 data selection to ZA, ZB, ZC and ZD. When M is low (=VSS), S0, S1 and S2 are used to provide a common 8:1 data selection to the ZAB and ZCD outputs. A common enable ($\overline{EN}$) enables all outputs when low. Note that M must be strapped to VDDL or VSS and not driven by logic.

The 10G046 is designed to provide general purpose logical multiplexing for bus structures, data and address multiplexing and fan-in of data channels or interrupt signals. Two devices can be easily interconnected to form a dual 16:1 MUX by wire-OR tying their respective 8:1 outputs and driving the $\overline{EN}$ inputs with an S3 select line (see drawing pg. 2). The 10G046 is a member of GigaBit's PicoLogic family of GaAs digital integrated circuits, and is fabricated using GigaBit's high volume GaAs MESFET process technology.

LOGIC DIAGRAM



10G046 ORDERING INFORMATION

PACKAGE TYPE	SPEED (Min. 0°C to 85°C)	
	1.5 GHz	1.25 GHz
C-Leaded CC Leadless CC Dice	10G046-2C 10G046-2L	10G046-3C 10G046-3L 10G046-3X

GBL GigaBit Logic

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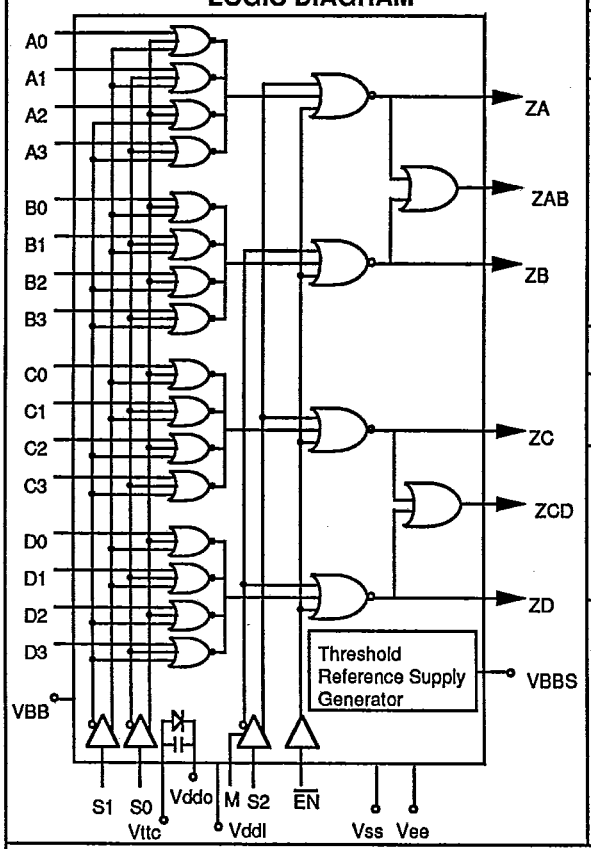
LOGIC DIAGRAM



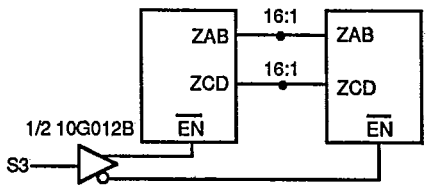
Truth Table 2 X 8:1

Mode M	Enable $\overline{EN}$	Select Inputs S0	S1	S2	Outputs ZAB	ZCD
L	L	L	L	L	A0	C0
L	L	H	L	L	A1	C1
L	L	L	H	L	A2	C2
L	L	H	H	L	A3	C3
L	L	L	L	H	B0	D0
L	L	H	L	H	B1	D1
L	L	L	H	H	B2	D2
L	L	H	H	H	B3	D3
X	H	X	X	X	L	L

Truth Table 4 X 4:1

Mode M	Enable $\overline{EN}$	Select Inputs S0	S1	S2	Outputs ZA	ZB	ZC	ZD
H	L	L	L	X	A0	B0	C0	D0
H	L	H	L	X	A1	B1	C1	D1
H	L	L	H	X	A2	B2	C2	D2
H	L	H	H	X	A3	B3	C3	D3
X	H	X	X	X	L	L	L	L

DUAL 16:1 MUX



PIN DESCRIPTIONS

A0 - A3	Data inputs, A group
B0 - B3	Data inputs, B group
C1 - C3	Data inputs, C group
D0 - D3	Data inputs, D group
S0, S1, S2	Data select inputs
M	Mode control input (selects 8:1 or 4:1 operating mode; tie to Vddl or Vss)
$\overline{EN}$	Active low output enable control (GaAs level compatible only)
ZA	4:1 output of group A inputs
ZAB	8:1 output of group A and B inputs
ZB	4:1 output of group B inputs
ZC	4:1 output of group C inputs
ZCD	8:1 output of group C and D inputs
ZD	4:1 output of group D inputs
VDDO	Output driver ground pin
VDDL	Internal logic ground pin
VSS	-3.4 volt power supply
VEE	- 5.2 volt power supply
VTTC	AC return lead for the package internal VDDO decoupling capacitor. Typically connect to VTT.
VBB	Threshold reference level input. Provides temperature and voltage compensation of the input threshold. Connect to VBBS when driving from PicoLogic. When driving from ECL or other GaAs families, connect to that families' threshold voltage. This pin may not be left unconnected.
VBBS	PicoLogic threshold reference voltage output. Connect to VBB when interfacing to PicoLogic.

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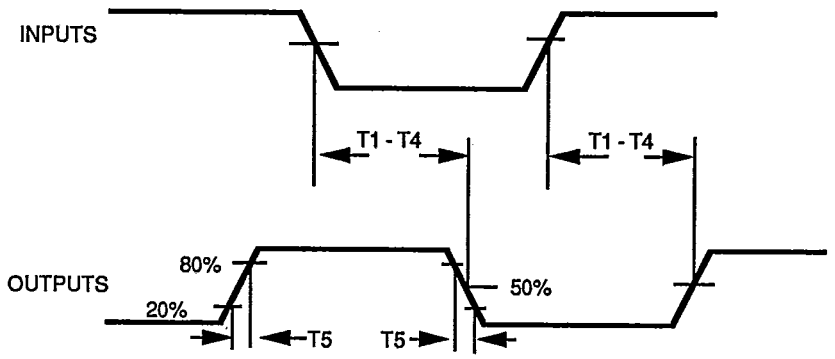
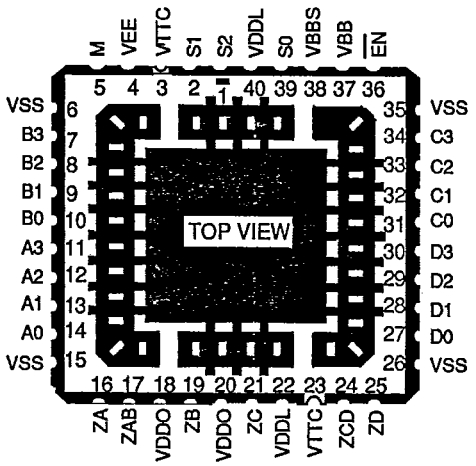
SWITCHING WAVEFORMS



PIN FUNCTIONS - PACKAGE TYPES "L" AND "C"



NOTES:
Pin 1 is marked for orientation. N/C = no connection.

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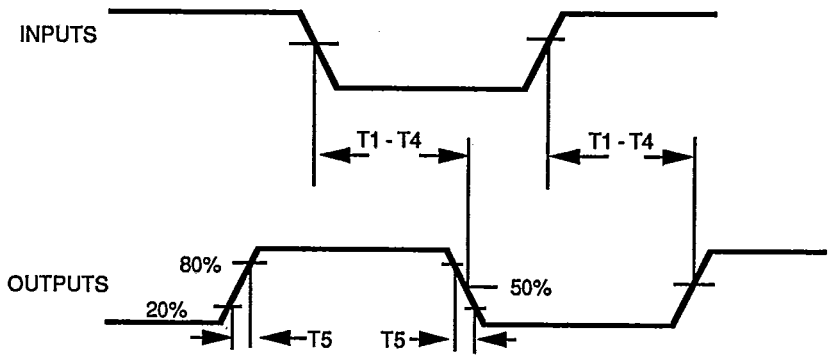
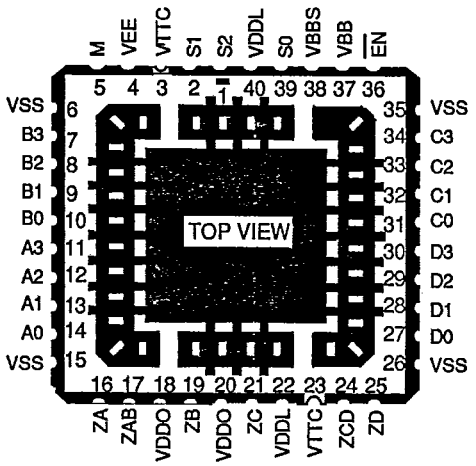
SWITCHING WAVEFORMS



PIN FUNCTIONS - PACKAGE TYPES "L" AND "C"



NOTES:
Pin 1 is marked for orientation. N/C = no connection.

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24 PIN HYBRID 18 PIN PACKAGE

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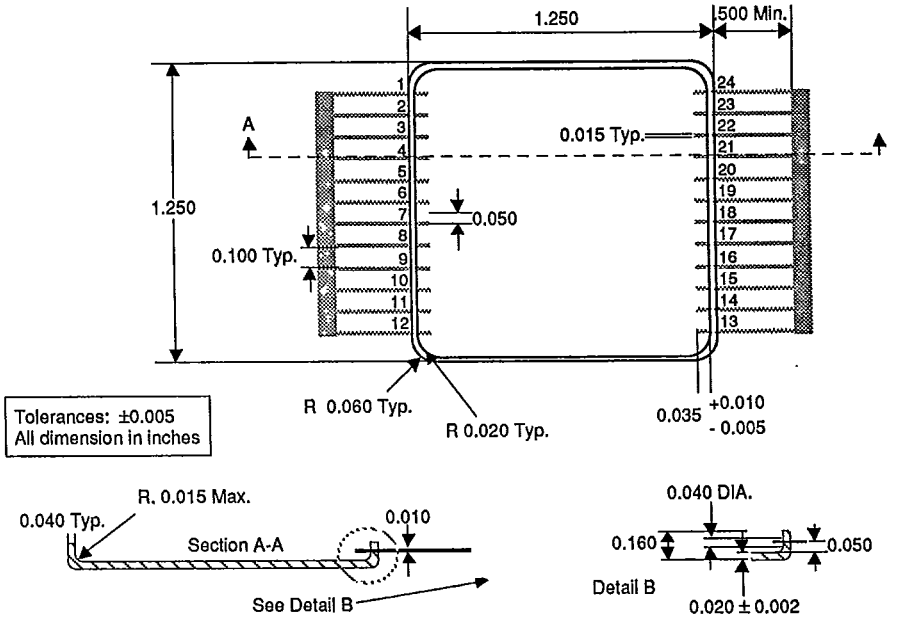
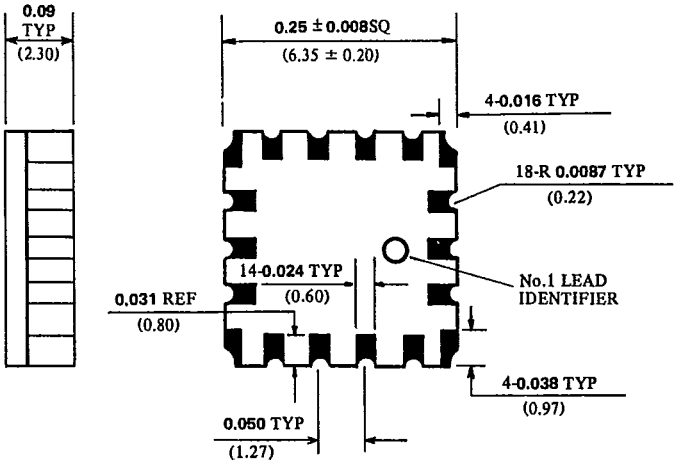
24 PIN HYBRID PACKAGE

Type H



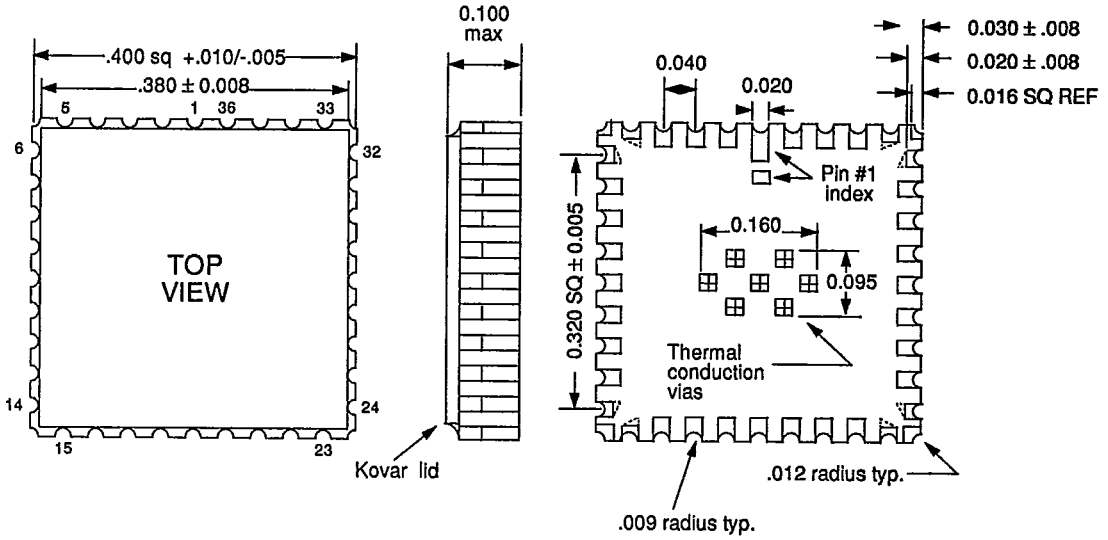
18 PIN LEADLESS CHIP CARRIER

TYPE L1



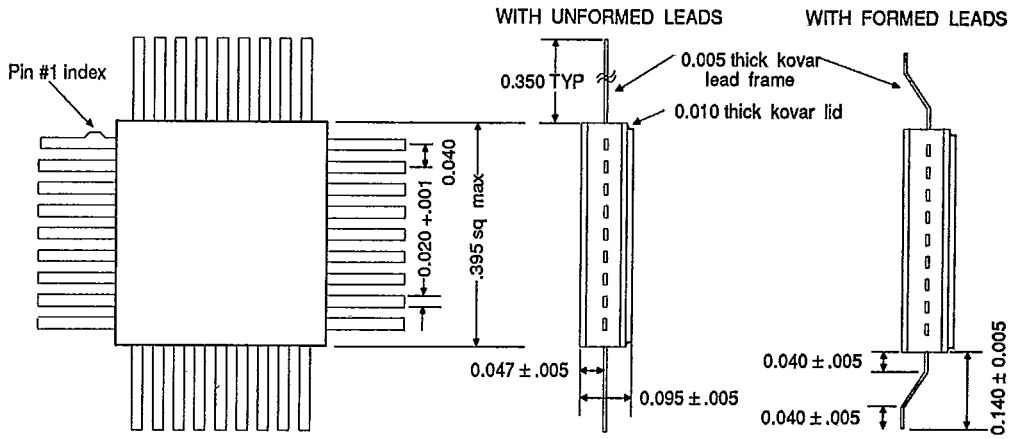
All dimensions shown in **inches** and (millimeters)

36 PIN LEADLESS CHIP CARRIER
TYPE L36



NOTES:
1) The package bottom thermal vias, top lid surface and 4 metallized corner castellations (when present) are all at Vss potential.
2) All dimensions in inches.
3) Pin #1 identifier may be an elongated pad or small, square gray marker.

36 I/O LEAD FLATPACK
TYPE F



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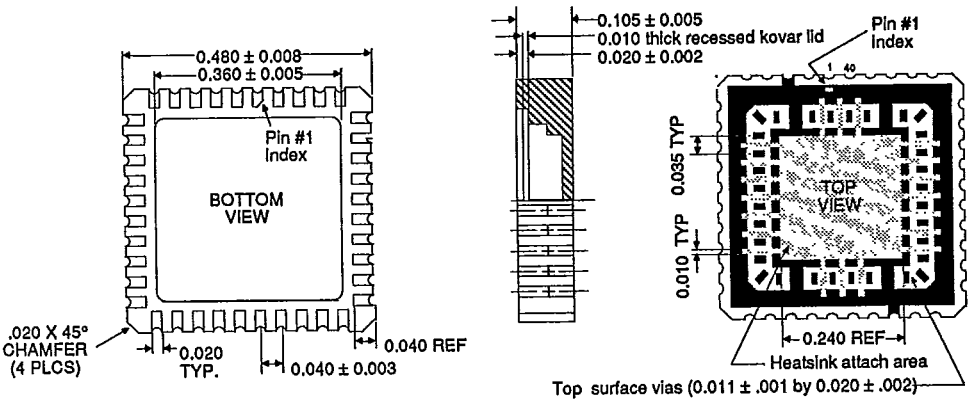
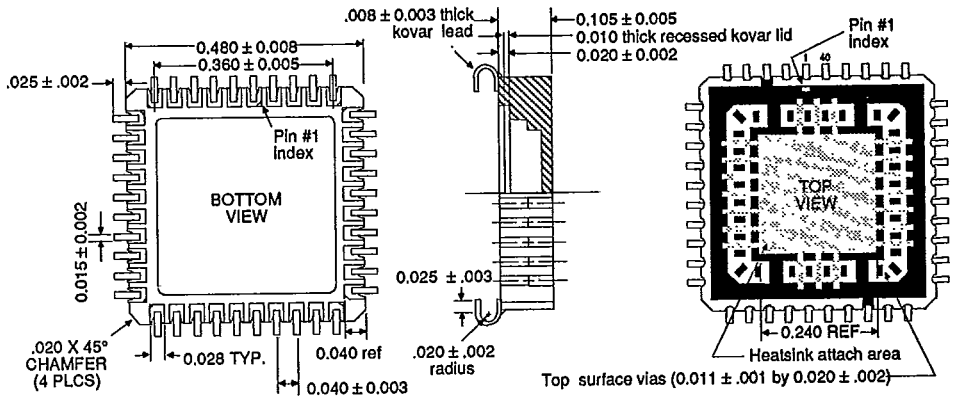
40 PIN PACKAGES

40 PIN LEADLESS CHIP CARRIER
TYPE L



40 PIN LEADED CHIP CARRIER
TYPE C

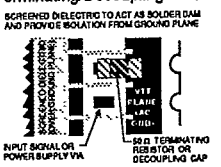


NOTES:

(1) Footprint is JEDEC standard outline.
(2) Top surface vias (for terminating resistors and decoupling capacitors) are not available on pins 3,4,17, 18, 23,24,37 and 38.
(3) Top surface metal (not including vias) and pins 3 and 23 are fixed at VTT potential.
(4) Recommended top surface chip resistors are0.040 long by 0.020 wide by 0.010 thick typ, 100 mw min. nominal power rating (Mini-Systems MSR-21 or equivalent.)
(5) Recommended top surface chip capacitors are 0.040 long by 0.030 wide by 0.020 thick typ, 25V VDCW, 1000 pf, min. (Johanson R09 case or equivalent).
(6) Recommended heatsinks are GBL P/Ns 90GHS-40-A and 90GHS-40-B.
(7) Thermally conductive, electrically non-conductive epoxy is recommended for heatsink attachment (Ablestick 789-4 or 561K, or Thermalloy Thermalbond™ or equivalent.)
(8) L40 and C40 packages are dimensionally identical except for contact finger width.

TOP SURFACE LEGEND:
Metalized Ceramic.....
Screened Dielectric.....
Bare Ceramic.....

Top Surface Terminating/Decoupling Detail



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68 & 132 PIN PACKAGES

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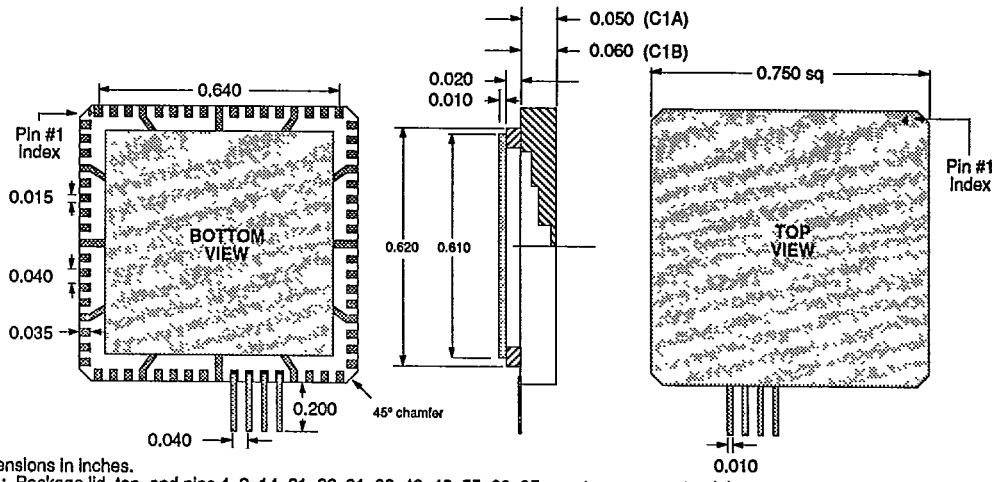
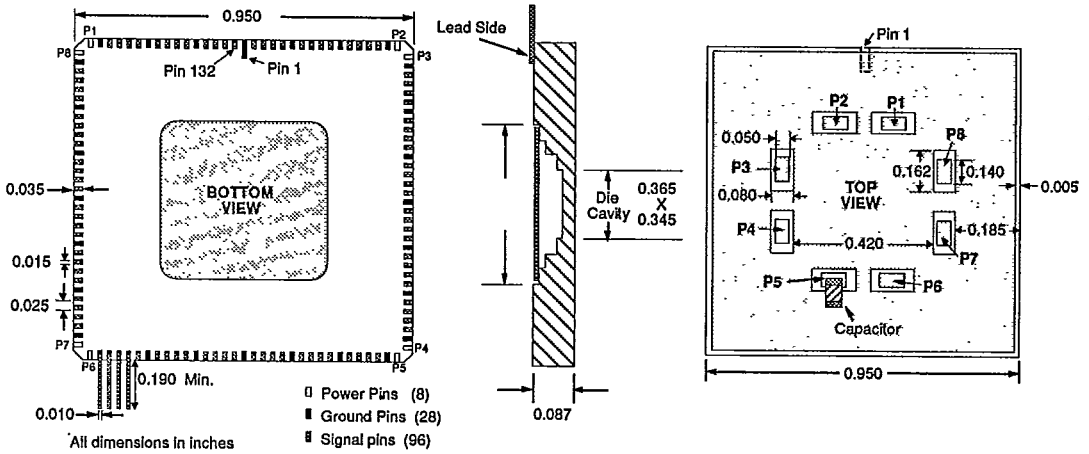
68 PIN LEADED CHIP CARRIER
TYPE C1



(1) All dimensions in inches.
(2) a. C1A: Package lid, top, and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
b. C1B: Package lid and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).

132 PIN LEADED CHIP CARRIER
TYPE C3



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