REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Added devices 04-06. Updated drawing with boilerplate paragraphs. Editorial changes throughout. ksr	1997 AUG 25	Raymond Monnin

REV																			
SHEET																			
REV	A	A	A																
SHEET	15	16	17																

REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
97 - 03 - 07

REVISION LEVEL
A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 42316

MICROCIRCUITS, MEMORY, DIGITAL, CMOS, 8K X 9 SRAM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-88683**

SHEET 1 OF 17

DESC FORM 2233
APR 97

5962-E245-97

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN) The complete PIN is as shown in the following example:

5962-88683	01	X	X
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Acess time
01	(See 6.4)	8192 X 9 CMOS static RAM	45 ns
02	(See 6.4)	8192 X 9 CMOS static RAM	35 ns
03	(See 6.4)	8192 X 9 CMOS static RAM	25 ns
04	(See 6.4)	8192 X 9 CMOS static RAM	45 ns
05	(See 6.4)	8192 X 9 CMOS static RAM	35 ns
06	(See 6.4)	8192 X 9 CMOS static RAM	25 ns

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
U	CQCC3-N28	28	rectangular chip carrier package
X	GDIP1-T28 or CDIP2-T28	28	dual-in-line package
Y	See figure 1	28	dual-in-line package
Z	GDFP2-F28	28	flat package

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings

Supply voltage to ground potential	-0.5 V dc to +7.0 V dc
DC voltage applied to outputs	-0.5 V dc to +7.0 V dc
DC input voltage	-0.5 V dc to VCC + 0.5 V dc
DC output current	20 mA
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	1.0 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Cases U, X, and Z	See MIL-STD-1835
Case Y	28°C/W 1/
Junction temperature (T_J) 2/	+150°C

1.4 Recommended operating conditions

Supply voltage (V_{CC})	4.5 V dc to 5.5 V dc
High level input voltage (V_{IH})	2.2 V dc to V_{CC} + 0.5 V dc
Low level input voltage (V_{IL}) 3/	-1.0 V dc to +0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ When the thermal resistance for this case is specified in MIL-STD-1835, that value shall supersede the value indicated herein.
2/ Maximum junction temperature may be increased to +175°C during burn-in and steady state life.
3/ V_{IL} (min) for short pulse durations of 20 ns or less.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 and figure 1 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection only. Each coated microcircuit inspection lot (see inspection lot as defined in MIL-PRF-38535) shall be subjected to and pass the internal moisture content test at 5000 ppm (see method 1018 of MIL-STD-883). The frequency of the internal water vapor testing shall not be decreased unless approved by the preparing activity for class M. The TRB will ascertain the requirements as provided by MIL-PRF-38535 for classes Q and V. Samples may be pulled any time after seal.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_I and C_O measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. Sample size is fifteen devices, all input and output terminals tested and no failures.

d. Subgroups 7 and 8 shall include verification of the truth table.

TABLE I. Electrical performance characteristics

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -4.0 mA, V_{IL} = 0.8 V, V_{IH} = 2.2 V	1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8 mA, V_{IL} = 0.8 V, V_{IH} = 2.2 V		All		0.4	V
Input load current	I_I	$0\ V \le V_{IN} \le 5.5\ V$		All	-10	+10	µA
Output current, high impedance	I_{OZ}	$GND \le V_{OUT} \le V_{CC}$, output disabled		All	-10	+10	µA
Operating supply current	I_{CC1}	V_{CC} = 5.5 V, I_O = 0 mA, f = 1/ t_{AVAV}, $\overline{CE}_1 = V_{IL}$		01, 02		120	mA
				03 - 06		130	
Standby supply current, TTL level inputs	I_{CC2}	$\overline{CE}_1 > V_{IH}$, V_{CC} = 5.5 V, f = 0 Mhz, all other inputs $\le V_{IL}$ or $> V_{IH}$		All		10	mA
Standby supply current, CMOS level inputs	I_{CC3}	$\overline{CE}_1 = V_{CC} \pm 0.3\ V$, V_{CC} = 5.5 V, f = 0 Mhz, all other inputs $\le 0.3\ V$ or $> V_{CC} + 0.3\ V$		01-03		0.9	mA
				04-06		5	
V_{CC} for data retention	VDR	$\overline{CE}_1 > V_{CC} - 0.2\ V$, VIN > VCC -0.2 V or $\le +0.2\ V$		All	2.0		V
Data retention current	I_{CCDR1}	V_{CC} = 2.0 V		01-03		100	µA
				04-06		300	
	I_{CCDR2}	V_{CC} = 3.0 V		01-03		200	
				04-06		500	
Input leakage current (data retention mode) 3/	I_{LI}			01-03		1.0	µA
				04-06		2.0	
Input capacitance	C_I	V_{CC} = 5.0 V, T_A = +25°C, f = 1 Mhz, see 4.3.1c; V_{IN} = 0V	4	All		8	pF
Output capacitance	C_O	V_{OUT} = 0V	4	All		10	pF
Functional tests		See 4.3.1d	7, 8A, 8B	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device Types	Limits		Unit
					Min	Max	
Read cycle time	t_{AVAV}	See figures 4 and 5 1/	9, 10, 11	01, 04	45		ns
				02, 05	35		
				03, 06	25		
Address valid to data valid	t_{AVQV}			01, 04		45	
				02, 05		35	
				03, 06		25	
Output hold from address change	t_{AVQX}			All	3.0		
Chip enable access time	t_{ELQV}			01, 04		45	
				02, 05		35	
				03, 06		25	
Chip enable to output in low Z	t_{ELQX}	See figures 4 and 5 2/ 3/		01, 04	3.0		
				02, 03, 05, 06	0		
Chip disable to output in high Z	t_{EHQZ}			01, 04		20	
				02, 03, 05, 06		15	
Output enable low to data valid	t_{OLQV}	See figures 4 and 5 1/		01, 02, 04,05		20	
				03, 06		15	
Output enable low to low Z	t_{OLQX}	See figures 4 and 5 2/ 3/		All	0		
Output enable high to high Z	t_{OHQZ}			01,04		20	
				02, 05		15	
				03, 06		10	
Write cycle time	t_{AVAV}	See figures 4 and 6 1/		01, 04	45		
				02, 05	35		
				03, 06	25		
Chip enable time to end of write	t_{ELWH}			01, 04	40		
				02, 05	30		
				03, 06	20		

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

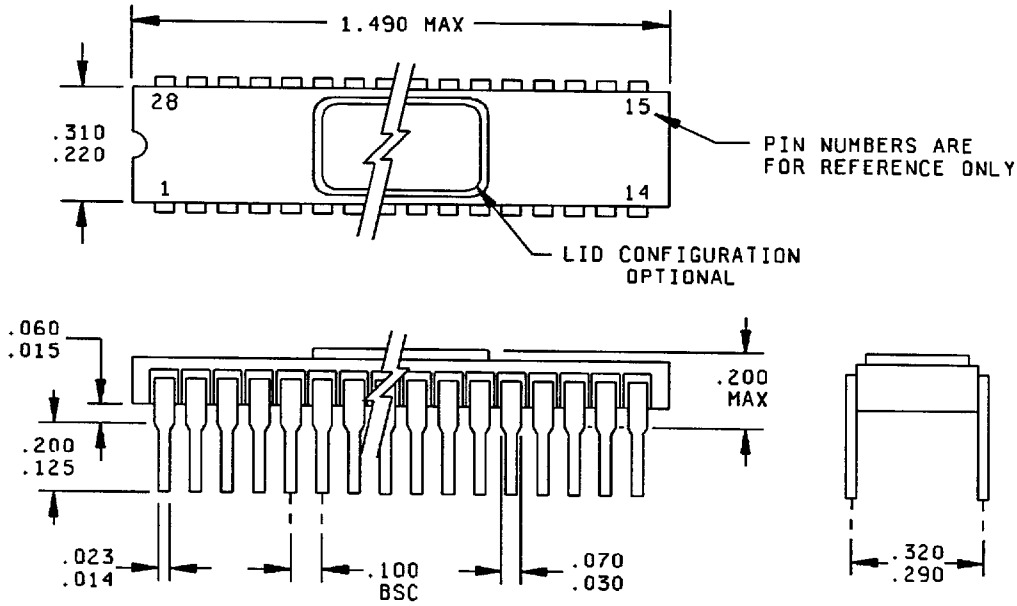
Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device Types	Limits		Unit
					Min	Max	
Address set-up to write end	t_{AVWH}	See figures 4 and 6 1/	9, 10, 11	01, 04	40		ns
				02, 05	30		
				03, 06	25		
Address hold from write end	t_{WHAV}			All	5		
Address set-up to write start	t_{AVWL}			All	5		
Write enable pulse width	t_{WLWH}			01, 04	25		
				02, 05	20		
				03, 06	15		
Data set-up to write end	t_{DVWH}			01, 04	20		
				02, 05	15		
				03, 06	10		
Data hold from write end	t_{WHDX}			All	5		
Write enable to output in high Z	t_{WLQZ}	See figures 4 and 6 2/ 3/		01, 04		20	
				02, 05		15	
				03, 06		10	
Output active from end of write	t_{WHQX}			01, 04	3.0		
				02, 03, 05, 06	0		
Operation recovery time	t_R	$\overline{CE}_1 > VCC - 0.2\ V$, $VIN > VCC - 0.2\ V$ or $< +0.2\ V$, See figure 7 3/		All	t_{RC} 4/		

1/ Test conditions assume signal transition times of 5.0 ns or less. Timing is referenced at input and output levels of 1.5 V. Output loading is equivalent to the specified I_{OL}/I_{OH} with a load capacitance of 30 pF (see figure 4).

2/ Test conditions assume signal transition times of 5.0 ns or less. Transition is measured at steady state high level of -500 mV or steady state low level of +500 mV on the output from 1.5 V level on the input with a load capacitance of 5.0 pF (see figure 4).

3/ May not be tested, but shall be guaranteed to the limits specified in table I.

4/ t_{RC} = read cycle time.



Inches	mm	Inches	mm
1.490	37.85	.100	2.54
.320	8.13	.070	1.78
.310	7.87	.060	1.52
.290	7.37	.030	0.76
.220	5.59	.023	0.58
.200	5.08	.015	0.38
.125	3.18	.014	0.36

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.

FIGURE 1. Case outline Y.

DEVICE TYPE	ALL
CASE OUTLINE	X, Y, Z, AND U
TERMINAL NUMBER	TERMINAL SYMBOL
1	A
2	A
3	A
4	A
5	A
6	A
7	A
8	A
9	A
10	I/O_1
11	I/O_2
12	I/O_3
13	I/O_4
14	GND
15	I/O_5
16	I/O_6
17	I/O_7
18	I/O_8
19	I/O_9
20	$\overline{CE}_1$
21	A
22	$\overline{OE}$
23	A
24	A
25	A
26	CE_2
27	$\overline{WE}$
28	V_{CC}

FIGURE 2. Terminal connections.

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	MODE	I/O
H	X	X	X	Not selected	High Z
X	L	X	X	Not selected	High Z
L	H	H	H	D_{OUT} disabled	High Z
L	H	L	H	Read	D_{OUT}
L	H	X	L	Write	D_{IN}

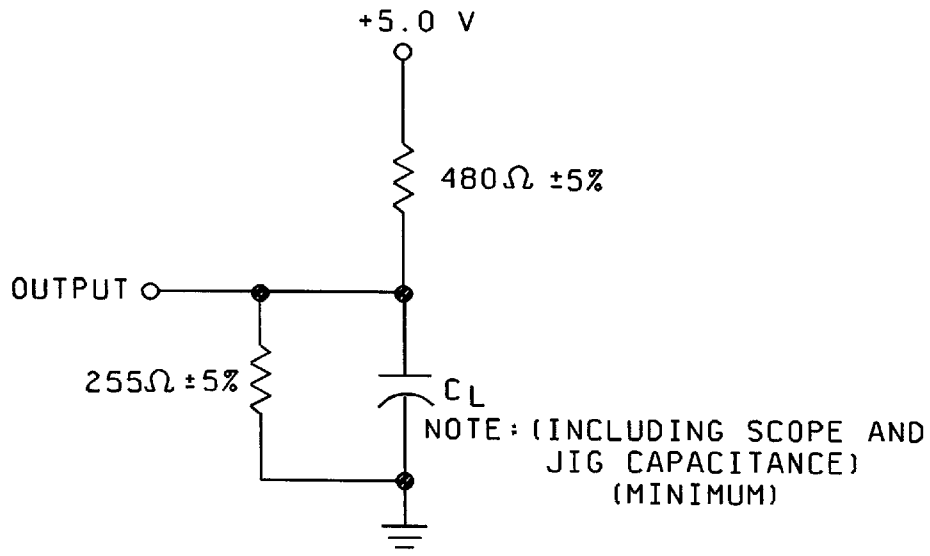
H = Logic 1 state

L = Logic 0 state

X = Don't care

HIGH Z = High impedance state

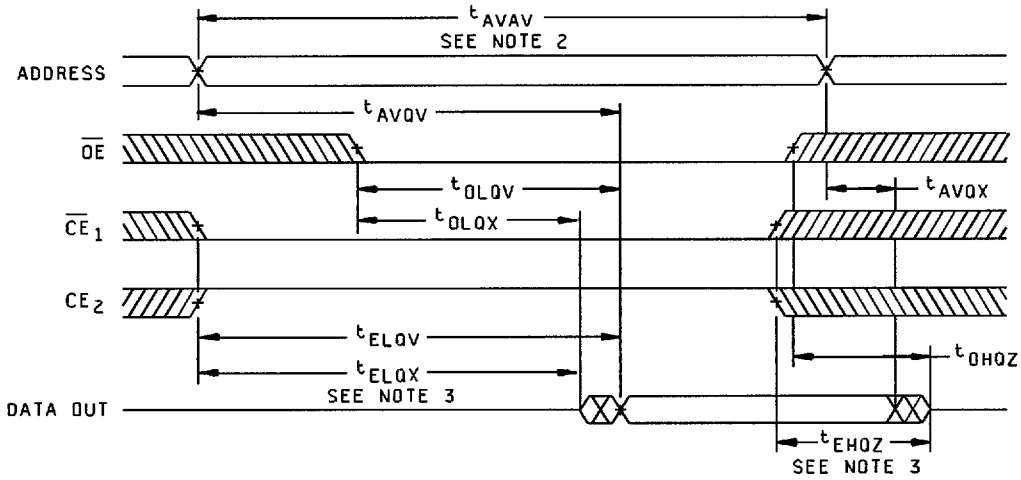
FIGURE 3. Truth table.



Measurement	C_L
t_{EHQZ}, t_{ELQX}, t_{WLQZ}, and t_{WHQX}	C_L = 5.0 pF
All others	C_L = 30 pF

FIGURE 4. Output load circuit.

READ CYCLE NUMBER 1 - $\overline{OE}$ CONTROLLED
SEE NOTE 1



READ CYCLE NUMBER 2 - ADDRESS CONTROLLED
SEE NOTES 1 AND 4

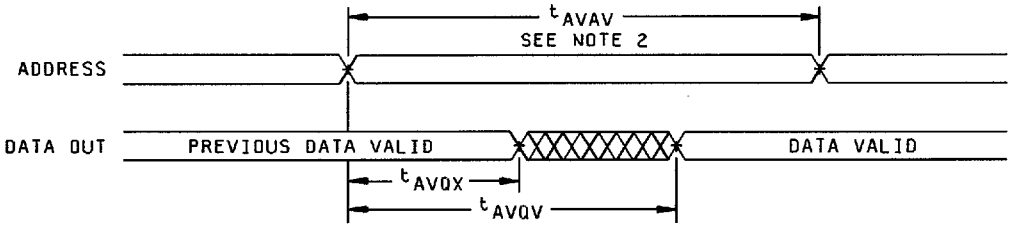
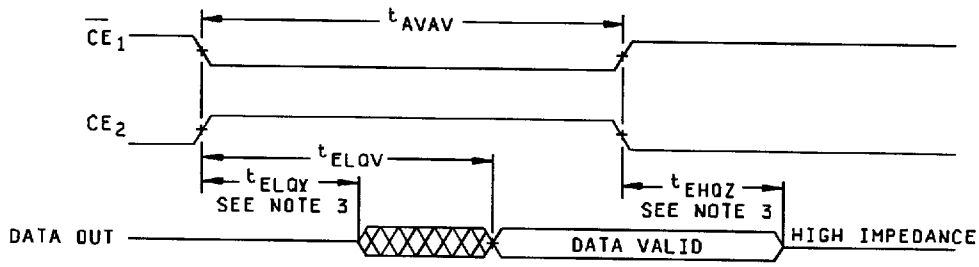


FIGURE 5. Read cycle timing diagrams

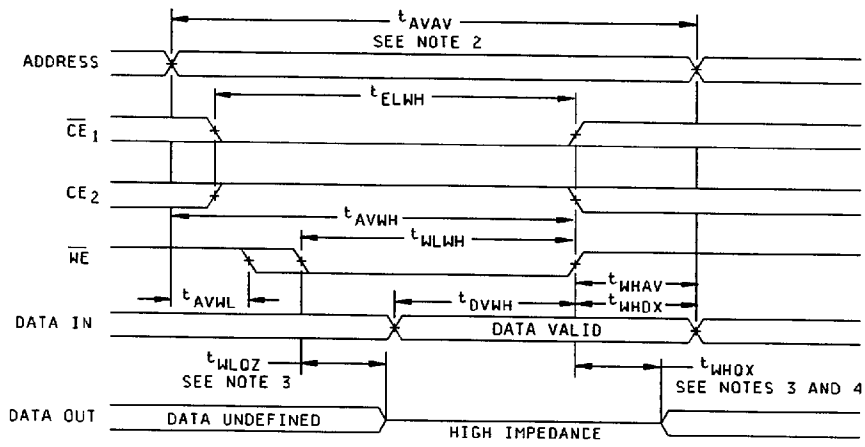
READ CYCLE NUMBER 3 - $\overline{CE}_1$,CE_2 CONTROLLED
SEE NOTES 1, 5, AND 6



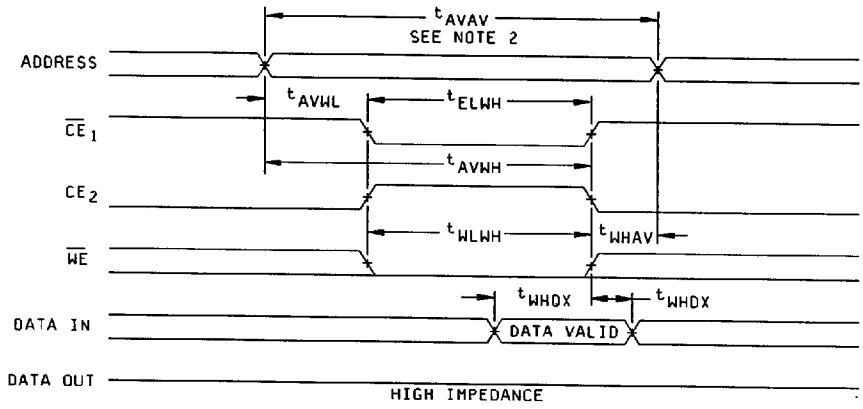
NOTES:
1. $\overline{WE}$ is high for READ cycle.
2. Read cycle time is measured from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady state voltage prior to change.
4. $\overline{CE}_1$ is low, CE_2 is high and $\overline{OE}$ is low for READ cycle.
5. ADDRESS must be valid prior to, or coincident with, $\overline{CE}_1$ transition low and CE_2 transition high.
6. Transitions caused by a chip enable control have similar delays irrespective of whether $\overline{CE}_1$ or CE_2 causes them.

FIGURE 5. Read cycle timing diagrams - Continued.

WRITE CYCLE NUMBER 1 - $\overline{WE}$ CONTROLLED
SEE NOTE 1



WRITE CYCLE NUMBER 2 - $\overline{CE}_1$,CE_2 CONTROLLED
SEE NOTE 1



NOTES:
1. $\overline{CE}_1$ and $\overline{WE}$ must be low, CE_2 high, for WRITE cycle.
2. WRITE cycle time is measured from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady state voltage prior to change.
4. If $\overline{CE}_1$ goes high, or CE_2 goes low simultaneously with $\overline{WE}$ high, the output remains in low impedance state.
5. $\overline{OE}$ is low for this WRITE cycle to show t_{WLQZ} and t_{WHQX}.

FIGURE 6. Write cycle timing diagrams.

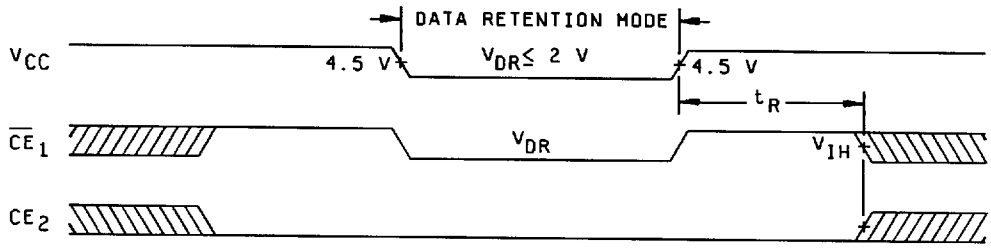


FIGURE 7. Data retention waveform.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4**, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8

* PDA applies to subgroup 1 and 7.
** See 4.3.1c

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 1997 AUG 19

Approved sources of supply for SMD 5962-88683 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 3/
5962-8868301XX	2/	P4C163L-45DWMB
5962-8868301YX	2/	P4C163L-45CMB
5962-8868301ZX	2/	P4C163L-45FMB
5962-8868301UX	2/	P4C163L-45LMB
5962-8868302XX	2/	P4C163L-35DWMB
5962-8868302YX	2/	P4C163L-35CMB
5962-8868302ZX	2/	P4C163L-35FMB
5962-8868302UX	2/	P4C163L-35LMB
5962-8868303XX	2/	P4C163L-25DWMB
5962-8868303YX	2/	P4C163L-25CMB
5962-8868303ZX	2/	P4C163L-25FMB
5962-8868303UX	2/	P4C163L-25LMB
5962-8868304XX	75569	P4C163L-45DWMB
5962-8868304YX	75569	P4C163L-45CMB
5962-8868304ZX	75569	P4C163L-45FMB
5962-8868304UX	75569	P4C163L-45LMB

See notes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 3/
5962-8868305XX	75569	P4C163L-35DWMB
5962-8868305YX	75569	P4C163L-35CMB
5962-8868305ZX	75569	P4C163L-35FMB
5962-8868305UX	75569	P4C163L-35LMB
5962-8868306XX	75569	P4C163L-25DWMB
5962-8868306YX	75569	P4C163L-25CMB
5962-8868306ZX	75569	P4C163L-25FMB
5962-8868306UX	75569	P4C163L-25LMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. The device manufacturers listed herein are authorized to supply alternate lead finishes "A", "B", or "C" at their discretion. Contact the listed approved source of supply for further information.
2/ Not available from an approved source.
3/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
75569	Performance Semiconductor Corp. 610 East Weddell Drive Sunnyvale, CA 94089

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