

HD100160

Dual Parity Generators/Checker

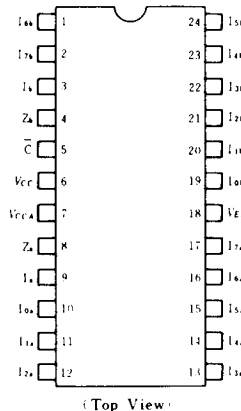
The HD100160 is a Dual Parity Checker/Generator. Each half has nine inputs, with the output being high when an even number of inputs are high. One of the nine inputs (Ia or Ib) has the shorter through-put delay and is therefore preferred as the expansion input for generating parity

for 16 or more bits. The HD100160 also has a Compare ($\bar{C}$) output which allows the circuit to compare two 8-bit words.

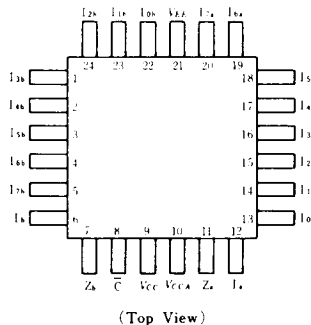
The $\bar{C}$ output is low when the two words match, bit for bit.

PIN ARRANGEMENT

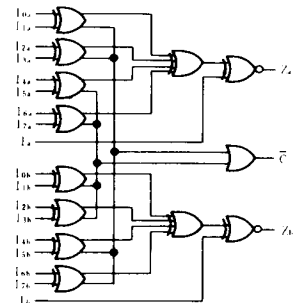
HD100160



HD100160F



LOGIC DIAGRAM



TRUTH TABLE (each half)

Sum of High Input	Output Z
EVEN	H
ODD	L

$$\bar{C} = (I_{a1} \oplus I_{a2}) \oplus (I_{a3} \oplus I_{a4}) \oplus (I_{a5} \oplus I_{a6}) \oplus (I_{a7} \oplus I_{a8}) \oplus (I_{a9} \oplus I_{a10}) \oplus (I_{a11} \oplus I_{a12}) \oplus (I_{a13} \oplus I_{a14}) \oplus (I_{a15} \oplus I_{a16}) \oplus (I_{a17} \oplus I_{a18}) \oplus (I_{a19} \oplus I_{a20}) \oplus (I_{a21} \oplus I_{a22}) \oplus (I_{a23} \oplus I_{a24})$$

DC CHARACTERISTICS ($V_{EE} = -4.2$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$, $T_a = 0$ to $+85^\circ C$)

Item	Symbol	Test Condition	min	typ	max	Unit
Supply Current	I_{EE}	All input open	57	82	115	mA
Input Current	I_{IH}	$V_{IN} = V_{IH\ max}$ Ia, Ib			340	μA
		All input except Ia and Ib			220	μA

Note) As for other items, refer to the "Common DC Characteristics"

■ AC CHARACTERISTICS ($V_{EE} = -2.2$ to -2.8 V, $V_{CC} = V_{CCA} = 2.0$ V)

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Item	Symbol	Test Condition	0℃		25℃			85℃		Unit	
			min	max	min	typ	max	min	max		
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	$I_{a, I_{b}}$ to Z_a, Z_b	1.20	3.50	1.30	2.50	3.60	1.30	3.60	ns
			$I_{a, I_{b}}$ to $\overline{C}$	1.10	2.65	1.20	2.00	2.75	1.20	2.75	
			I_a, I_b to Z_a, Z_b	0.50	1.20	0.60	0.90	1.30	0.60	1.30	
Transition Time	t_{TLH}, t_{THL}			0.40	1.40	0.40	0.90	1.40	0.40	1.40	ns

● HD100160F

Item	Symbol	Test Condition	0℃		25℃			85℃		Unit	
			min	max	min	typ	max	min	max		
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	I_{oa}, I_{ob} to Z_a, Z_b	1.20	3.60	1.30	2.30	3.75	1.30	3.75	ns
			I_{oa}, I_{ob} to $\overline{C}$	1.10	2.80	1.20	1.90	2.90	1.20	2.90	
			I_d, I_b to Z_a, Z_b	0.50	1.20	0.60	0.80	1.30	0.60	1.30	
Transition Time	t_{TLH}, t_{THL}			0.35	1.30	0.35	0.75	1.30	0.35	1.30	ns

Note: The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.