2.5V 200Pin DDR-I SDRAM Small Outline Modules

1GB Module
PC1600, PC2100 & PC2700
Preliminary Data Sheet V0.6, 2003-01-07

- 200-pin Unbuffered 8-Byte Dual-In-Line DDR-I SDRAM non-parity Small Outline Modules
- 128M x 64 organization with two memory banks
- JEDEC standard Double Data Rate Synchronous DRAMs (DDR-I SDRAM)
- Single +2.5V (±0.2V) power supply
- Uses eight 1Gbit DDR-I SDRAM components (2x 64Mb x8) made of stacked 512Mb dies in P-TFBGA package.
- Programmable $\overline{\text{CAS}}$ Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- All inputs and outputs SSTL_2 compatible
- Serial Presence Detect with E^2PROM
- Jedec standard form factor: 67.60mm × 31.75mm × 3.80mm
- Gold plated contacts

Performance

		-6	-7	Unit
	Component Speed Grade	DDR333	DDR266A	
	Module Speed Grade	PC2700	PC2100	
f_{CK}	Clock Frequency (max.) @ CL = 2.5	166	143	MHz
f_{CK}	Clock Frequency (max.) @ CL = 2	133	133	MHz

The HYS64D128020GBDL are industry standard 200-pin 8-byte Small Outline Dual in-line Memory Modules (DIMMs) organized as 128M x 64 in two memory banks. The memory array is designed with Double Data Rate Synchronous DRAMs. A variety of decoupling capacitors are mounted on the PC board. The DIMMs feature serial presence detect based on a serial E^2PROM device using the 2-pin I^2C protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer.

Ordering Information

Type	Compliance Code	Description	SDRAM Technology
HYS64D128020GBDL-6-A	PC2700S-2533-0-Z	1GB SO-DIMM w/ 2 banks	512Mbit Stacked Die in a FBGA
HYS64D128020GBDL-7-A	PC2100S-2033-0-Z		

Note: All part numbers end with a place code, designating the silicon die revision. Reference information available on request. Example: HYS 64D128020GBDL-8-A, indicating Rev.A die is used for DDR-SDRAM components.
The Compliance Code which is printed on the module labels describes the speed sort class ("e.g. PC2100"), the module type ("S"), the latencies (e.g. 2033 means CAS latency = 2.0, RCD latency = 3 and row precharge latency = 3), the JEDEC SPD Revision ("0") and the Raw Card used on this DIMM ("Z").

Pin Definitions and Functions

Pin Name	Pin Function
A0 - A12	Address Inputs
BA0, BA1	Bank Selects
DQ0 - DQ63	Data Input/Output
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Input
CKE0 - CKE1	Clock Enable
DQS0 - DQS8	SDRAM low data strobes
CLK0 - CLK1,	SDRAM clock (positive lines)
$\overline{CLK0}$ - $\overline{CLK1}$	SDRAM clock (negative lines)
DM0 - DM8	data masks
DQS0 - DQS8	data strobes

Pin Name	Pin Function
$\overline{CS0}$, $\overline{CS1}$	Chip Selects
V_{DD}	Power (+ 2.5 V)
V_{SS}	Ground
V_{DDQ}	I/O Driver power supply
V_{DDID}	VDD Indentification flag
V_{REF}	I/O reference supply
V_{DDSPD}	Serial EEPROM power supply
SCL	Serial bus clock
SDA	Serial bus data line
SA0 - SA2	slave address select
NC	no connect
DU	Dont use, reserved

Address Format

Density	Organization	Memory Banks	SDRAMs	# of SDRAMs	SDRAM density	# of row/ bank/ column bits	Refresh	Period	Interval
1024 MB	128M × 64	2	64M x 8	16	512 Mbit	13/2/11	8k	64 ms	7.8 µs

Pin Configuration

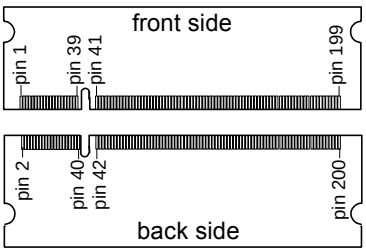
Pin #	Front Side	Pin #	Back Side
1	VREF	2	VREF
3	VSS	4	VSS
5	DQ0	6	DQ4
7	DQ1	8	DQ5
9	VDD	10	VDD
11	DQS0	12	DM0
13	DQ2	14	DQ6
15	VSS	16	VSS
17	DQ3	18	DQ7
19	DQ8	20	DQ12
21	VDD	22	VDD
23	DQ9	24	DQ13
25	DQS1	26	DM1
27	VSS	28	VSS
29	DQ10	30	DQ14
31	DQ11	32	DQ15
33	VDD	34	VDD
35	CK0	36	VDD
37	$\overline{\text{CK0}}$	38	VSS
39	VSS	40	VSS
41	DQ16	42	DQ20
43	DQ17	44	DQ21
45	VDD	46	VDD
47	DQS2	48	DM2
49	DQ18	50	DQ22

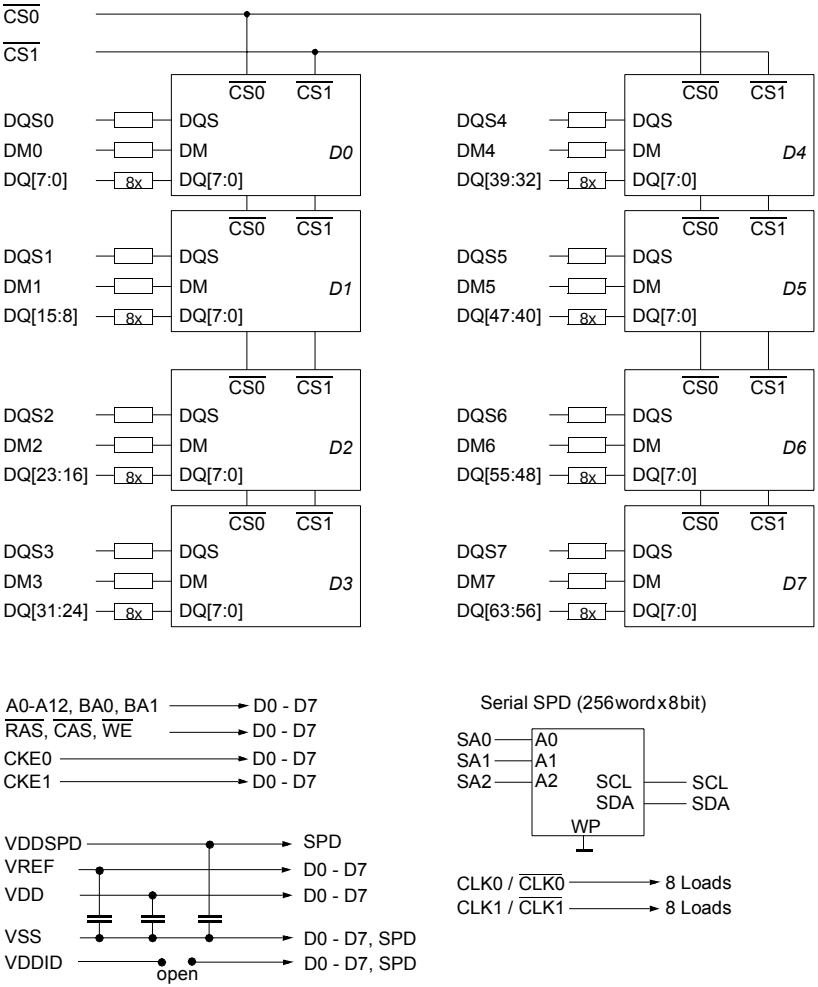
Pin #	Front Side	Pin #	Back Side
51	VSS	52	VSS
53	DQ19	54	DQ23
55	DQ24	56	DQ28
57	VDD	58	VDD
59	DQ25	60	DQ29
61	DQS3	62	DM3
63	VSS	64	VSS
65	DQ26	66	DQ30
67	DQ27	68	DQ31
69	VDD	70	VDD
71	(CB0)	72	(CB4)
73	(CB1)	74	(CB5)
75	VSS	76	VSS
77	(DQS8)	78	(DM8)
79	(CB2)	80	(CB6)
81	VDD	82	VDD
83	(CB3)	84	(CB7)
85	DU	86	DU
87	VSS	88	VSS
89	(CK2)	90	VSS
91	$\overline{\text{(CK2)}}$	92	VDD
93	VDD	94	VDD
95	CKE1	96	CKE0
97	DU	98	DU
99	A12	100	A11

Pin #	Front Side	Pin #	Back Side
101	A9	102	A8
103	VSS	104	VSS
105	A7	106	A6
107	A5	108	A4
109	A3	110	A2
111	A1	112	A0
113	VDD	114	VDD
115	A10/AP	116	BA1
117	BA0	118	$\overline{\text{RAS}}$
119	$\overline{\text{WE}}$	120	$\overline{\text{CAS}}$
121	$\overline{\text{CS0}}$	122	$\overline{\text{CS1}}$
123	DU	124	DU
125	VSS	126	VSS
127	DQ32	128	DQ36
129	DQ33	130	DQ37
131	VDD	132	VDD
133	DQS4	134	DM4
135	DQ34	136	DQ38
137	VSS	138	VSS
139	DQ35	130	DQ39
141	DQ40	142	DQ44
143	VDD	144	VDD
145	DQ41	146	DQ45
147	DQS5	148	DM5
149	VSS	150	VSS

Pin #	Front Side	Pin #	Back Side
151	DQ42	152	DQ46
153	DQ43	154	DQ47
155	VDD	156	VDD
157	VDD	158	$\overline{\text{CK1}}$
159	VSS	160	CK1
161	VSS	162	VSS
163	DQ48	164	DQ52
165	DQ49	166	DQ53
167	VDD	168	VDD
169	DQS6	170	DM6
171	DQ50	172	DQ54
173	VSS	174	VSS
175	DQ51	176	DQ55
177	DQ56	178	DQ60
179	VDD	180	VDD
181	DQ57	182	DQ61
183	DQS7	184	DM7
185	VSS	186	VSS
187	DQ58	188	DQ62
189	DQ59	190	DQ63
191	VDD	192	VDD
193	SDA	194	SA0
195	SCL	196	SA1
197	Vddspd	198	SA2
199	Vddid	200	DU

Note: Pins 71, 72, 73, 74, 77, 78, 79, 80, 83, 84, 89 and 91 are reserved for x72 variants of this module and are not used on the x64 versions. Pin 86 is reserved for a registered variant of this module and is not used on the unbuffered version





Note

1. DQ wiring may differ than describes in this drawing, however DQ/DM/DQS relationship must be maintained as shown.

2. All resistors are 22 Ohm.

Block Diagram: Two Banks 128M x 64 DDR-SDRAM SO-DIMM Modules using x8 Organized SDRAMs

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input / Output voltage relative to V_{SS}	V_{IN}, V_{OUT}	-0.5	3.6	V
Power supply voltage on V_{DD}/V_{DDQ} to V_{SS}	V_{DD}, V_{DDQ}	-0.5	3.6	V
Storage temperature range	T_{STG}	-55	+150	°C
Power dissipation (per SDRAM component)	P_D	–	1	W
Data out current (short circuit)	I_{OS}	–	50	mA

Permanent device damage may occur if “Absolute Maximum Ratings” are exceeded.
Functional operation should be restricted to recommended operation conditions.
Exposure to higher than recommended voltage for extended periods of time affect device reliability

Supply Voltage Levels

Parameter	Symbol	Limit Values			Unit	Notes
		min.	nom.	max.		
Device Supply Voltage	V_{DD}	2.3	2.5	2.7	V	
Output Supply Voltage	V_{DDQ}	2.3	2.5	2.7	V	1
Input Reference Voltage	V_{REF}	0.49 x V_{DDQ}	0.5 x V_{DDQ}	0.51 x V_{DDQ}	V	2
Termination Voltage	V_{TT}	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V	3
EEPROM supply voltage	V_{DDSPD}	2.3	2.5	3.6	V	

1 Under all conditions, V_{DDQ} must be less than or equal to V_{DD}
2 Peak to peak AC noise on V_{REF} may not exceed ± 2% $V_{REF\ (DC)}$.
V_{REF} is also expected to track noise variations in V_{DDQ}.
3 V_{TT} of the transmitting device must track V_{REF} of the receiving device.

DC Operating Conditions (SSTL_2 Inputs)

(VDDQ = 2.5 V, TA = 70 °C, Voltage Referenced to VSS)

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
DC Input Logic High	$V_{IH\ (DC)}$	V_{REF} + 0.15	V_{DDQ} + 0.3	V	1
DC Input Logic Low	$V_{IL\ (DC)}$	-0.30	V_{REF} - 0.15	V	
Input Leakage Current	I_{IL}	-5	5	µA	1
Output Leakage Current	I_{OL}	-5	5	µA	2

1) The relationship between the V_{DDQ} of the driving device and the V_{REF} of the receiving device is what determines noise margins. However, in the case of $V_{IH\ (max)}$ (input overdrive), it is the V_{DDQ} of the receiving device that is referenced. In the case where a device is implemented such that it supports SSTL_2 inputs but has no SSTL_2 outputs (such as a translator), and therefore no V_{DDQ} supply voltage connection, inputs must tolerate input overdrive to 3.0 V (High corner V_{DDQ} + 300 mV).
2) For any pin under test input of 0 V ≤ V_{IN} ≤ V_{DDQ} + 0.3 V. Values are shown per DDR-SDRAM component.

Operating, Standby and Refresh Currents

Symbol	Parameter/Condition	1GB, 2 banks -6 PC2700S-2533		1GB, 2 banks -7 PC2100S-2033		Unit	Notes
		TYP	MAX	TYP	MAX		4
IDD0	**Operating Current**: one bank; active / precharge; tRC = tRC MIN; DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles	1360	1560	1208	1400	mA	1
IDD1	**Operating Current**: one bank; active/read/precharge; burst length 4; Refer to the following page for detailed test conditions.	1552	1760	1416	1600	mA	1, 3
IDD2P	**Precharge Power-Down Standby Current**: all banks idle; power-down mode; CKE <= VIL MAX	120	176	112	160	mA	2
IDD2F	**Precharge Floating Standby Current**: /CS >= VIH MIN, all banks idle; CKE >= VIH MIN; address and other control inputs changing once per clock cycle, VIN = VREF for DQ, DQS and DM.	576	656	496	560	mA	2
IDD2Q	**Precharge Quiet Standby Current**: /CS >= VIH MIN, all banks idle; CKE >= VIH MIN; address and other control inputs stable at >= VIH MIN or <= VIL MAX; VIN = VREF for DQ, DQS and DM.	440	528	384	448	mA	2
IDD3P	**Active Power-Down Standby Current**: one bank active; power-down mode; CKE <= VIL MAX; VIN = VREF for DQ, DQS and DM.	256	320	224	288	mA	2
IDD3N	**Active Standby Current**: one bank active; CS >= VIH MIN; CKE >= VIH MIN; tRC = tRAS MAX; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	688	800	608	720	mA	2
IDD4R	**Operating Current**: one bank active; burst length 2; reads; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR200 and DDR266(A), CL=3 for DDR333 and DDR400; IOUT = 0mA	1680	1960	1424	1680	mA	1, 3
IDD4W	**Operating Current**: one bank active; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR200 and DDR266(A), CL=3 for DDR333 and DDR400	1600	1880	1368	1600	mA	1
IDD5	**Auto-Refresh Current**: tRC = tRFC MIN, distributed refresh	2328	2600	2200	2480	mA	1
IDD6	**Self-Refresh Current**: CKE <= 0.2V; external clock on	40	56	40	56	mA	
IDD7	**Operating Current**: four bank; four bank interleaving with burst length 4; Refer to the following page for detailed test conditions.	3056	3440	2536	3000	mA	1, 3

1. The module IDD values are calculated from the component IDD datasheet values as: *IDDx[component] * m + IDD3N[component] * n*
   with *m, n* number of components of bank 1 and 2; n=0 for 1 bank modules
2. The module IDD values are calculated from the component IDD datasheet values as: *IDDx[component] * (m + n)*
3. DQ I/O (IDDQ) currents are not included into calculations: module IDD values will be measured differently depending on load conditions
4. Test condition for typical values : VDD = 2.5V ,Ta = 25°C, test condition for maximum values: test limit at VDD = 2.7V ,Ta = 10°C

Electrical Characteristics & AC Timing for DDR-I components

(for reference only)

(0 °C ≤ T_A ≤ 70 °C; V_{DDQ} = 2.5V ± 0.2V; V_{DD} = 2.5V ± 0.2V)

Symbol	Parameter		DDR333 -6		DDR266A -7		Unit	Notes
			min.	max.	min.	max.		
t_{AC}	DQ output access time from CK/$\overline{CK}$		- 0.7	+ 0.7	– 0.75	+ 0.75	ns	1-4
t_{DQSCK}	DQS output access time from CK/$\overline{CK}$		- 0.6	+ 0.6	– 0.75	+ 0.75	ns	1-4
t_{CH}	CK high-level width		0.45	0.55	0.45	0.55	t_{CK}	1-4
t_{CL}	CK low-level width		0.45	0.55	0.45	0.55	t_{CK}	1-4
t_{HP}	Clock Half Period		min (t_{CL}, t_{CH})		min (t_{CL}, t_{CH})		ns	1-4
t_{CK}	Clock cycle time	CL = 2.5	6	12	7	12	ns	1-4
t_{CK}		CL = 2.0	7.5	12	7.5	12	ns	1-4
t_{DH}	DQ and DM input hold time		0.45		0.5		ns	1-4
t_{DS}	DQ and DM input setup time		0.45		0.5		ns	1-4
t_{IPW}	Control and Addr. input pulse width (each input)		2.2		2.2		ns	1, 10
t_{DIPW}	DQ and DM input pulse width (each input)		1.75		1.75		ns	1-4, 11
t_{HZ}	Data-out high-impedence time from CK/$\overline{CK}$		- 0.7	+ 0.7	– 0.75	+ 0.75	ns	1-4, 5
t_{LZ}	Data-out low-impedence time from CK/$\overline{CK}$		- 0.7	+ 0.7	– 0.75	+ 0.75	ns	1-4, 5
t_{DQSS}	Write command to 1st DQS latching transition		0.75	1.25	0.75	1.25	t_{CK}	1-4
t_{DQSQ}	DQS-DQ skew (for DQS & associated DQ signals)			+ 0.40		+ 0.5	ns	1-4
t_{QHS}	Data hold skew factor			+ 0.50		+ 0.75	ns	1-4
t_{QH}	Data Output hold time from DQS		t_{HP}-t_{QHS}		t_{HP}-t_{QHS}		ns	1-4
$t_{DQSL,H}$	DQS input low (high) pulse width (write cycle)		0.35		0.35		t_{CK}	1-4
t_{DSS}	DQS falling edge to CK setup time (write cycle)		0.2		0.2		t_{CK}	1-4
t_{DSH}	DQS falling edge hold time from CK (write cycle)		0.2		0.2		t_{CK}	1-4
t_{MRD}	Mode register set command cycle time		2		2		t_{CK}	1-4
t_{WPRES}	Write preamble setup time		0		0		ns	1-4, 7
t_{WPST}	Write postamble		0.40	0.60	0.40	0.60	t_{CK}	1-4, 6
t_{WPRE}	Write preamble		0.25		0.25		t_{CK}	1-4
t_{IS}	Address and control input setup time	fast slew rate	0.75		0.9		ns	2-4, 10,11
		slow slew rate	0.8		1.0		ns	
t_{IH}	Address and control input hold time	fast slew rate	0.75		0.9		ns	
		slow slew rate	0.8		1.0		ns	
t_{RPRE}	Read preamble		0.9	1.1	0.9	1.1	t_{CK}	1-4
t_{RPST}	Read postamble		0.40	0.60	0.40	0.60	t_{CK}	1-4
t_{RAS}	Active to Precharge command		42	70,000	45	120,000	ns	1-4
t_{RC}	Active to Active/Auto-refresh command period		60		65		ns	1-4
t_{RFC}	Auto-refresh to Active/Auto-refresh command period		72		75		ns	1-4
t_{RCD}	Active to Read or Write delay		18		20		ns	1-4
t_{RP}	Precharge command period		18		20		ns	1-4
t_{RRD}	Active bank A to Active bank B command		12		15		ns	1-4
t_{WR}	Write recovery time		15		15		ns	1-4
t_{DAL}	Auto precharge write recovery + precharge time		(twr/tck) + (trp/tck)				t_{CK}	1-4,9

Symbol	Parameter	DDR333 -6		DDR266A -7		Unit	Notes
		min.	max.	min.	max.		
t_{WTR}	Internal write to read command delay	1		1		t_{CK}	1-4
t_{XSNR}	Exit self-refresh to non-read command	75		75		ns	1-4
t_{XSRD}	Exit self-refresh to read command	200		200		t_{CK}	1-4
t_{REFI}	Average Periodic Refresh Interval		7.8		7.8	µs	1-4, 8

1. Input slew rate >=1V/ns for DDR266 & DDR333 and = 1V/ns for DDR200.
2. The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross: the input reference level for signals other than CK/$\overline{CK}$, is V_{REF}. CK/$\overline{CK}$ slew rate are >= 1.0 V/ns.
3. Inputs are not recognized as valid until V_{REF} stabilizes.
4. The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (Note 3) is V_{TT}.
5. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
6. The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
7. The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.
8. A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.
9. For each of the terms, if not already an integer, round to the next highest integer. tCK is equal to the actual system clock cycle time.
10. These parameters guarantee device timing, but they are not necessarily tested on each device
11. Fast slew rate >= 1.0 V/ns , slow slew rate >= 0.5 V/ns and < 1V/ns for command/address and CK & $\overline{CK}$ slew rate >1.0 V/ns, measured between VOH(ac) and VOL(ac)

SPD Codes

Byte#	Description	SPD Entry Value	PC2100	PC2700
0	Number of SPD Bytes	128	80	
1	Total Bytes in Serial PD	256	08	
2	Memory Type	DDR-SDRAM	07	
3	Number of Row Addresses	13	0D	
4	Number of Column Addresses	11	0B	
5	Number of DIMM Banks	2	02	
6	Module Data Width	x64	40	
7	Module Data Width (cont'd)	0	00	
8	Module Interface Levels	SSTL_2.5	04	
9	SDRAM Cycle Time at CL = 2.5	7ns, 6ns	70	60
10	SDRAM Access Time from Clock at CL = 2.5	0.75ns, 0.6ns	75	70
11	DIMM Config	non-ECC	00	
12	Refresh Rate/Type	Self-Refresh 7.8µs	82	
13	SDRAM Width, Primary	x8	08	
14	Error Checking SDRAM Data Width	na	00	
15	Minimum Clock Delay for Back-to-Back Random Column Address	t_{CCD} = 1 CLK	01	
16	Burst Length Supported	2, 4 & 8	0E	
17	Number of SDRAM Banks	4	04	
18	Supported $\overline{CAS}$ Latencies	$\overline{CAS}$ latency = 2 & 2.5	0C	
19	$\overline{CS}$ Latencies	$\overline{CS}$ latency = 0	01	
20	$\overline{WE}$ Latencies	Write latency = 1	02	
21	SDRAM DIMM Module Attributes	unbuffered	20	
22	SDRAM Device Attributes: General	Conc. AP weak driver	C1	
23	Min. Clock Cycle Time at $\overline{CAS}$ Latency = 2	7.5ns	75	75
24	Max. Data Access Time from Clock for CL = 2	0.75ns, 0.7ns	75	70
25	Minimum Clock Cycle Time at CL = 1.5	not supported	00	
26	Maximum Data Access Time from Clock at CL = 1.5	not supported	00	
27	Minimum Row Precharge Time	20ns, 18ns	50	48
28	Minimum Row Active to Row Active Delay t_{RRD}	15ns, 12ns	3C	30
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay t_{RCD}	20ns, 18ns	50	48
30	Minimum $\overline{RAS}$ Pulse Width t_{RAS}	45ns, 42ns	2D	2A
31	Module Bank Density (per bank)	512 MByte	80	
32	Addr. and Command Setup Time	0.9 ns, 0.75ns	90	75
33	Addr. and Command Hold Time	0.9 ns, 0.75ns	90	75
34	Data Input Setup Time	0.5ns, 0.45 ns	50	45
35	Data Input Hold Time	0.5ns, 0.45 ns	50	45
36-40	Superset Information	–	00	
41	Minimum Core Cycle Time tRC	65 ns, 60 ns	41	3C
42	Min. Auto Refresh Cmd Cycle Time tRFC	75ns, 72 ns	4B	48
43	Maximum Clock Cycle Time tck	12 ns	30	
44	Max. DQS-DQ Skew tDQSQ	0.5 ns, 0.4 ns	32	28
45	X-Factor tQHS	0.75ns, 0.5 ns	75	50
46-61	Superset Information (may be used in future)		00	
62	SPD Revision	Revision 0.0	00	

Byte#	Description	SPD Entry Value	PC2100	PC2700
63	Checksum for Bytes 0 - 62	–	F5	39
64	Manufacturers JEDEC ID	–	C1	
65-71	Manufacturer		INFINEO(N)	
72	Assembly Manufacturing Location			
73-90	Module Part Number			
91-92	Module Revision Code			
93-94	Module Manufacturing Date			
95-98	Module Serial Number			
99-127	Superset Information			
128-255	Open for Customer Use			

Package Outlines

DDR-SDRAM SO-DIMM Modules