Integrated Device Technology, Inc.

32K x 36, 3.3V SYNCHRONOUS BURST SRAM WITH FLOW-THROUGH OUTPUTS

PRELIMINARY
IDT71V537

FEATURES:

- 32K x 36 memory configuration
- Supports high performance system speed - up to 75 MHz (8 ns Clock-to-Data Access)
- $\overline{LBO}$ input selects interleaved or linear burst mode
- Self-timed write cycle with global write control ($\overline{GW}$), byte write enable ($\overline{BWE}$), and byte writes ($\overline{BW}$x)
- Power down controlled by ZZ input
- Operates with a single 3.3V power supply (+10/-5%)
- Packaged in a JEDEC Standard 100-pin rectangular plastic thin quad flatpack (TQFP)

DESCRIPTION:

The IDT71V537 is a 3.3V high-speed 1,179,648-bit SRAM organized as 32K x 36 with full support of various processor interfaces including the Pentium™ and PowerPC™. The flow-through burst architecture provides cost-effective 2-1-1-1 performance for processors up to 75 MHz.

The IDT71V537 SRAM contains write, data-input, address and control registers. There are no registers in the data output path (flow-through architecture). Internal logic allows the SRAM to generate a self-timed write based upon a decision which can be left until the extreme end of the write cycle.

The burst mode feature offers the highest level of performance to the system designer, as the IDT71V537 can provide four cycles of data for a single address presented to the SRAM. An internal burst address counter accepts the first cycle address from the processor, initiating the access sequence. The first cycle of output data will flow-through from the array after a clock-to-data access time delay from the rising clock edge of the same cycle. If burst mode operation is selected ($\overline{ADV}$=LOW), the subsequent three cycles of output data will be available to the user on the next three rising clock edges. The order of these three addresses will be defined by the internal burst counter and the $\overline{LBO}$ input pin.

The IDT71V537 SRAM utilizes IDT's high-performance 3.3V CMOS process, and is packaged in a JEDEC Standard 14mm x 20mm 100-pin thin plastic quad flatpack (TQFP).

PIN DESCRIPTION SUMMARY

$A_0 - A_{14}$	Address Inputs	Input	Synchronous
$\overline{CE}$	Chip Enable	Input	Synchronous
CS_0, $\overline{CS_1}$	Chips Selects	Input	Synchronous
$\overline{OE}$	Output Enable	Input	Asynchronous
$\overline{GW}$	Global Write Enable	Input	Synchronous
$\overline{BWE}$	Byte Write Enable	Input	Synchronous
$\overline{BW_1}$-$\overline{BW_4}$	Individual Byte Write Selects	Input	Synchronous
CLK	Clock Input	Input	N/A
$\overline{ADV}$	Burst Address Advance	Input	Synchronous
$\overline{ADSC}$	Address Status (Cache Controller)	Input	Synchronous
$\overline{ADSP}$	Address Status (Processor)	Input	Synchronous
$\overline{LBO}$	Linear / Interleaved Burst Order	Input	DC
ZZ	Sleep Mode	Input	Asynchronous
I/O_0-I/O_{31}	Data Input/Output	I/O	Synchronous
I/OP_1-I/OP_4	Data Input/Output (Parity)	I/O	Synchronous
V_{DD}, V_{DDQ}	3.3V	Power	N/A
V_{SS}, V_{SSQ}	Array Ground, I/O Ground	Power	N/A

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 For latest information contact IDT's web site at www.idt.com or fax-on-demand at 408-492-8391.

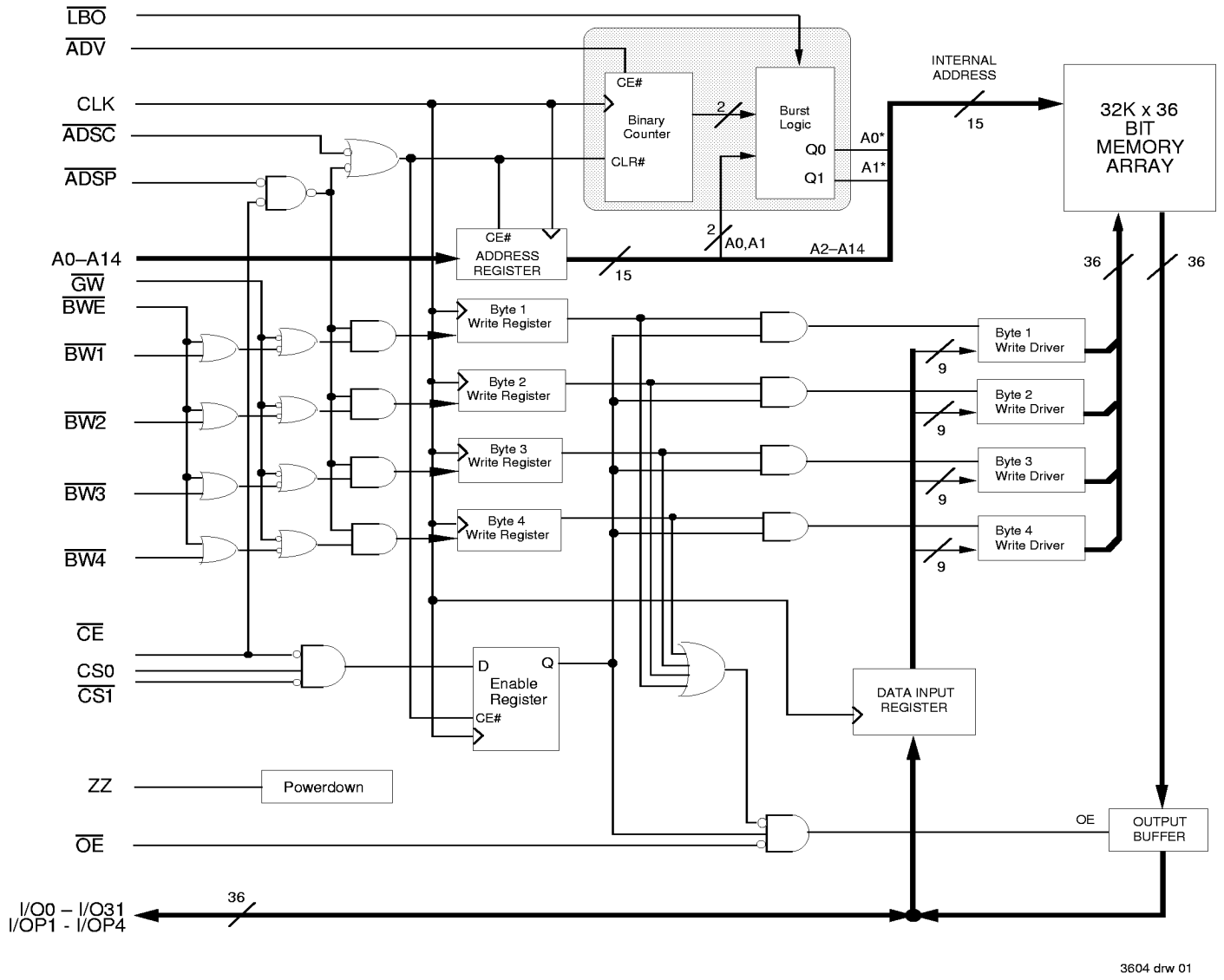
PIN DEFINITIONS(1)

Symbol	Pin Function	I/O	Active	Description
A_0-A_{14}	Address Inputs	I	N/A	Synchronous Address inputs. The address register is triggered by a combination of the rising edge of CLK and $\overline{ADSC}$ Low or $\overline{ADSP}$ Low and $\overline{CE}$ Low.
$\overline{ADSC}$	Address Status (Cache Controller)	I	LOW	Synchronous Address Status from Cache Controller. $\overline{ADSC}$ is an active LOW input that is used to load the address registers with new addresses. $\overline{ADSC}$ is NOT GATED by $\overline{CE}$.
$\overline{ADSP}$	Address Status (Processor)	I	LOW	Synchronous Address Status from Processor. $\overline{ADSP}$ is an active LOW input that is used to load the address registers with new addresses. $\overline{ADSP}$ is gated by $\overline{CE}$.
$\overline{ADV}$	Burst Address Advance	I	LOW	Synchronous Address Advance. $\overline{ADV}$ is an active LOW input that is used to advance the internal burst counter, controlling burst access after the initial address is loaded. When this input is HIGH the burst counter is not incremented; that is, there is no address advance.
$\overline{BWE}$	Byte Write Enable	I	LOW	Synchronous byte write enable gates the byte write inputs $\overline{BW_1}$-$\overline{BW_4}$. If $\overline{BWE}$ is LOW at the rising edge of CLK then $\overline{BW}$X inputs are passed to the next stage in the circuit. A byte write can still be blocked if $\overline{ADSP}$ is LOW at the rising edge of CLK. If $\overline{ADSP}$ is HIGH and $\overline{BW}$X is LOW at the rising edge of CLK then data will be written to the SRAM. If $\overline{BWE}$ is HIGH then the byte write inputs are blocked and only $\overline{GW}$ can initiate a write cycle.
$\overline{BW_1}$-$\overline{BW_4}$	Individual Byte Write Enables	I	LOW	Synchronous byte write enables. Each 9-bit byte has its own active LOW byte write. Any active byte write causes all outputs to be disabled. $\overline{ADSP}$ LOW disables all byte writes. $\overline{BW_1}$-$\overline{BW_4}$ must meet specified setup and hold times with respect to CLK.
$\overline{CE}$	Chip Enable	I	LOW	Synchronous chip enable. $\overline{CE}$ is used with CS_0 and $\overline{CS_1}$ to enable the IDT71V537. $\overline{CE}$ also gates $\overline{ADSP}$.
CLK	Clock	I	N/A	This is the clock input. All timing references for the device are made with respect to this input.
CS_0	Chip Select 0	I	HIGH	Synchronous active HIGH chip select. CS_0 is used with $\overline{CE}$ and $\overline{CS_1}$ to enable the chip.
$\overline{CS_1}$	Chip Select 1	I	LOW	Synchronous active LOW chip select. $\overline{CS_1}$ is used with $\overline{CE}$ and CS_0 to enable the chip.
$\overline{GW}$	Global Write Enable	I	LOW	Synchronous global write enable. This input will write all four 9-bit data bytes when LOW on the rising edge of CLK. $\overline{GW}$ superceeds individual byte write enables.
I/O_0-I/O_{31} I/OP_1-I/OP_4	Data Input/Output	I/O	N/A	Synchronous data input/output (I/O) pins. Only the data input path is registered and triggered by the rising edge of CLK. Outputs are Flow-through.
$\overline{LBO}$	Linear Burst Order	I	LOW	Asynchronous burst order selection DC input. When $\overline{LBO}$ is HIGH the Interleaved (Intel) burst sequence is selected. When $\overline{LBO}$ is LOW the Linear (PowerPC) burst sequence is selected. $\overline{LBO}$ is a static DC input and must not change state while the device is operating. $\overline{LBO}$ has an internal pull-up resistor.
$\overline{OE}$	Output Enable	I	LOW	Asynchronous output enable. When $\overline{OE}$ is HIGH the I/O pins are in a high-impedence state. When $\overline{OE}$ is LOW the data output drivers are enabled if the chip is also selected.
V_{DD}	Power Supply	N/A	N/A	3.3V core power supply inputs.
V_{DDQ}	Power Supply	N/A	N/A	3.3V I/O power supply inputs.
V_{SS}	Ground	N/A	N/A	Core ground pins.
V_{SSQ}	Ground	N/A	N/A	I/O ground pins.
NC	No Connect	N/A	N/A	NC pins are not electrically connected to the chip.
ZZ	Sleep Mode	I	HIGH	Asynchronous sleep mode input. ZZ HIGH will gate the CLK internally and power down the IDT71V537 to its lowest power consumption level. Data retention is guaranteed in Sleep Mode. ZZ has an internal pull-down resistor.

NOTE:
1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

3604 tbl 02

FUNCTIONAL BLOCK DIAGRAM



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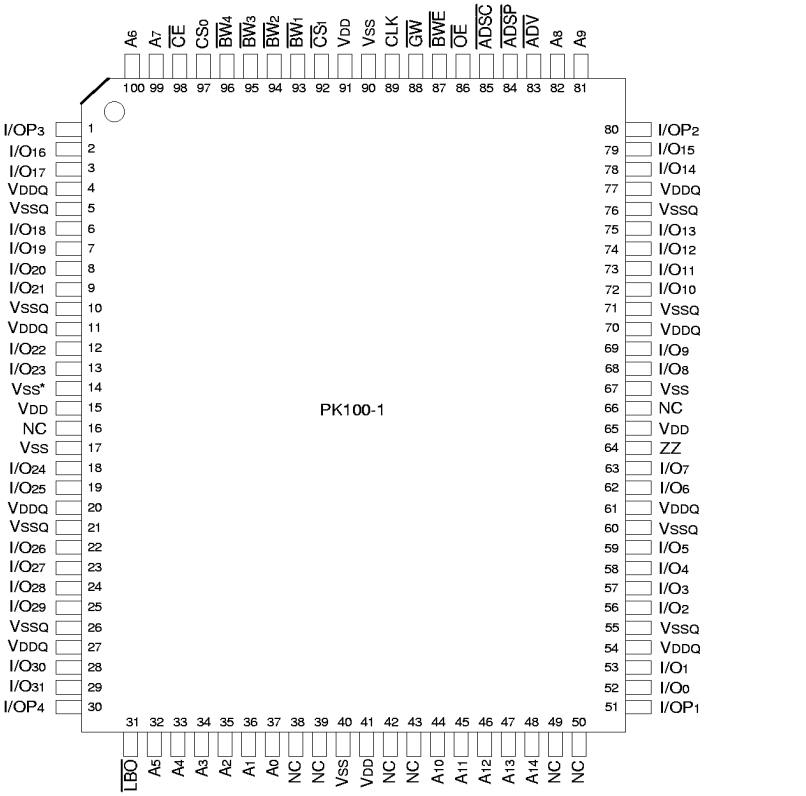
RECOMMENDED DC OPERATING

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Core Supply Voltage	3.135	3.3	3.63	V
V_{DDQ}	I/O Supply Voltage	3.135	3.3	3.63	V
V_{SS}, V_{SSQ}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.0(1)	—	V_{DDQ}+.5(2)	V
V_{IL}	Input Low Voltage	-0.5(3)	—	0.8	V

3604 tbl 03

NOTE:
1. V_{IH} and V_{IL} as indicated is for both input and I/O pins.
2. V_{IH} (max) = 6.0V for pulse width less than tCYC/2, once per cycle.
3. V_{IL} (min) = -1.0V for pulse width less than tCYC/2, once per cycle.

PIN CONFIGURATION



* Pin 14 does not have to be directly connected to V_{SS} as long as the input voltage is ≤ V_{IL}

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TOP VIEW
TQFP

ABSOLUTE MAXIMUM DC RATINGS(1)

Symbol	Rating	Com'l.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to +V_{DD}+0.5	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.2	W
I_{OUT}	DC Output Current	50	mA

NOTES: 3604 tbl 05

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{DD}, V_{DDQ} and input terminals only.
3. I/O terminals.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz, TQFP package)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	4	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

NOTE: 3604 tbl 06

1. This parameter is guaranteed by device characterization, but not production tested.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{DD} = 3.3V +10/-5%)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	5	µA
$\|I_{LI}\|$	ZZ & $\overline{LBO}$ Input Leakage Current(1)	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	30	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE} \geq V_{IH}$ or $\overline{OE} \geq V_{IH}$, V_{OUT} = 0V to V_{DD}, V_{DD} = Max.	—	5	µA
V_{OL} (3.3V)	Output Low Voltage	I_{OL} = 5mA, V_{DD} = Min.	—	0.4	V
V_{OH} (3.3V)	Output High Voltage	I_{OL} = –5mA, V_{DD} = Min.	2.4	—	V

NOTE: 3604 tbl 07

1. The $\overline{ZZ}$ pin has an internal pull-down resistor to V_{SSQ}.
   The $\overline{LBO}$ pin has an internal pull-up resistor to V_{DDQ}.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(1) (V_{HD} = V_{DDQ}–0.2V, V_{LD} = 0.2V)

Symbol	Parameter	Test Condition	75MHz(3)	66MHz(3)	60MHz	50MHz	Unit
I_{DD}	Operating Core Power Supply Current	Device Selected, Outputs Open, V_{DD} = Max., V_{DDQ} = Max., $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, f = f_{MAX}(2)	225	220	215	200	mA
I_{SB}	Standby Core Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., V_{DDQ} = Max., $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, f = f_{MAX}(2)	75	70	65	55	mA
I_{SB1}	Full Standby Core Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., V_{DDQ} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = 0(2)	15	15	15	15	mA
I_{ZZ}	Full Sleep Mode Core Power Supply Current	ZZ $\geq V_{HD}$, V_{DD} = Max., V_{DDQ} = Max.	10	10	10	10	mA

NOTES: 3604 tbl 07

1. All values are maximum guaranteed values.
2. At f = f_{MAX}, inputs are cycling at the maximum frequency of read cycles of 1/t_{CYC} while $\overline{ADSC}$ = LOW; f=0 means no input lines are changing.
3. 75 MHz and 66 MHz specs are prelimnary

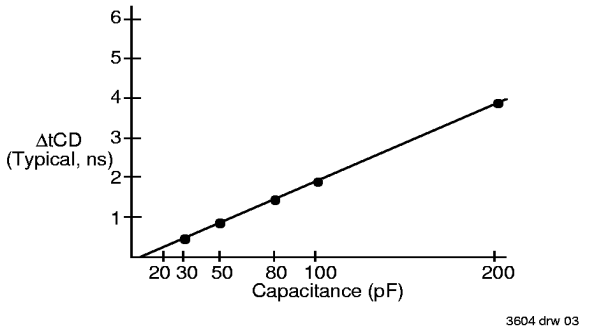


Figure 1. Lumped Capacitive Load, Typical Derating

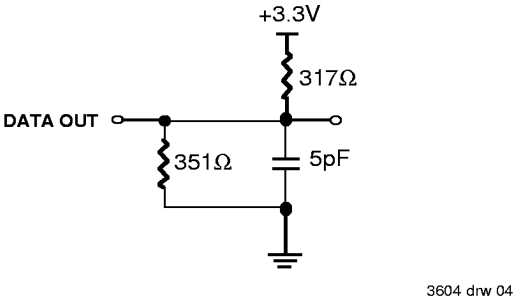


Figure 2. High-Impedence Test Load (for t_{OHZ}, t_{CHZ}, t_{OLZ}, and t_{DC1})

* Including scope and jig

SYNCHRONOUS TRUTH TABLE(1, 2)

Operation	Address Used	$\overline{CE}$	CS_0	$\overline{CS_1}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{GW}$	$\overline{BWE}$	$\overline{BWx}$	$\overline{OE}$ (3)	CLK	I/O
Deselected Cycle, Power Down	None	H	X	X	X	L	X	X	X	X	X	↑	HI-Z
Deselected Cycle, Power Down	None	L	X	H	L	X	X	X	X	X	X	↑	HI-Z
Deselected Cycle, Power Down	None	L	L	X	L	X	X	X	X	X	X	↑	HI-Z
Deselected Cycle, Power Down	None	L	X	H	X	L	X	X	X	X	X	↑	HI-Z
Deselected Cycle, Power Down	None	L	L	X	X	L	X	X	X	X	X	↑	HI-Z
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	X	L	↑	D_{OUT}
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	X	H	↑	HI-Z
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	H	X	L	↑	D_{OUT}
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	H	L	↑	D_{OUT}
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	H	H	↑	HI-Z
Write Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	L	X	↑	D_{IN}
Write Cycle, Begin Burst	External	L	H	L	H	L	X	L	X	X	X	↑	D_{IN}
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	X	L	↑	D_{OUT}
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	X	H	↑	HI-Z
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	X	H	L	↑	D_{OUT}
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	X	H	H	↑	HI-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	X	L	↑	D_{OUT}
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	X	H	↑	HI-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	X	H	L	↑	D_{OUT}
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	X	H	H	↑	HI-Z
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L	X	↑	D_{IN}
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	X	X	↑	D_{IN}
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L	X	↑	D_{IN}
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	X	X	↑	D_{IN}
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	X	L	↑	D_{OUT}
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	X	H	↑	HI-Z
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	X	H	L	↑	D_{OUT}
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	X	H	H	↑	HI-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	X	L	↑	D_{OUT}
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	X	H	↑	HI-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	X	H	L	↑	D_{OUT}
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	X	H	H	↑	HI-Z
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L	X	↑	D_{IN}
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	X	X	↑	D_{IN}
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L	X	↑	D_{IN}
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	X	X	↑	D_{IN}

NOTES:
1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. $\overline{ZZ}$ = LOW for this table.
3. $\overline{OE}$ is an asynchronous input.

3604 tbl 09

SYNCHRONOUS WRITE FUNCTION TRUTH TABLE(1)

Operation	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_1}$	$\overline{BW_2}$	$\overline{BW_3}$	$\overline{BW_4}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write all Bytes	L	X	X	X	X	X
Write all Bytes	H	L	L	L	L	L
Write Byte 1 (2)	H	L	L	H	H	H
Write Byte 2 (2)	H	L	H	L	H	H
Write Byte 3 (2)	H	L	H	H	L	H
Write Byte 4 (2)	H	L	H	H	H	L

NOTES: 3604 tbl 10
1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. Multiple bytes may be selected during the same cycle.

ASYNCHRONOUS TRUTH TABLE(1)

Operation(2)	$\overline{OE}$	ZZ	I/O Status	Power
Read	L	L	Data Out (I/O_0 – I/O_{31}, I/OP_1 - I/OP_2)	Active
Read	H	L	High-Z	Active
Write	X	L	High-Z — Data In (I/O_0 – I/O_{31}, I/OP_1 - I/OP_2)	Active
Deselected	X	L	High-Z	Standby
Sleep Mode	X	H	High-Z	Sleep

NOTES: 3604 tbl 11
1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. Synchronous function pins must be biased appropriately to satisfy operation requirements.

INTERLEAVED BURST SEQUENCE TABLE ($\overline{LBO}$=V_{DD})

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	0	0	1	1	1	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address(1)	1	1	1	0	0	1	0	0

NOTE: 3604 tbl 12
1. Upon completion of the Burst sequence the counter wraps around to its initial state.

LINEAR BURST SEQUENCE TABLE ($\overline{LBO}$=V_{SS})

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	1	0	1	1	0	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address(1)	1	1	0	0	0	1	1	0

NOTE: 3604 tbl 13
1. Upon completion of the Burst sequence the counter wraps around to its initial state.

AC ELECTRICAL CHARACTERISTICS

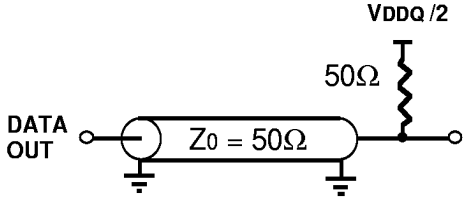
(V_{DD}, V_{DDQ} = 3.3V +10/-5%, T_A = 0 to 70°C

Symbol	Parameter	75 MHz[5]		66 MHz[5]		60 MHz		50 MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clock Parameters										
t_{CYC}	Clock Cycle Time	13	—	15	—	17	—	20	—	ns
t_{CH}[1]	Clock High Pulse Width	4	—	4.5	—	5	—	6	—	ns
t_{CL}[1]	Clock Low Pulse Width	4	—	4.5	—	5	—	6	—	ns
Output Parameters										
t_{CD}	Clock High to Valid Data	—	8	—	9	—	10	—	12	ns
t_{CDC}	Clock High to Data Change	3	—	3	—	3	—	3	—	ns
t_{CLZ}[2]	Clock High to Output Active	0	—	0	—	0	—	0	—	ns
t_{CHZ}[2]	Clock High to Data High-Z	3	5	3	5	3	5	3	6	ns
t_{OE}	Output Enable Access Time	—	5	—	5	—	5	—	6	ns
t_{OLZ}[2]	Output Enable Low to Data Active	0	—	0	—	0	—	0	—	ns
t_{OHZ}[2]	Output Enable High to Data High-Z	—	5	—	5	—	5	—	6	ns
Set Up Times										
t_{SA}	Address Setup Time	2.5	—	2.5	—	2.5	—	2.5	—	ns
t_{SS}	Address Status Setup Time	2.5	—	2.5	—	2.5	—	2.5	—	ns
t_{SD}	Data In Setup Time	2.5	—	2.5	—	2.5	—	2.5	—	ns
t_{SW}	Write Setup Time	2.5	—	2.5	—	2.5	—	2.5	—	ns
t_{SAV}	Address Advance Setup Time	2.5	—	2.5	—	2.5	—	2.5	—	ns
t_{SC}	Chip Enable/Select Setup Time	2.5	—	2.5	—	2.5	—	2.5	—	ns
Hold Times										
t_{HA}	Address Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{HS}	Address Status Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{HD}	Data In Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{HW}	Write Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{HAV}	Address Advance Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{HC}	Chip Enable/Select Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
Sleep Mode and Configuration Parameters										
t_{ZZPW}	ZZ Pulse Width	100	—	100	—	100	—	100	—	ns
t_{ZZR}[3]	ZZ Recovery Time	100	—	100	—	100	—	100	—	ns
t_{CFG}[4]	Configuration Set-up Time	48	—	60	—	60	—	80	—	ns

NOTES:
3604 tbl 14

1. Measured as HIGH above 2.0V and LOW below 0.8V.
2. Transition is measured ±200mV from steady-state.
3. Device must be deselected when powered-up from sleep mode.
4. t_{CFG} is the minimum time required to configure the device based on the $\overline{LBO}$ input. $\overline{LBO}$ is a static input and must not change during normal operation.
5. 75 MHz and 66 MHz specs are prelimnary.

AC TEST LOAD



3604 drw 05

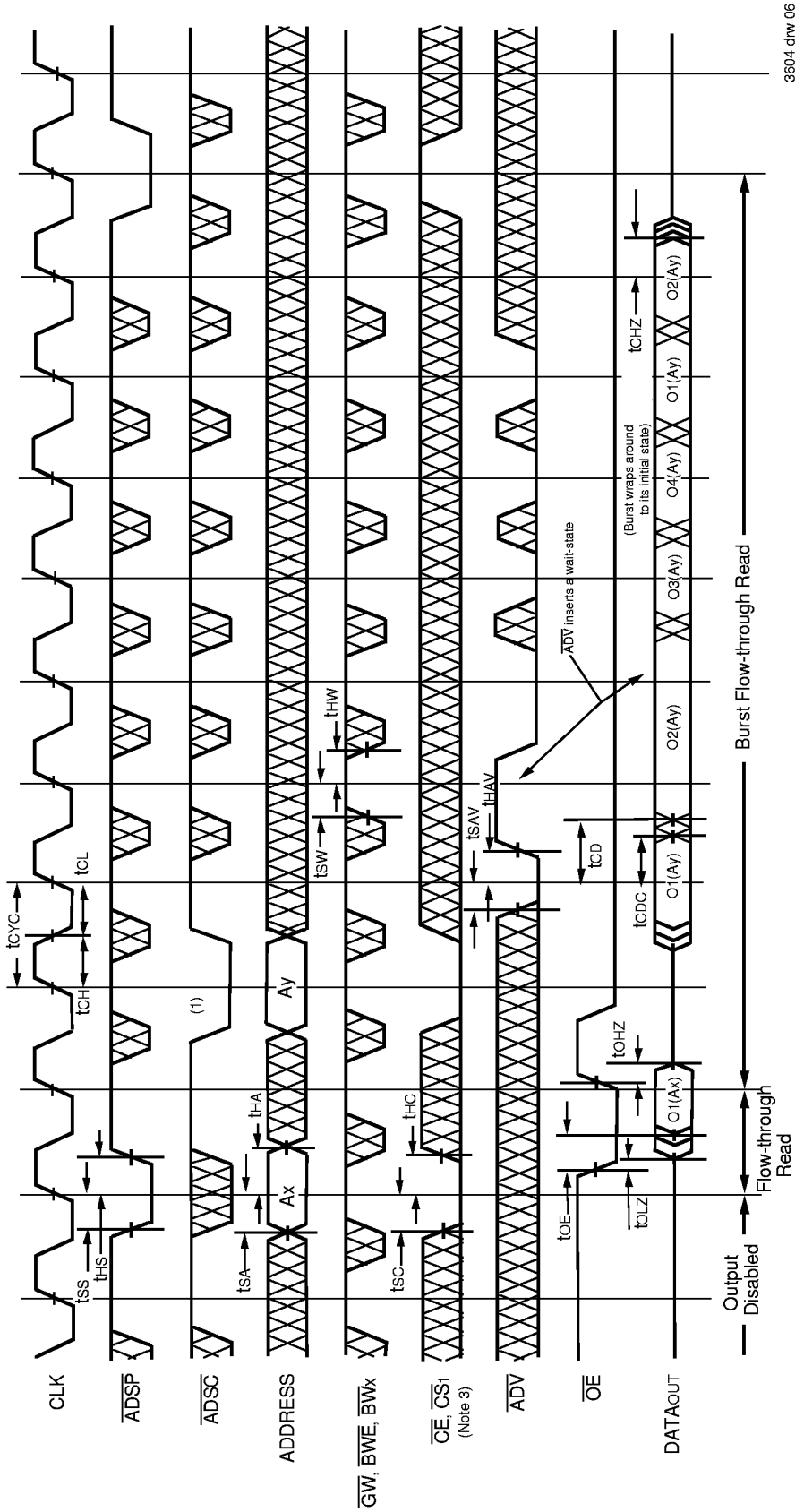
Figure 3. AC Test Load

AC TEST CONDITIONS

Input Pulse Levels	0 to 3V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
AC Test Load	See Figures 2 and 3

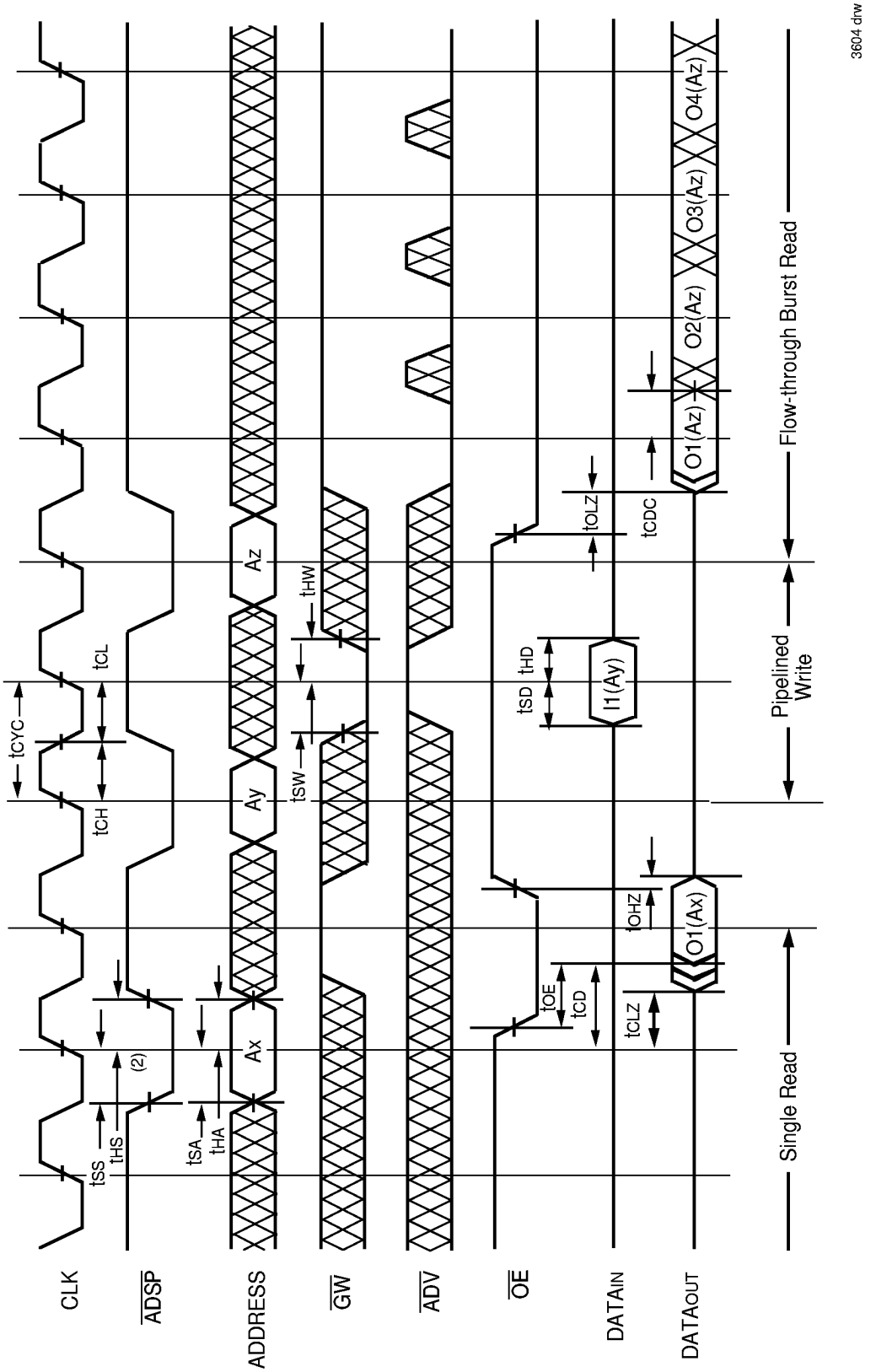
3604 tbl 15

TIMING WAVEFORM OF PIPELINED READ CYCLE(1, 2)



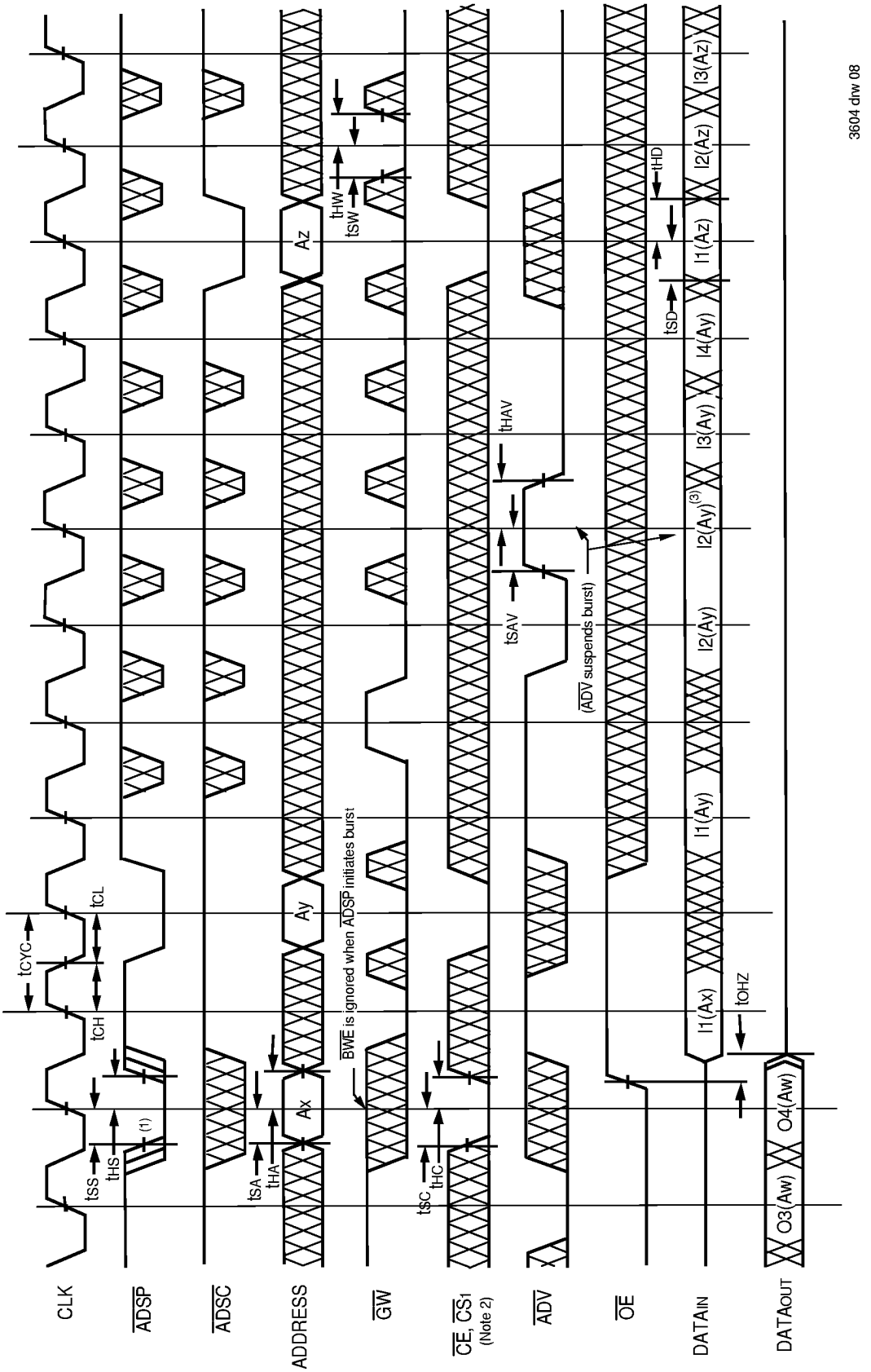
NOTES:
1. O1 (Ax) represents the first output from the external address Ax. O1 (Ay) represents the first output from the external address Ay; O2 (Ay) represents the next output data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.
2. $\overline{ZZ}$ input is LOW and $\overline{LBO}$ is Don't Care for this cycle.
3. $\overline{CS_0}$ timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS_1}$ signals. For example, when $\overline{CE}$ and $\overline{CS_1}$ are LOW on this waveform, $\overline{CS_0}$ is HIGH.

TIMING WAVEFORM OF COMBINED PIPELINED READ AND WRITE CYCLES(1, 2,3)



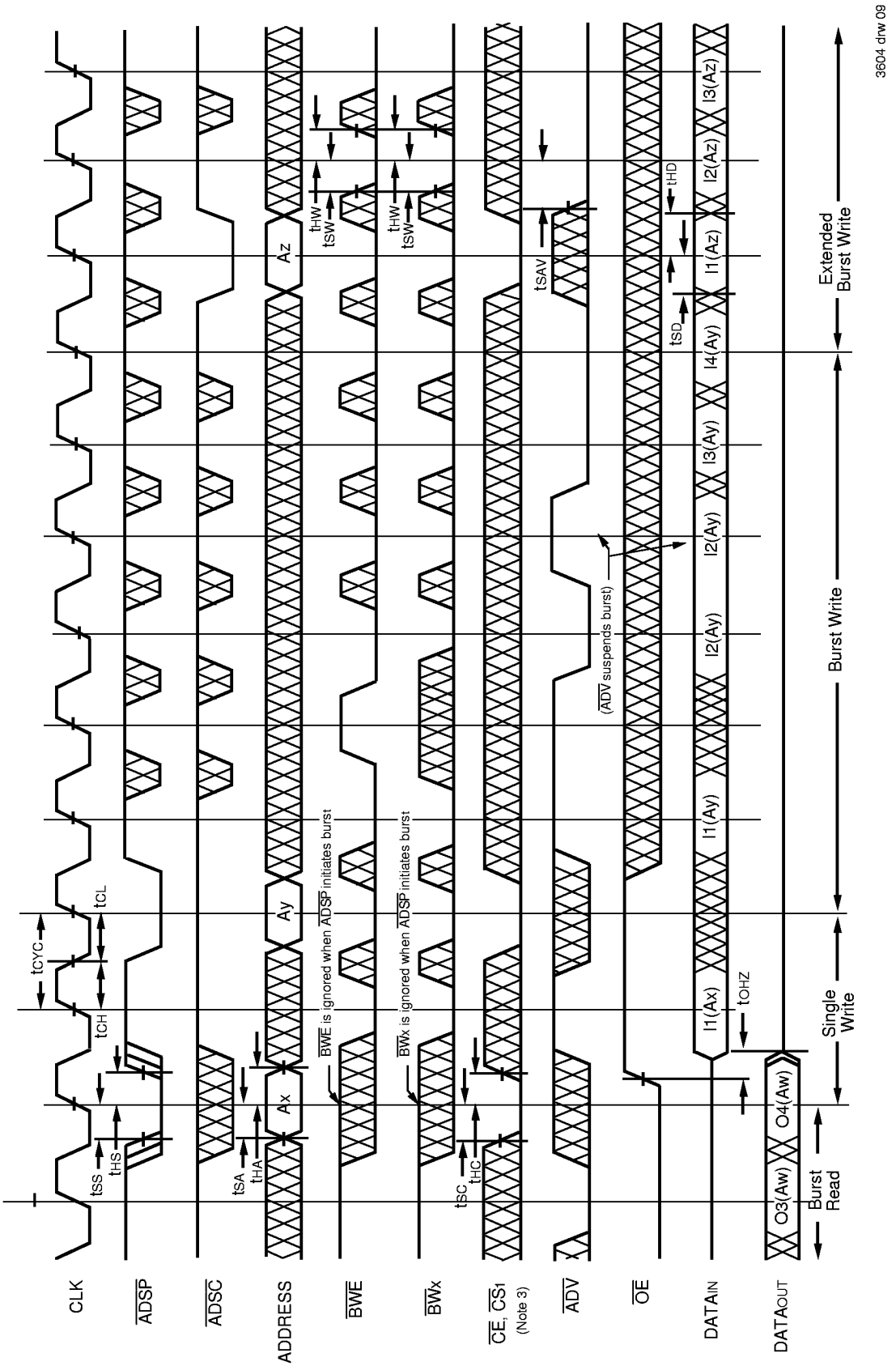
NOTES:
1. Device is selected through entire cycle; $\overline{CE}$ and $\overline{CS_1}$ are LOW, CS_0 is HIGH.
2. $\overline{ZZ}$ input is LOW and $\overline{LBO}$ is Don't Care for this cycle.
3. O1 (Ax) represents the first output from the external address Ax. O1 (Ay) represents the first output from the external address Ay; O2 (Ay) represents the next output data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 - $\overline{GW}$ CONTROLLED(1, 2, 3)



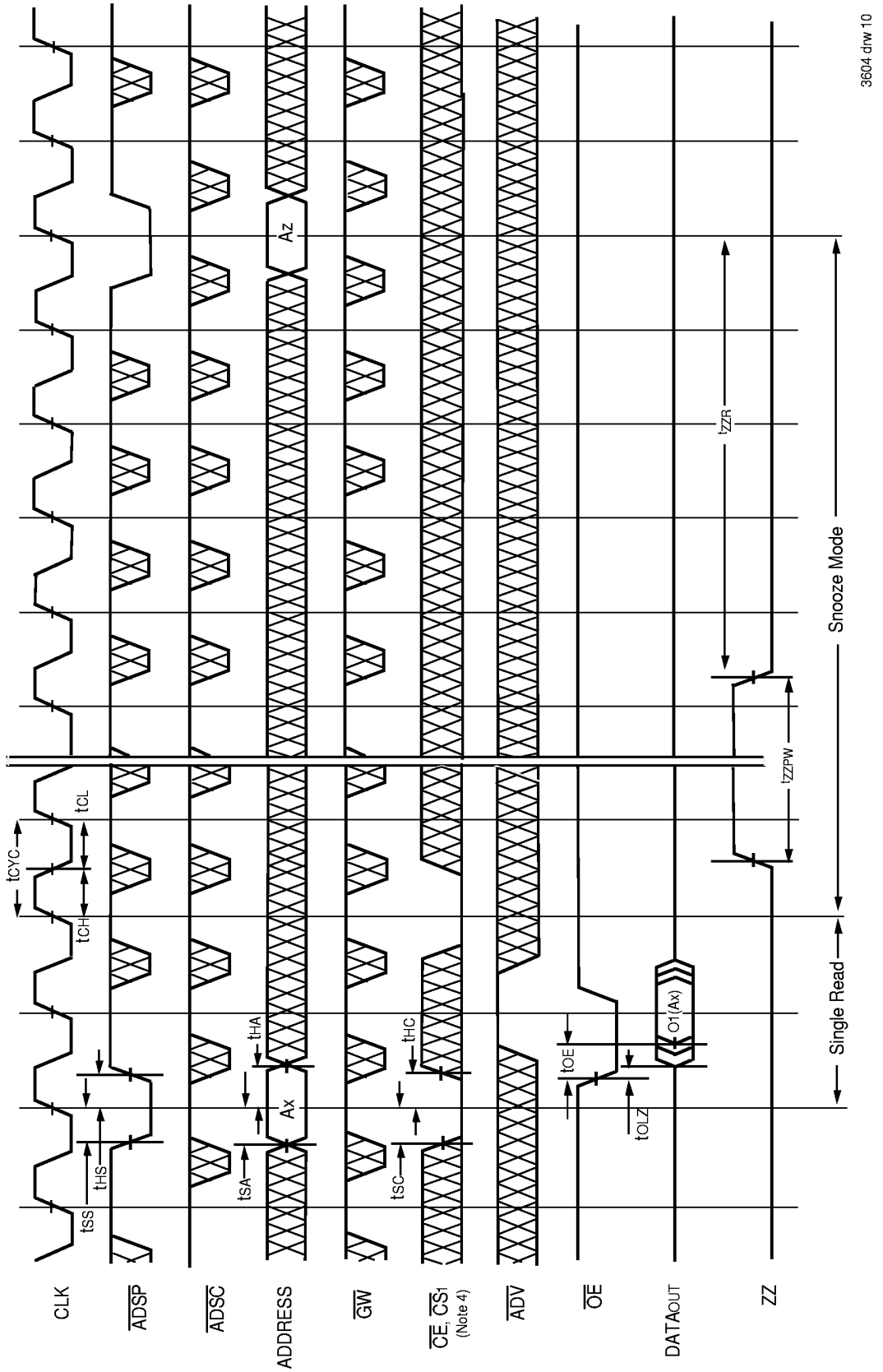
NOTES:
1. ZZ input is LOW, $\overline{BWE}$ is HIGH, and $\overline{LBO}$ is Don't Care for this cycle.
2. O1 (Ax) represents the first output from the external address Ax. O1 (Ay) represents the first output from the external address Ay; O2 (Ay) represents the next output data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.
3. $\overline{CS}_0$ timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS}_1$ signals. For example, when $\overline{CE}$ and $\overline{CS}_1$ are LOW on this waveform, $\overline{CS}_0$ is HIGH.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 - BYTE CONTROLLED(1, 2, 3)



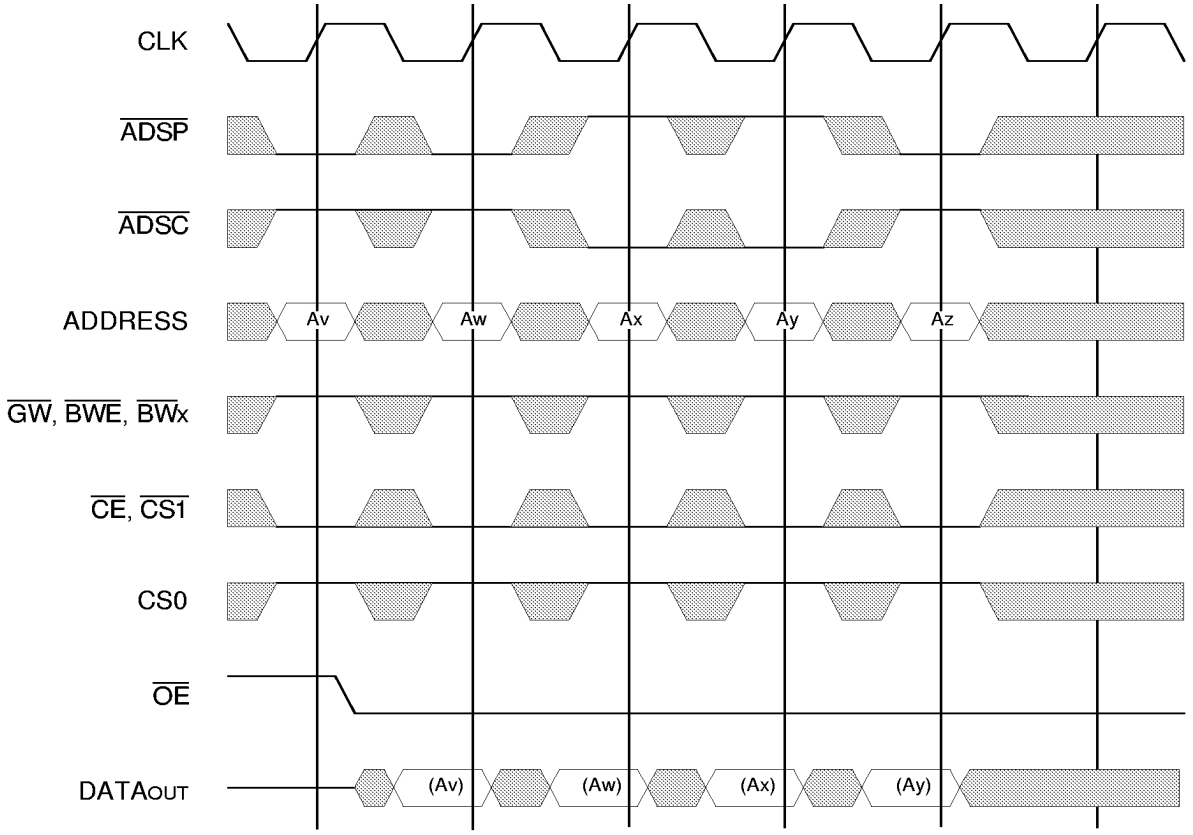
NOTES:
1. ZZ input is LOW, $\overline{GW}$ is HIGH, and $\overline{LBO}$ is Don't Care for this cycle.
2. O1 (Ax) represents the first output from the external address Ax. O1 (Ay) represents the first output from the external address Ay; O2 (Ay) represents the next output data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.
3. CS_0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS_1}$ signals. For example, when $\overline{CE}$ and $\overline{CS_1}$ are LOW on this waveform, CS_0 is HIGH.

TIMING WAVEFORM OF SLEEP (ZZ) AND POWER-DOWN MODES(1, 2, 3)



NOTES:
1. ZZ input is LOW, $\overline{GW}$ is HIGH, and $\overline{LBO}$ is Don't Care for this cycle.
2. O1 (Ax) represents the first output from the external address Ax. O1 (Ay) represents the first output from the external address Ay; O2 (Ay) represents the next output data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.
3. CS_0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS}_1$ signals. For example, when $\overline{CE}$ and $\overline{CS}_1$ are LOW on this waveform, CS_0 is HIGH.

NON-BURST READ CYCLE TIMING WAVEFORM



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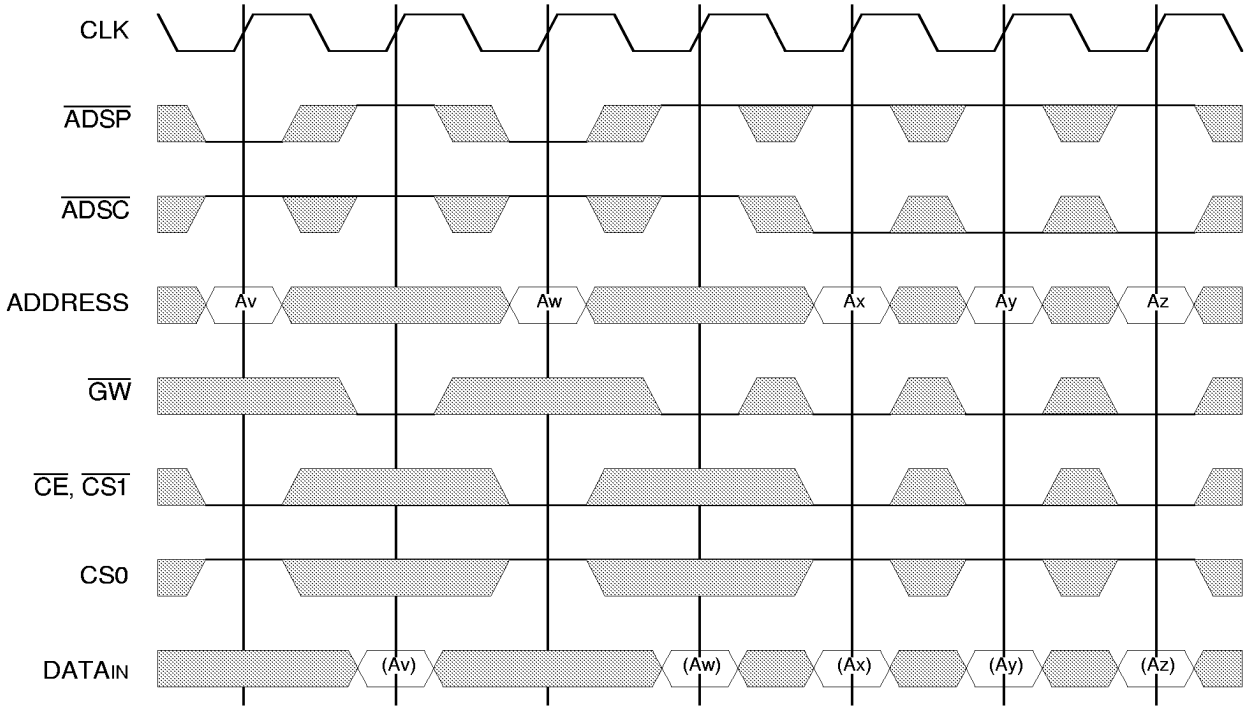
NOTES:
1. ZZ input is LOW, ADV is HIGH, and LBO is Don't Care for this cycle.
2. (Ax) represents the data for address Ax, etc.
3. For read cycles, ADSP and ADSC function identically and are therefore interchangable.

NON-BURST WRITE CYCLE TIMING WAVEFORM



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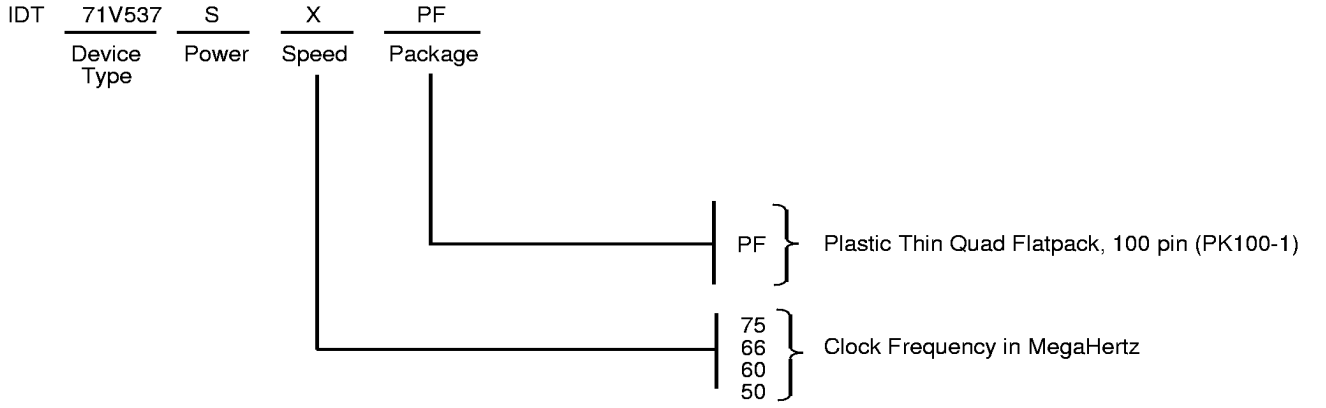
NOTES:
1. ZZ input is LOW, ADV and OE are HIGH, and LBO is Don't Care for this cycle.
2. (Ax) represents the data for address Ax, etc.
3. Although only GW writes are shown, the functionality of BWE and BWx together is the same as GW.
4. For write cycles, ADSP and ADSC have different limitations.

ORDERING INFORMATION



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