Chapter 15
Specifications

This chapter describes the electrical specifications for the LSI Logic L64360 chip, based upon the ATMizer Architecture.

This chapter has four sections:

- Section 15.1, "AC Timing"
- Section 15.2, "Electrical Requirements"
- Section 15.3, "Pin Summary"
- Section 15.4, "Pinout, Pin List, and Package Information"

15.1 AC Timing

This section specifies the AC timing characteristics of the L64360. The relationship between various signals is depicted in Figures 15.3 through 15.9. The figures depict:

- Secondary Port Timing
- Host/DMA Port Timing 1
- Host/DMA Port Timing 2
- Transmitting Cell Timing
- ACI Transmitter TX_IDLE Timing
- Received Cell Timing
- ACI Receiver RC_FULL Timing

Table 15.1 shows AC timing values specified for 70 pF loading. The numbers in Figures 15.3 through 15.9 refer to the AC timing parameters listed in Table 15.1.

The L64360 was designed using LSI Logic's LEA300K process.

During AC testing, HIGH inputs are driven at V_{DD}, and LOW inputs are driven at 0 V. For transitions between HIGH, LOW, and invalid states, timing measurements are made at 1.5 V, as shown in Figure 15.1.

For 3-state outputs, timing measurements are made from the point at which the output turns ON or OFF. An output is ON when its voltage is greater than 3.5 V or less than 1.5 V. An output is OFF when its voltage is less than V_{DD} – 1.5 V or greater than 1.5 V, as shown in Figure 15.2.

Figure 15.1
AC Test Load and Waveform for Standard Outputs

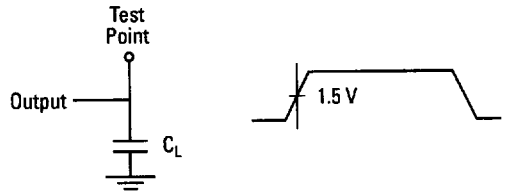


Figure 15.2
AC Test Load and Waveform for 3-State Outputs

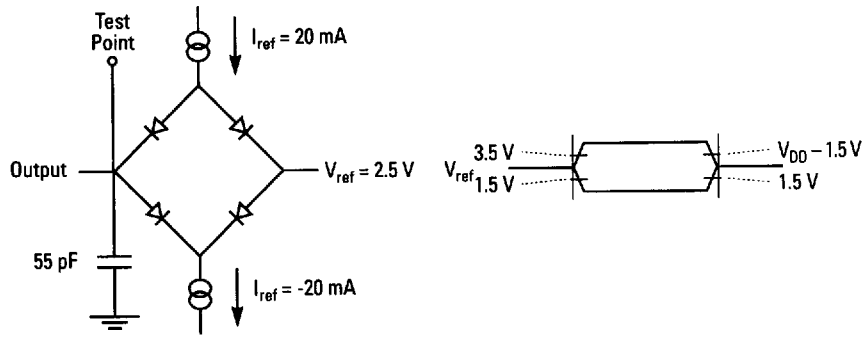


Table 15.1
AC Timing Values for
70-pF Loading (in ns)

		50 MHz		40 MHz		33 MHz		25 MHz	
	Description	***Min***	***Max***	***Min***	***Max***	***Min***	***Max***	***Min***	***Max***
1	CLK High/Low Time	9.6		12		14		17	
2	Output Delay from Rising CLK to SP_RQ High or Low		14		16		17		17
3	Output Delay from Rising CLK to SP_WR Valid		13		15		16		16
4	Output Delay from SP_GNT High to SP_AD[31:0] Address Valid		11		13		14		14
5	Output Delay from SP_ASEL Low to SP_AD[31:0] Data Valid for Write		11		13		14		14
6	Output Delay from SP_ASEL Low to SP_AD[31:0] 3-State for Read		11		13		14		14
7	Input Setup from $\overline{\text{SP\_ACK}}$ Low to Rising CLK	3		5		5		6	
8	Input Setup from $\overline{\text{SP\_BWIDE}}$ Low to Rising CLK	3		5		5		6	
9	Input Setup from SP_AD[31:0] Data Valid to Rising CLK for Read	6		8		8		9	
10	Input Hold from Rising CLK to SP_AD[31:0] Data Invalid for Read	2		3		3		4	
11	Output Delay from Rising CLK to HBS_RQ High		11		13		14		14
12	Output Delay from Rising CLK to HBS_WR Valid		15		17		18		18
13	Output Delay from Rising CLK to $\overline{\text{HBS\_AS}}$ Low		15		17		18		18
14	Output Delay from Rising CLK to $\overline{\text{HBS\_END}}$ Low		15		17		18		18
15	Output Delay from Rising CLK to HBS_A[31:2] Valid		15		17		18		18
16	Output Delay from Rising CLK to HBS_D[31:0] Valid for Write		15		17		18		18
17	Output Delay from Rising CLK to $\overline{\text{HBS\_BE}}$[3:0] Valid		15		17		18		18
18	Output Delay from Rising CLK to HBS_S[2:0] Valid		15		17		18		18
19	Output Delay from Rising CLK to HBS_WR 3-State		13		15		16		16
20	Output Delay from Rising CLK to $\overline{\text{HBS\_AS}}$ 3-State		13		15		16		16
21	Output Delay from Rising CLK to $\overline{\text{HBS\_END}}$ 3-State		13		15		16		16
22	Output Delay from Rising CLK to HBS_A[31:2] 3-State		14		16		17		17
23	Output Delay from Rising CLK to HBS_D[31:0] 3-State for Write		14		16		17		17

(Sheet 1 of 3)

Table 15.1 (Cont.)
AC Timing Values for
70-pF Loading (in ns)

		50 MHz		40 MHz		33 MHz		25 MHz	
	Description	***Min***	***Max***	***Min***	***Max***	***Min***	***Max***	***Min***	***Max***
24	Output Delay from Rising CLK to $\overline{\text{HBS\_BE}}$[3:0] 3-State		14		16		17		17
25	Output Delay from Rising CLK to HBS_S[2:0] 3-State		14		16		17		17
26	Input Setup from HBS_GNT High to Rising CLK	3		5		5		6	
27	Input Setup from $\overline{\text{HBS\_ACK}}$ Low to Rising CLK	7		9		9		10	
28	Input Setup from HBS_D[31:0] Valid to Rising CLK	4		6		6		7	
29	Input Hold from Rising CLK to HBS_GNT Low	2		3		3		4	
30	Input Hold from Rising CLK to $\overline{\text{HBS\_ACK}}$ Low	2		3		3		4	
31	Input Hold from Rising CLK to HBS_D[31:0] Invalid for Read	2		3		3		4	
32	Output Delay from HBS_AOE High to HBS_A[31:2] Valid		14		16		17		17
33	Output Delay from HBS_AOE Low to HBS_A[31:2] 3-State		14		16		17		17
34	Output Delay from HBS_DOE High to HBS_D[31:0] Valid for Write		14		16		17		17
35	Output Delay from HBS_DOE Low to HBS_D[31:0] 3-State for Write		14		16		17		17
36	Output Delay from Rising CLK to HBS_INT High		12		14		15		15
37	TX_CLK Cycle Time	40		50		60		80	
38	Output Delay from Rising TX_CLK to $\overline{\text{TX\_RST}}$ High		12		14		15		15
39	Output Delay from Rising TX_CLK to $\overline{\text{TX\_DRDY}}$ Low or High		9		11		12		12
40	Output Delay from Rising TX_CLK to TX_BOC High		13		15		16		16
41	Output Delay from Rising TX_CLK to TX_D[7:0] Valid		15		17		18		18
42	Input Setup from TX_ACK Valid to Rising TX_CLK	7		9		9		9	
43	Input Hold from Rising TX_CLK to TX_ACK Valid	1		2		2		3	
44	Input Setup from $\overline{\text{TX\_FULL}}$ Low to Rising TX_CLK	7		9		9		9	
45	Input Hold from Rising TX_CLK to $\overline{\text{TX\_FULL}}$ High	1		2		2		3	
46	Output Delay from Rising TX_CLK to TX_IDLE Valid		9		11		12		12
47	RC_CLK Cycle Time	40		50		60		80	
48	Output Delay from Rising RC_CLK to $\overline{\text{RC\_RST}}$ High		10		12		13		13

(Sheet 2 of 3)

Table 15.1 (Cont.)
AC Timing Values for
70-pF Loading (in ns)

		50 MHz		*40 MHz*		*33 MHz*		*25 MHz*	
	Description	***Min***	***Max***	***Min***	***Max***	***Min***	***Max***	***Min***	***Max***
49	Input Setup from RC_BOC High to Rising RC_CLK	7		9		9		10	
50	Input Setup from RC_ACK High or Low to Rising RC_CLK	7		9		9		10	
51	Input Setup from RC_D[7:0] Valid to Rising RC_CLK	7		9		9		10	
52	Input Hold from Rising RC_CLK to RC_D[7:0] Invalid	1		2		2		3	
53	Input Hold from Rising RC_CLK to RC_ACK Low or High	1		2		2		3	
54	Input Hold from Rising RC_CLK to RC_BOC Low	1		2		2		3	
55	Output Delay from Rising RC_CLK to HEC_ERR High		10		12		13		13
56	Output Delay from Rising RC_CLK to RC_FULL High or Low		10		12		13		13

(Sheet 3 of 3)

Figure 15.3
Secondary Port
Timing

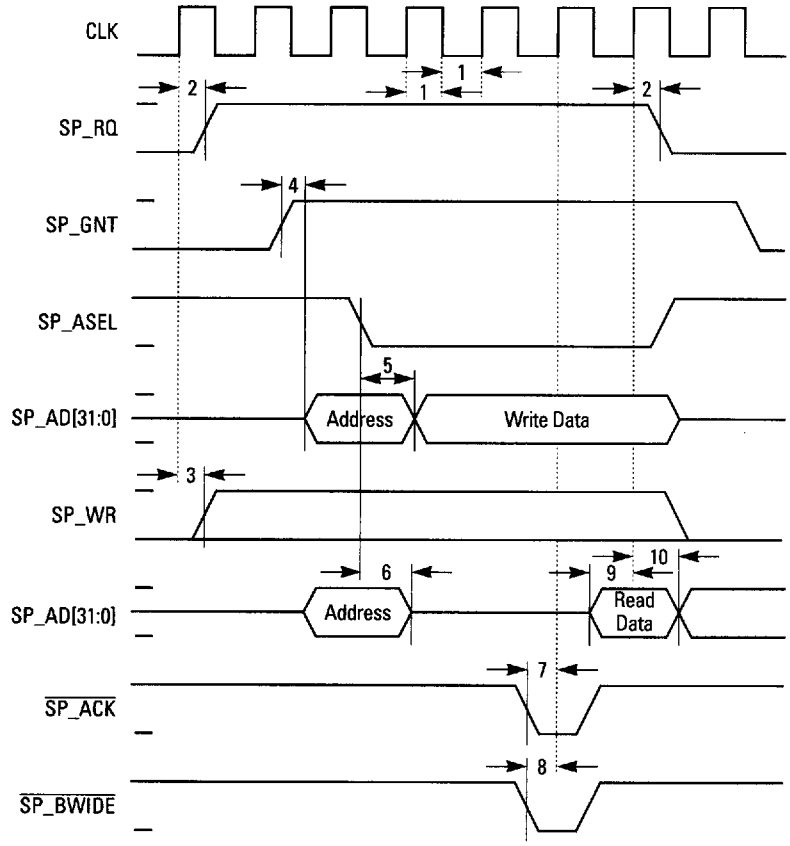


Figure 15.4
Host/DMA Port Timing 1

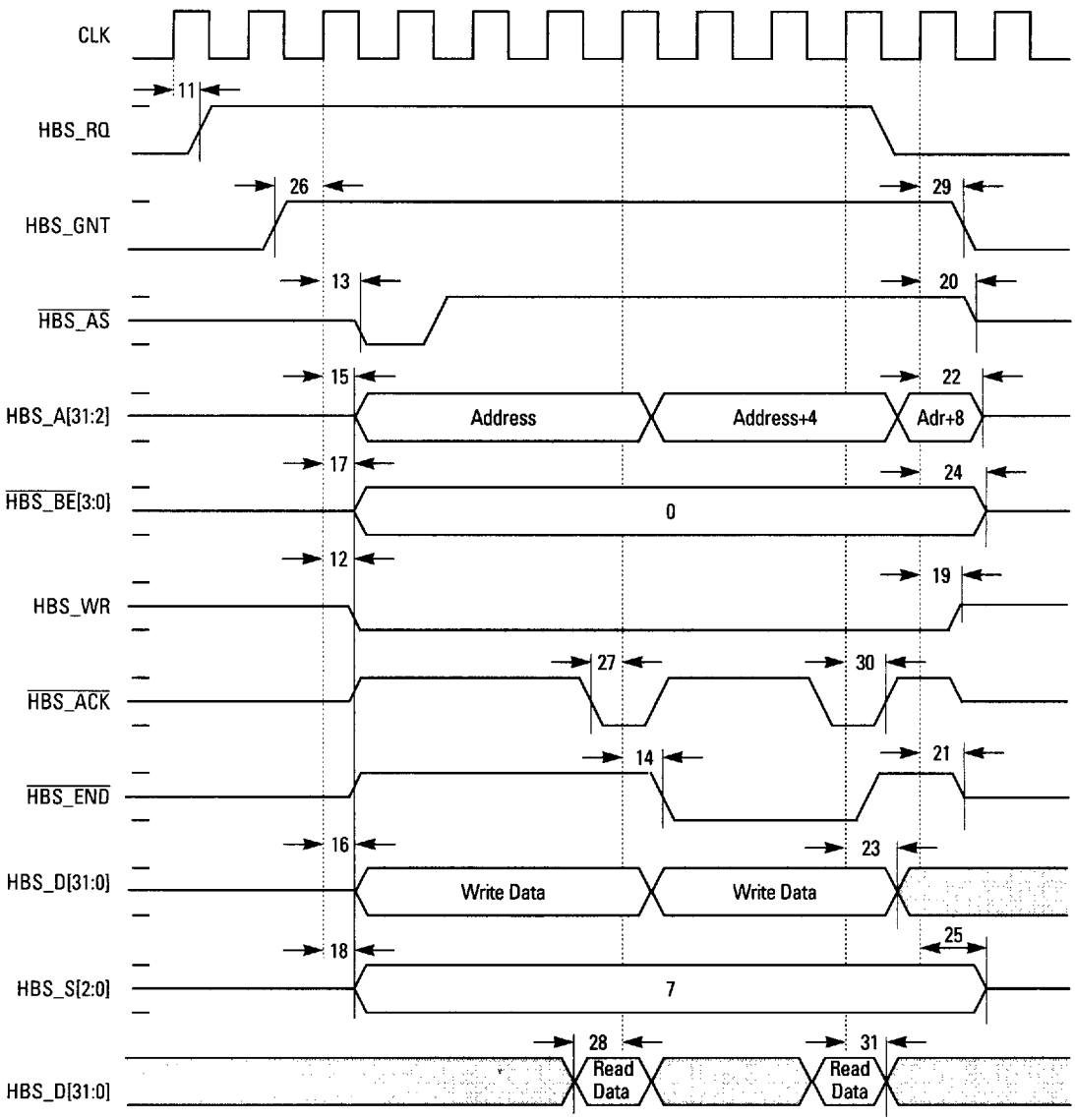


Figure 15.5
Host/DMA Port Timing 2

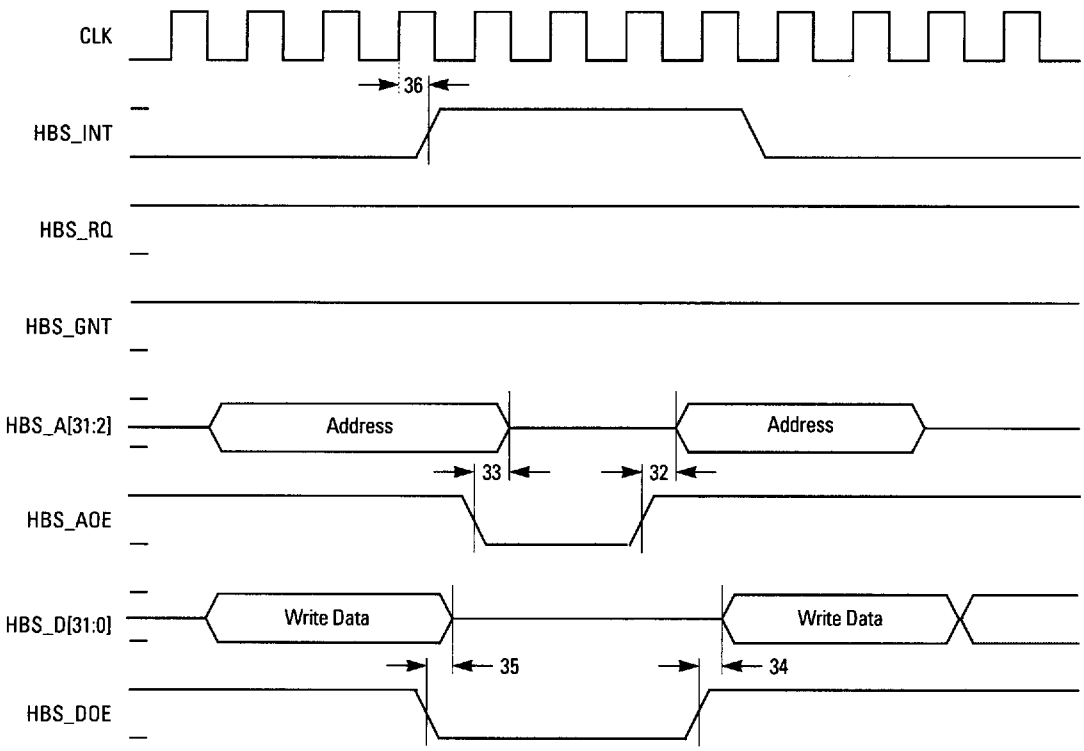


Figure 15.6
Transmitting Cell Timing

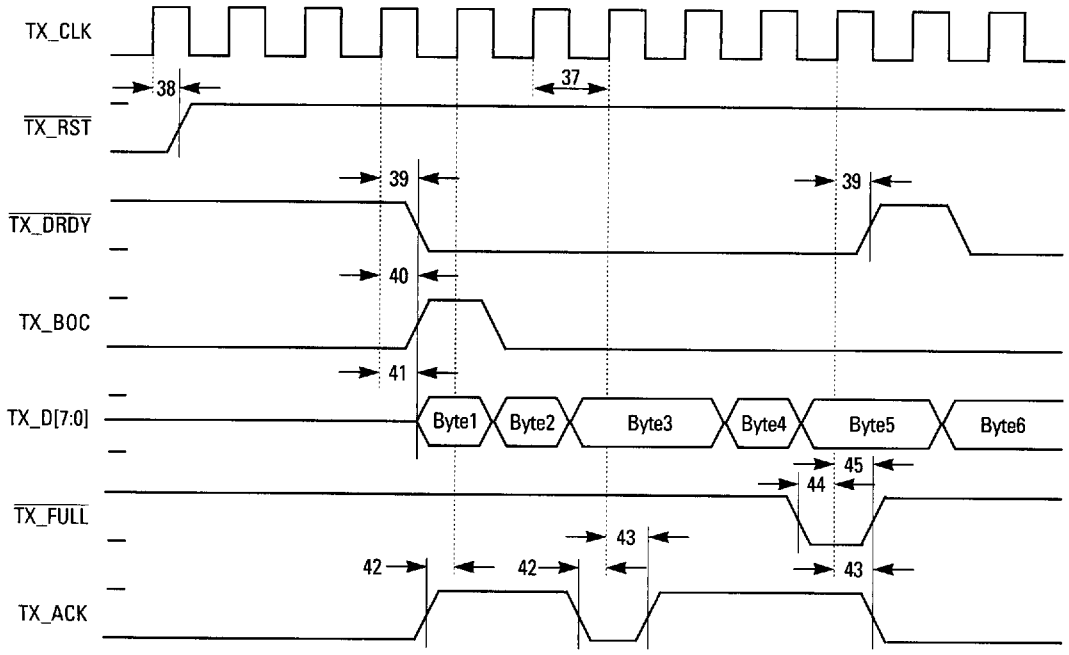


Figure 15.7
ACI Transmitter TX_IDLE Timing

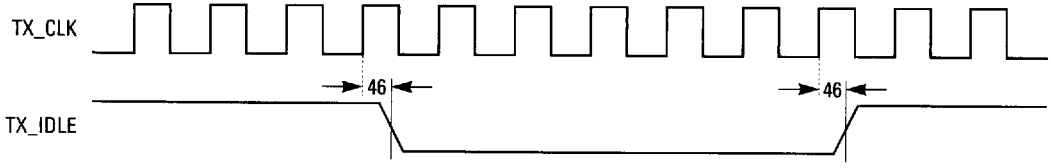


Figure 15.8
Received Cell Timing

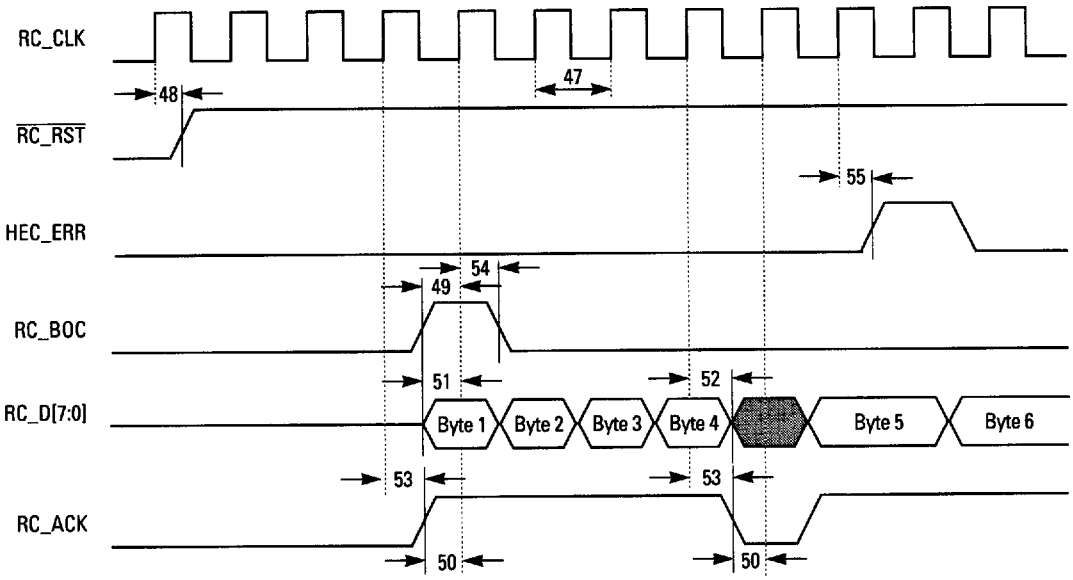
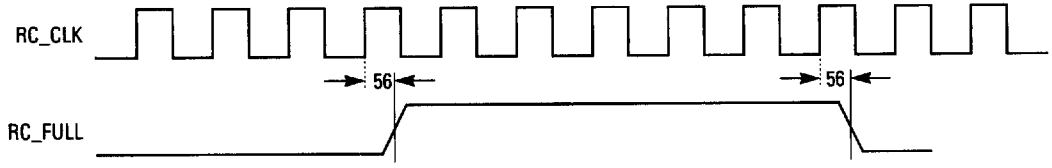


Figure 15.9
ACI Receiver RC_FULL Timing



15.2 Electrical Requirements

This section specifies the electrical requirements for the L64360. Five tables list electrical data in the following categories:

- Absolute Maximum Ratings
- Recommended Operating Conditions
- Worst Case Thermal Operating Conditions
- Capacitance
- DC Characteristics

Table 15.2 Absolute Maximum Ratings

Symbol	*Parameter*	*Limits*[1]	*Unit*
V_{DD}	DC Supply	-0.3 to +7.0	V
V_{IN}	Input Voltage	-0.3 to V_{DD} + 0.3	V
I_{IN}	DC Input Current	10	mA
T_{STG}	Storage Temperature Range, metal	0 to +125	°C

1. Referenced to V_{SS}.

Table 15.3 Recommended Operating Conditions

Symbol	*Parameter*	*Limits*	*Unit*
V_{DD}	DC Supply	+ 4.75 to +5.25	V
T_A	Ambient Temperature (50 MHz)	0 to 50	°C
T_A	Ambient Temperature (40 MHz and Below)	0 to 70	°C

Table 15.4 Worst Case Thermal Operating Conditions

Operating Speed	*Case Temperature*	*Unit*
50 MHz	0 to 85	°C
40 MHz and Below	0 to 100	°C

Table 15.5 Capacitance

Symbol	*Parameter*[1]	*Min*	*Typ*	*Max*	*Unit*
C_{IN}	Input Capacitance			5	pF
C_{OUT}	Output Capacitance			10	pF
C_{IO}	I/O Bus Capacitance			15	pF

1. Measurement conditions are V_{IN} = 5.0 V, T_A = 25° C, and clock frequency = 1 MHz.

Table 15.6 DC Characteristics

Symbol	*Parameter*	*Condition*[1]	*Min*	*Typ*	*Max*	*Units*
V_{IL}	Voltage Input Low		–	–	0.8	V
V_{IH}	Voltage Input High		2.0	–	–	V
V_{OH}	Voltage Output High	I_{OH} = -4.0 mA	2.4	4.5	–	V
		I_{OH} = -8.0 mA	2.4	4.5	–	V
V_{OL}	Voltage Output Low	I_{OL} = 4.0 mA	–	0.2	0.4	V
		I_{OL} = 8.0 mA	–	0.2	0.4	V
I_{IL}	Current Input Leakage	V_{DD} = Max, V_{IN} = V_{DD} or V_{SS}	-10	±1	10	µA

Table 15.6 (Cont.)
DC Characteristics

Symbol	*Parameter*	*Condition*[1]	*Min*	*Typ*	*Max*	*Units*
I_{OZ}	Current 3-State Output Leakage	V_{DD} = Max, V_{OUT} = V_{SS} or V_{DD}	-10	±1	10	µA
I_{IPU}	Current Input Pull-up	V_{IN} = V_{SS}	-35	-115	-350	µA
I_{OZU}	Current 3-State Output w/Pull-up	V_{IN} = V_{SS}	-2	–	-175	µA
I_{DD}	Quiescent Supply Current	V_{IN} = V_{DD} or V_{SS}	–	–	100	µA
I_{CC}	Dynamic Supply Current	V_{DD} = Max, 25 MHz	–	–	480	mA
		V_{DD} = Max, 33 MHz	–	–	550	mA
		V_{DD} = Max, 40 MHz	–	–	650	mA
		V_{DD} = Max, 50 MHz	–	–	750	mA

1. Specified at V_{DD} = 5 ± 5% at ambient temperature over the ranges specified in Table 15.3.

15.3 Pin Summary

Table 15.7 summarizes the L64360 pins. The table provides the drive capacity of the outputs and the signal types for both output and input pins.

Table 15.7
L64360 Pin Description Summary

Mnemonic	*Description*	*Type*	*Drive (mA)*	*Active*
$\overline{\text{CLK}}$	System Clock	Input	4	–
GPINT_AUTO	General Purpose APU Interrupt	Input	4	High
GPINT_TST	L64360 Interrupt	Input	4	High
HBS_A[31:2]	Host/DMA Port Address Bus	Output	4	–
$\overline{\text{HBS\_ACK}}$	Host/DMA Port Data Acknowledgment	Input	4	Low
HBS_AOE	Host/DMA Port Address Output Enable	Input	4	High
$\overline{\text{HBS\_AS}}$	Host/DMA Port Address Strobe	Output	4	Low
$\overline{\text{HBS\_BE}}$[3:0]	Host/DMA Port Byte Enables	Output	4	Low
HBS_BOOT	Host/DMA Port Boot Select	Input	4	High
HBS_D[31:0]	Host/DMA Port Data Bus	Bidirectional	4	–
HBS_DOE	Host/DMA Port Output Enable	Input	4	High
$\overline{\text{HBS\_END}}$	Host/DMA Port Operation Ending	Output	4	Low
HBS_GNT	Host/DMA Port Grant Operation	Input	4	High
HBS_INT	Host Interrupt	Output	4	High
HBS_RQ	Host/DMA Port Operation Request	Output	4	High
HBS_S[2:0]	Host/DMA Port DMA Transfer Size	Output	4	–
HBS_WR	Host/DMA Port Operation Type	Output	4	–
HEC_ERR	HEC Error	Output	4	High
PRU_CLK	Pacing Rate Unit Clock	Input	4	–
RC_ACK	ACI Receiver Data Acknowledge	Input	4	High

(Sheet 1 of 2)

Table 15.7 (Cont.) L64360 Pin Description Summary

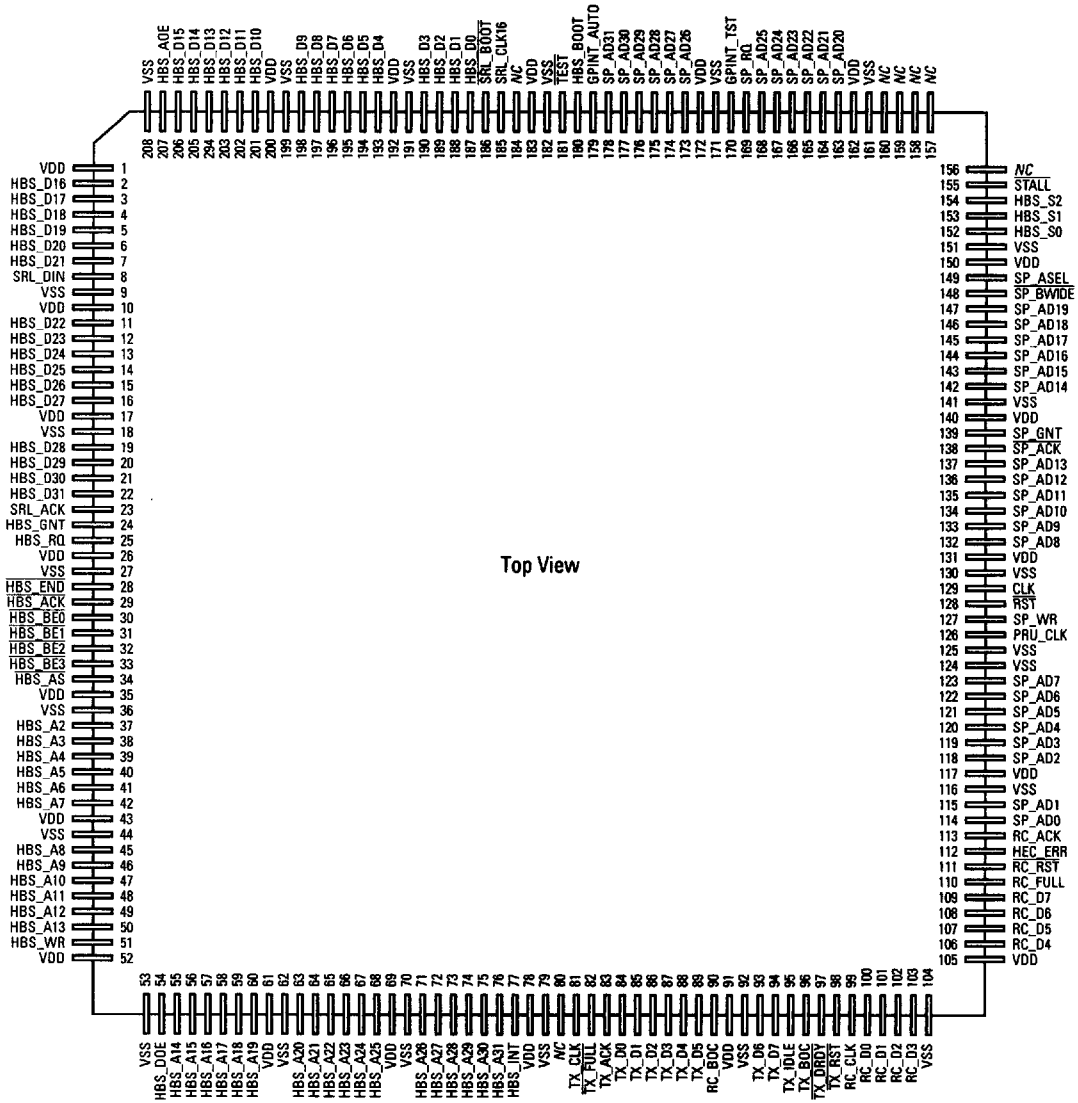
Mnemonic	*Description*	*Type*	*Drive (mA)*	*Active*
RC_BOC	ACI Receiver Beginning of Cell	Input	4	High
RC_CLK	ACI Receiver Clock	Input	4	–
RC_D[7:0]	ACI Receiver Data Bus	Input	4	–
RC_FULL	ACI Receiver Cell Holder Buffer Full	Output	4	High
$\overline{\text{RC\_RST}}$	ACI Receiver Reset	Output	4	Low
$\overline{\text{RST}}$	System Reset	Input	4	Low
SP_ACK	Secondary Port Data Acknowledge	Input	4	High
SP_AD[31:0]	Secondary Port Address/Data Bus	Bidirectional	4	–
SP_ASEL	Secondary Port Address/Data Select	Input	4	High
$\overline{\text{SP\_BWIDE}}$	Secondary Port Byte-wide Device	Input	4	Low
SP_GNT	Secondary Port Bus Grant	Input	4	High
SP_RQ	Secondary Port Access Request	Output	4	High
SP_WR	Secondary Port Operation Type	Output	4	High
$\overline{\text{STALL}}$	APU Pipeline Stall	Output	4	Low
SRL_ACK	Serial Acknowledge	Input	4	High
$\overline{\text{SRL\_BOOT}}$	Serial Boot Select	Input	4	Low
SRL_CLK16	Serial Clock	Output	4	–
SRL_DIN	Serial Data Input	Input	4	–
$\overline{\text{TEST}}$	Test Mode	Input	4	Low
TX_ACK	ACI Transmitter Data Acknowledge	Input	4	High
TX_BOC	ACI Transmitter Beginning of Cell	Output	4	High
TX_CLK	ACI Transmitter Clock	Input	4	–
TX_D[7:0]	ACI Transmitter Data Bus	Output	4	–
$\overline{\text{TX\_DRDY}}$	ACI Transmitter Data Ready	Output	4	Low
$\overline{\text{TX\_FULL}}$	ACI Transmitter Buffer Full	Input	4	Low
TX_IDLE	ACI Transmitter Idle Cell	Output	4	High
$\overline{\text{TX\_RST}}$	ACI Transmitter Reset	Output	4	Low

(Sheet 2 of 2)

15.4 Pinout, Pin List, and Package Information

The LSI Logic L64360 ASSP is available in a 208-pin, cavity down, metal quad flat package (MQUAD). Figure 15.10 illustrates the pinout of the 208-pin package, and Figure 15.11 is the mechanical drawing. Table 15.8 shows the L64360 pin list.

Figure 15.10
208-Pin MQUAD Pinout –
Cavity Down



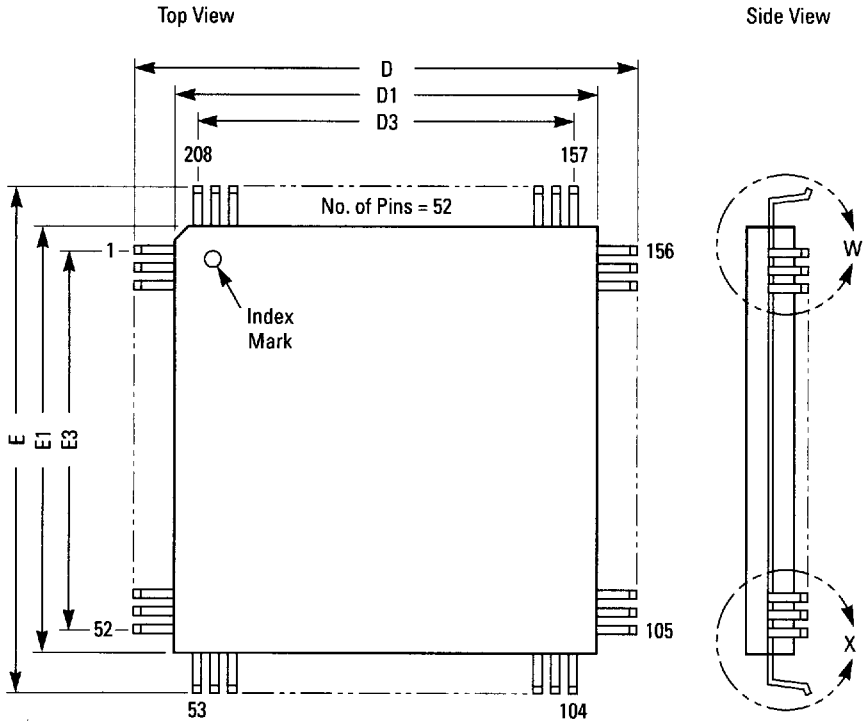
Note:
1. *NC* pins are not connected.

Table 15.8
L64360 Pin List

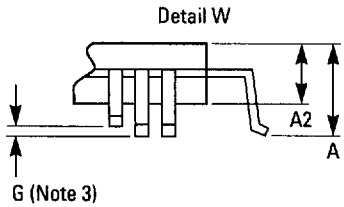
Signal	*Pin*	*Signal*	*Pin*	*Signal*	*Pin*	*Signal*	*Pin*	*Signal*	*Pin*
CLK	129	HBS_D30	21	*NC*	156	SP_AD11	135	VDD	35
GPINT_AUTO	179	HBS_D29	20	*NC*	157	SP_AD10	134	VDD	43
GPINT_TST	170	HBS_D28	19	*NC*	158	SP_AD9	133	VDD	52
HBS_A31	76	HBS_D27	16	*NC*	159	SP_AD8	132	VDD	61
HBS_A30	75	HBS_D26	15	*NC*	160	SP_AD7	123	VDD	69
HBS_A29	74	HBS_D25	14	*NC*	184	SP_AD6	122	VDD	78
HBS_A28	73	HBS_D24	13	PRU_CLK	126	SP_AD5	121	VDD	91
HBS_A27	72	HBS_D23	12	RC_ACK	113	SP_AD4	120	VDD	105
HBS_A26	71	HBS_D22	11	RC_BOC	90	SP_AD3	119	VDD	117
HBS_A25	68	HBS_D21	7	RC_CLK	99	SP_AD2	118	VDD	131
HBS_A24	67	HBS_D20	6	RC_D7	109	SP_AD1	115	VDD	140
HBS_A23	66	HBS_D19	5	RC_D6	108	SP_AD0	114	VDD	150
HBS_A22	65	HBS_D18	4	RC_D5	107	SP_ASEL	149	VDD	162
HBS_A21	64	HBS_D17	3	RC_D4	106	$\overline{\text{SP\_BWIDE}}$	148	VDD	172
HBS_A20	63	HBS_D16	2	RC_D3	103	SP_GNT	139	VDD	183
HBS_A19	60	HBS_D15	206	RC_D2	102	SP_RQ	169	VDD	192
HBS_A18	59	HBS_D14	205	RC_D1	101	SP_WR	127	VDD	200
HBS_A17	58	HBS_D13	204	RC_D0	100	SRL_ACK	23	VSS	9
HBS_A16	57	HBS_D12	203	RC_FULL	110	$\overline{\text{SRL\_BOOT}}$	186	VSS	18
HBS_A15	56	HBS_D11	202	$\overline{\text{RC\_RST}}$	111	SRL_CLK16	185	VSS	27
HBS_A14	55	HBS_D10	201	$\overline{\text{RST}}$	128	SRL_DIN	8	VSS	36
HBS_A13	50	HBS_D9	198	$\overline{\text{SP\_ACK}}$	138	$\overline{\text{STALL}}$	155	VSS	44
HBS_A12	49	HBS_D8	197	SP_AD31	178	$\overline{\text{TEST}}$	181	VSS	53
HBS_A11	48	HBS_D7	196	SP_AD30	177	TX_ACK	83	VSS	62
HBS_A10	47	HBS_D6	195	SP_AD29	176	TX_BOC	96	VSS	70
HBS_A9	46	HBS_D5	194	SP_AD28	175	TX_CLK	81	VSS	79
HBS_A8	45	HBS_D4	193	SP_AD27	174	TX_D7	94	VSS	92
HBS_A7	42	HBS_D3	190	SP_AD26	173	TX_D6	93	VSS	104
HBS_A6	41	HBS_D2	189	SP_AD25	168	TX_D5	89	VSS	116
HBS_A5	40	HBS_D1	188	SP_AD24	167	TX_D4	88	VSS	124
HBS_A4	39	HBS_D0	187	SP_AD23	166	TX_D3	87	VSS	125
HBS_A3	38	HBS_DOE	54	SP_AD22	165	TX_D2	86	VSS	130
HBS_A2	37	$\overline{\text{HBS\_END}}$	28	SP_AD21	164	TX_D1	85	VSS	141
$\overline{\text{HBS\_ACK}}$	29	HBS_GNT	24	SP_AD20	163	TX_D0	84	VSS	151
HBS_AOE	207	HBS_INT	77	SP_AD19	147	$\overline{\text{TX\_DRDY}}$	97	VSS	161
$\overline{\text{HBS\_AS}}$	34	HBS_RQ	25	SP_AD18	146	$\overline{\text{TX\_FULL}}$	82	VSS	171
$\overline{\text{HBS\_BE3}}$	33	HBS_S2	154	SP_AD17	145	TX_IDLE	95	VSS	182
$\overline{\text{HBS\_BE2}}$	32	HBS_S1	153	SP_AD16	144	$\overline{\text{TX\_RST}}$	98	VSS	191
$\overline{\text{HBS\_BE1}}$	31	HBS_S0	152	SP_AD15	143	VDD	1	VSS	199
$\overline{\text{HBS\_BE0}}$	30	HBS_WR	51	SP_AD14	142	VDD	10	VSS	208
HBS_BOOT	180	HEC_ERR	112	SP_AD13	137	VDD	17		
HBS_D31	22	*NC*[1]	80	SP_AD12	136	VDD	26		

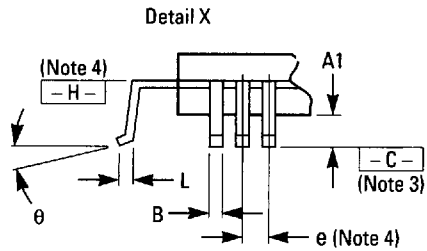
1. NC pins are not connected.

Figure 15.11
208-Pin MQUAD
Mechanical Drawing



Dimension		mm
A	Max	3.86
A1	Min	0.25
	Max	0.51
A2	Min	3.17
	Max	3.43
B	Typ	0.23
D	Min	30.40
	Max	30.80
D1	Min	27.56
	Max	27.72
D3	BSC	25.50
E	Min	30.40
	Max	30.80
E1	Min	27.56
	Max	27.72
E3	BSC	25.50
θ	Min	0°
	Max	7°
e	BSC	0.50
G	Max	0.10
L	Min	0.40
	Max	0.60





Note:
1. Total number of pins is 208.
2. Drawing is not to scale.
3. Coplanarity of all leads shall be within 0.10 mm (difference between the highest and lowest lead with seating plane – C – as reference).
4. Lead pitch determined at – H –.
5. Leadframe to package offset tolerance is ±0.10 mm Max.
6. For board layout and manufacturing, you may obtain engineering drawings from your LSI Logic Products marketing representative by requesting the outline drawing for package code WV.

MD92.WVa