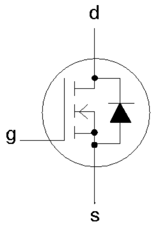
FEATURES

- '**Trench**' technology
- Low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

$V_{DSS} = 100$ V

$I_D = 6$ A

$R_{DS(ON)} \leq 0.1\ \Omega$

GENERAL DESCRIPTION

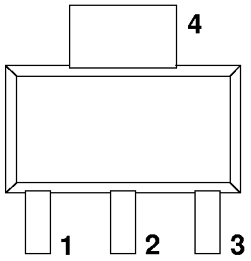
N-channel enhancement mode field-effect power transistor in a plastic envelope using '**trench**' technology. The device has very low on-state resistance. It is intended for use in dc to dc converters and general purpose switching applications.

The PHN6N10T is supplied in the SOT223 surface mounting package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

SOT223



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 ˚C to 175˚C	-	100	V
V_{DGR}	Drain-gate voltage	T_j = 25 ˚C to 175˚C; R_{GS} = 20 kΩ	-	100	V
V_{GS}	Gate-source voltage		-	± 20	V
I_D	Continuous drain current	T_{sp} = 25 ˚C	-	6	A
		T_{sp} = 100 ˚C	-	3.8	A
		T_{amb} = 25 ˚C	-	2.8	A
I_{DM}	Pulsed drain current	T_{sp} = 25 ˚C	-	24	A
P_D	Total power dissipation	T_{sp} = 25 ˚C	-	8.3	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	150	˚C

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_{AS} = 6 A; t_p = 0.2 ms; T_j prior to avalanche = 25˚C; $V_{DD} \leq 25$ V; R_{GS} = 50 Ω; V_{GS} = 10 V	-	78	mJ
I_{AS}	Non-repetitive avalanche current		-	6	A

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}sp}$	From junction to solder point	Mounted on any PCB	12	15	K/W
$R_{th\ j\text{-}amb}$	From junction to ambient	mounted on pcb of fig:1	70	-	K/W

ELECTRICAL CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	100	-	-	V
		T_j = -55˚C	95	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2	3	4	V
		T_j = 150˚C	1.2	-	-	V
		T_j = -55˚C	-		4.4	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 3 A	-	90	100	mΩ
		V_{GS} = 10 V; I_D = 3 A; T_j = 150˚C	-	-	270	mΩ
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V;	-	1	25	µA
		V_{DS} = 80 V; V_{GS} = 0 V; T_j = 150˚C	-	4	250	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	10	100	nA
$Q_{g(tot)}$	Total gate charge	I_D = 6 A; V_{DD} = 80 V; V_{GS} = 10 V	-	20	26	nC
Q_{gs}	Gate-source charge		-	3	5	nC
Q_{gd}	Gate-drain (Miller) charge		-	8	11	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 50 V; R_D = 8.2 Ω;	-	10	-	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 10 Ω	-	30	-	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	20	-	ns
t_f	Turn-off fall time		-	30	-	ns
L_d	Internal drain inductance	Measured tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	670	-	pF
C_{oss}	Output capacitance		-	250	-	pF
C_{rss}	Feedback capacitance		-	60	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{sp} = 25 ˚C	-	-	6	A
I_{SM}	Pulsed source current (body diode)		-	-	24	A
V_{SD}	Diode forward voltage	I_F = 6 A; V_{GS} = 0 V	-	0.8	1.5	V
t_{rr}	Reverse recovery time	I_F = 6 A; -dI_F/dt = 100 A/µs;	-	150	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 25 V	-	0.85	-	µC

PRINTED CIRCUIT BOARD

Dimensions in mm.

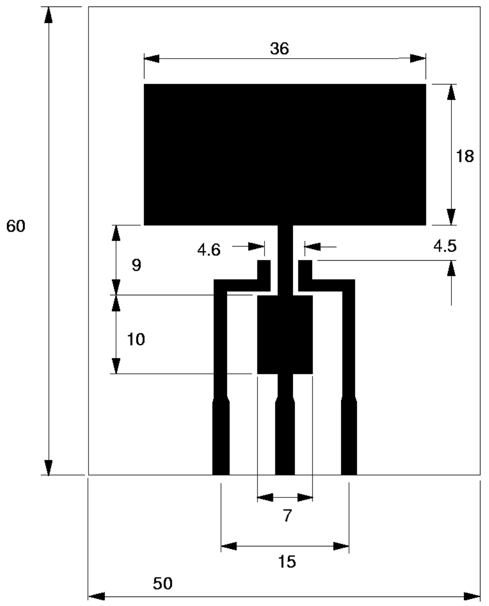


Fig.1. PCB for thermal resistance and power rating for SOT223.
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 µm thick).

MECHANICAL DATA

Dimensions in mm

Net Mass: 0.11 g

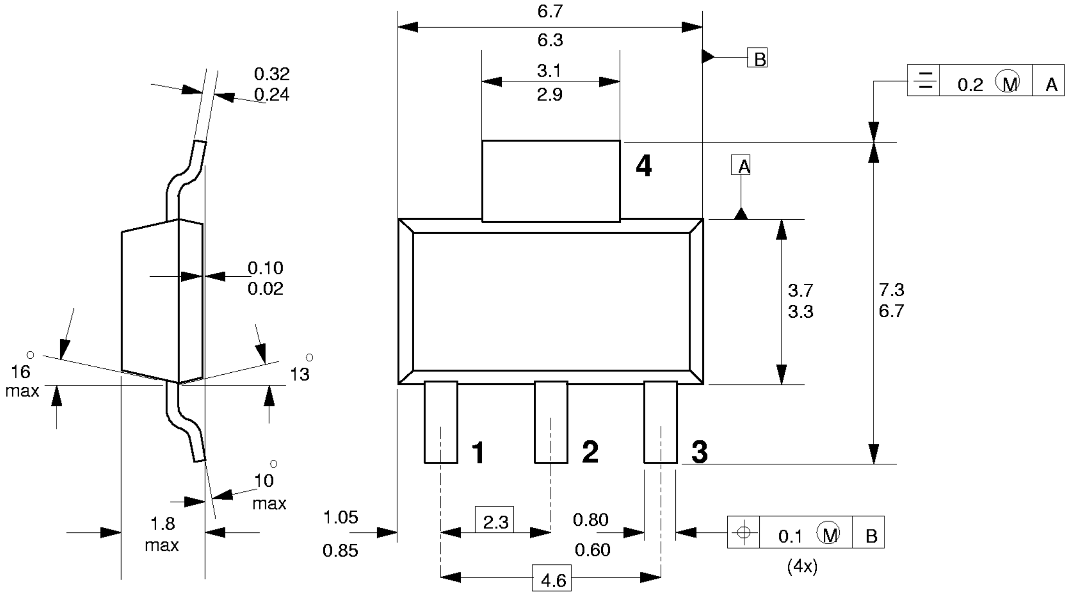


Fig.2. SOT223 surface mounting package.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to surface mounting instructions for SOT223 envelope.
3. Epoxy meets UL94 V0 at 1/8".