PRELIMINARY DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD720200

USB 3.0 HOST CONTROLLER

The μPD720200 is the Universal Serial Bus 3.0 host controller, which complies with Universal Serial Bus 3.0 Specification, and Intel's eXtensible Host Controller Interface (xHCI).

The μPD720200 has PCI Express® bus interface, and it is applicable for PCI Express solution for host PC system. The μPD720200 works up to 5 Gbps for data transfer when connecting to USB 3.0 compliant peripherals, while maintaining compatibility with existing USB peripheral devices.

Detailed function descriptions are provided in the following user's manual. Be sure to read the manual before designing.

μPD720200 User's Manual : TBD

★ FEATURES

- Compliant with Universal Serial Bus 3.0 specification Revision 1.0, which is released by USB Implementers Forum, Inc
  - Supports the following speed data rate as follows;
    Low-speed (1.5 Mbps) / Full-speed (12 Mbps) / High-speed (480 Mbps) / Super-speed (5 Gbps)
  - Supports 2 downstream ports for all speeds
  - Supports all USB compliant data transfer type as follows; Control / Bulk / Interrupt / Isochronous transfer
- Compliant with Intel's eXtensible Host Controller Interface (xHCI) Specification revision 0.95
- Support USB legacy function
- Compliant with PCI Express® Base Specification 2.0
- Supports ExpressCard™ Standard Release1.0
- Supports PCI Express® Card Electromechanical Specification Revision 2.0
- Supports PCI Bus Power Management Interface Specification revision 1.2
- Operational registers are direct-mapped to PCI memory space
- Supports Serial Peripheral Interface (SPI) type ROM
- System clock: 24 MHz crystal or 48MHz external clock.
- 3.3 V and 1.05 V power supply

ORDERING INFORMATION

Part Number	Package	Remark
μPD720200F1-DAK-A	176-pin plastic FBGA (10 × 10)	Lead-free product

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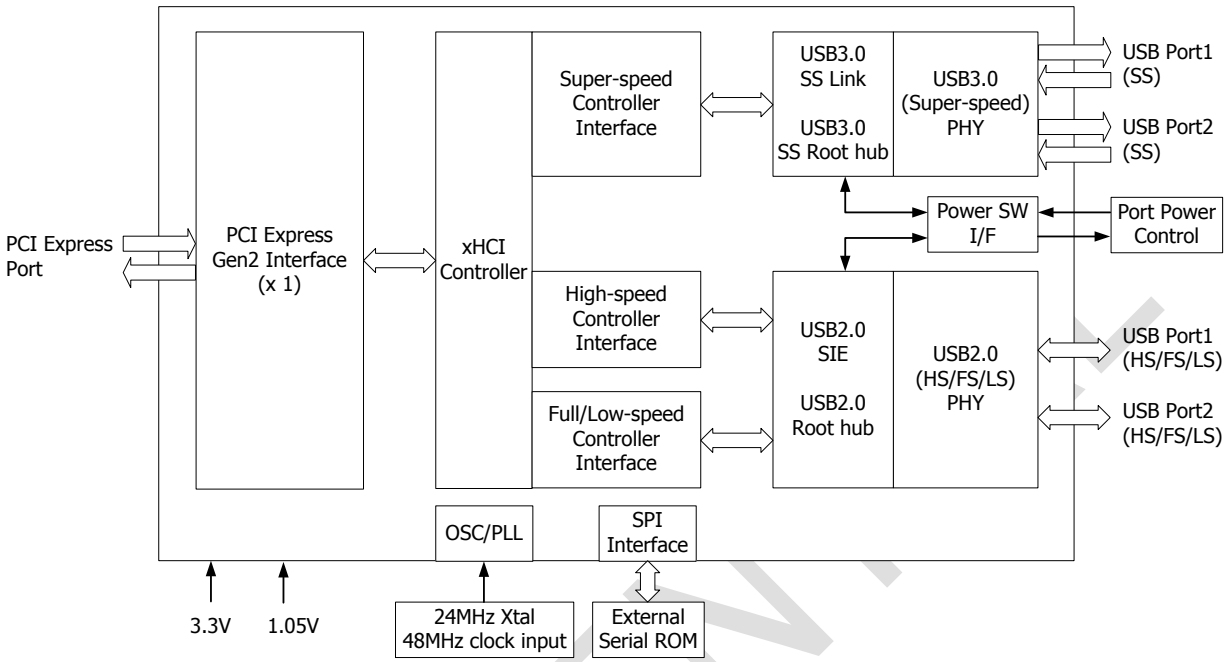
BLOCK DIAGRAM



PCI Express Gen2 Interface	: complies with PCI Express Gen2 interface, with 1 lane. This block includes link and PHY layer.
xHCI Controller	: handles all supped required for USB 3.0, super-/high-/full-/low-speed. This block includes register interface from system.
Super-speed Controller I/F	: handles super-speed operation in xHCI control block.
High-speed Controller I/F	: handles high-speed operation in xHCI control block.
Full/Low-speed Controller I/F	: handles full-/low-speed operation in xHCI control block.
USB3.0 SS Link	: is link layer defined in USB 3.0 specification, which maintains Link connectivity with USB devices.
USB3.0 SS Root hub	: is a hub function in host controller for USB 3.0 port managing.
USB3.0 PHY	: for super-speed Tx/Rx
USB2.0 SIE	: is Serial Interface Engine, which controls USB 2.0 protocol sequence.
USB2.0 Root hub	: is a hub function in host controller for USB 2.0 port managing.
USB2.0 PHY	: for high-/full-/low-speed Tx/Rx
Power SW I/F	: is connected to external power switch for port power control and over current detection.
SPI Interface	: is connected to external serial ROM.
PLL	: Internal PLL.
OSC	: Internal oscillator block.

PIN CONFIGURATION

- **176-pin plastic FBGA (10 × 10)**
  μPD720200F1-DAK-A

Bottom View

GND	GND	U3RXDN1	GND	U3TXDN1	GND	U3RXDN2	GND	U3TXDN2	GND	GND	GND	GND	GND	A
GND	GND	U3RXDP1	GND	U3TXDP1	GND	U3RXDP2	GND	U3TXDP2	GND	GND	GND	PECLKP	PECLKN	B
GND	GND	GND	GND	GND	VDD10	VDD10	VDD10	VDD10	VDD10	VDD10	GND	GND	GND	C
GND	GND	GND	GND	VDD33	VDD10	VDD10	U3AVDD33	U3AVSS	VDD10	GND	GND	PETXP	PETXN	D
GND	GND	VDD10	VDD10							VDD10	VDD10	GND	GND	E
VDD33	VDD33	GND	GND		GND	GND	GND	GND		GND	VDD33	PERXP	PERXN	F
OCI2B	GND	GND	GND		GND	GND	GND	GND		VDD33	VDD33	GND	GND	G
PPON2	OCI1B	GND	VDD10		GND	GND	GND	GND		VDD10	VDD10	PERSTB	SMIB	H
PPON1	GND	GND	GND		GND	GND	GND	GND		GND	GND	AUXDET	PSEL	J
GND	GND	VDD10	VDD10							GND	GND	PECREQB	PEWAKEB	K
VDD33	VDD33	GND	GND	VDD33	VDD33	VDD10	GND	GND	VDD10	GND	GND	GND	GND	L
XT2	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	SPISCK	SPISO	M
XT1	GND	U2AVSS	U2PVSS	U2DM1	GND	U2DM2	GND	VDD33	VDD33	VDD33	GND	SPICSB	SPISI	N
GND	U2AVDD33	RREF	GND	U2DP1	GND	U2DP2	GND	CSEL	PONRSTB	GND	VDD33	GND	GND	P
14	13	12	11	10	9	8	7	6	5	4	3	2	1	

1. PIN FUNCTIONS

This section describes each pin functions.

Power supply

Pin Name	Ball No.	Buffer Type	Function
V_{DD33}	D10, F3, F13, F14, G3, G4, L9, L10, L13, L14, N4, N5, N6, P3	Power	+3.3 V power supply
★ V_{DD10}	C4, C5, C6, C7, C8, C9, D5, D8, D9, E3, E4, E11, E12, H3, H4, H11, K11, K12, L5, L8	Power	+1.05 V power supply.
$U3AV_{DD33}$	D7	Power	+3.3 V power supply for analog circuit.
$U2AV_{DD33}$	P13	Power	+3.3 V power supply for analog circuit.
V_{SS}	A1, A2, A3, A4, A5, A7, A9, A11, A13, A14, B3, B4, B5, B7, B9, B11, B13, B14, C1, C2, C3, C10, C11, C12, C13, C14, D3, D4, D11, D12, D13, D14, E1, E2, E13, E14, F4, F6, F7, F8, F9, F11, F12, G1, G2, G6, G7, G8, G9, G11, G12, G13, H6, H7, H8, H9, H12, J3, J4, J6, J7, J8, J9, J11, J12, J13, K3, K4, K13, K14, L1, L2, L3, L4, L6, L7, L11, L12, M3, M4, M5, M6, M7, M8, M9, M10, M11, M12, M13, N3, N7, N9, N13, P1, P2, P4, P7, P9, P11, P14	Power	Ground.
$U3AV_{SS}$	D6	Power	Ground for USB3.0 analog circuit.
$U2AV_{SS}$	N12	Power	Ground for USB2.0 analog circuit
$U2PV_{SS}$	N11	Power	Ground for internal PLL.

The mark★ shows major revised points.

Analog Signal

Pin Name	Ball No.	Direction	Buffer Type	Active Level	Function
RREF	P12	—	Analog	—	Reference resistor connection.

System clock

Pin Name	Ball No.	Direction	Buffer Type	Active Level	Function
XT1	N14	I	OSC	–	Oscillator in During 24 MHz crystal mode, connect to 24 MHz crystal. In using external 48 MHz clock, this pin must be clamped to low.
XT2	M14	I/O	OSC	–	Oscillator out or external clock input During 24 MHz crystal mode, connect to 24 MHz crystal. In using external 48 MHz clock, this pin is used for external 48 MHz clock input signal..
CSEL	P6	I	3.3V Input	–	Clock select signal 0: 24 MHz crystal mode 1: 48 MHz external clock input

System Interface signal

Pin Name	Ball No.	Direction	Buffer Type	Active Level	Function
PONRSTB	P5	I	3.3V Schmitt Input	Low	Power on reset signal. When supporting wakeup from D3cold, this signal should be pulled high with system auxiliary power supply.
SMIB	H1	O	3.3V Output (6mA)	Low	System management Interrupt signal “SMI#”.

PCI express Interface

Pin Name	Ball No.	Direction	Buffer Type	Active Level	Function
PECLKP	B2	I	PCIE	—	PCI Express / USB3.0 100 MHz Reference Clock.
PECLKN	B1	I	PCIE	—	PCI Express / USB3.0 100 MHz Reference Clock.
PETXP	D2	O	PCIE	—	PCI Express Transmit Data.
PETXN	D1	O	PCIE	—	PCI Express Transmit Data.
PERXP	F2	I	PCIE	—	PCI Express Receive Data.
PERXN	F1	I	PCIE	—	PCI Express Receive Data.
PERSTB	H2	I	3.3V Schmitt Input	Low	PCI Express “PERST#” signal.
PEWAKEB	K1	O	Open Drain (6mA)	Low	PCI Express “WAKE#” signal. This signal is used for remote wakeup mechanism, and requests the recovery of power and reference clock input.
PECREQB	K2	O	Open Drain (6mA)	Low	PCI Express “CLKREQ#” signal. This signal is used to request run/stop of reference clock for ExpressCard or Mini Card.
AUXDET	J2	I	3.3V Input	High	Auxiliary Power detect signal. This signal should be connected to auxiliary power line, when system supports remote wakeup from D3cold.
PSEL	J1	I	3.3V Input	—	PCI Express/ExpressCard select signal. 1: Others 0: ExpressCard or Mini card

USB Interface

Pin Name	Ball No.	Direction	Buffer Type	Active Level	Function
U3TXDP (2:1)	B6, B10	O	USB3	—	USB3.0 Transmit data D+ signal for super-speed
U3TXDN (2:1)	A6, A10	O	USB3	—	USB3.0 Transmit data D- signal for super-speed
U3RXDP (2:1)	B8, B12	I	USB3	—	USB3.0 Receive data D+ signal for super-speed
U3RXDN (2:1)	A8, A12	I	USB3	—	USB3.0 Receive data D- signal for super-speed
U2DP (2:1)	P8, P10	I/O	USB2	—	USB2.0 D+ signal for high-/full-/low-speed
U2DM (2:1)	N8, N10	I/O	USB2	—	USB2.0 D− signal for high-/full-/low-speed
OCI1B OCI2B	H13 G14	I	3.3V Input	Low	Over-current status input signal for each downstream facing port. 0: Over-current condition is detected 1: No over-current condition is detected.
PPON (2:1)	H14, J14	O	3.3V Output (6mA)	High	USB port power supply control signal for each downstream facing ports. 0: Power supply OFF 1: Power supply ON

SPI Interface

Pin Name	Ball No.	Direction	Buffer Type	Active Level	Function
SPISCK	M2	O	3.3V Output (6mA)	_	SPI serial flash ROM clock signal.
SPICSB	N2	O	3.3V Output (6mA)	_	SPI serial flash ROM chip select signal.
SPISI	N1	O	3.3V Output (6mA)	_	SPI serial flash ROM data write signal.
SPISO	M1	I	3.3V Input		SPI serial flash ROM data read signal.

★ 2. ELECTRICAL SPECIFICATIONS

Buffer List

- 3.3 V input buffer
  CSEL, AUXDET, OCI1B, OCI2B, PSEL
- 3.3 V input schmitt buffer
  PONRSTB, PERSTB
- 3.3 V I_{OL} = 6mA output buffer
  SMIB, PPON(2:1)
- 3.3 V I_{OL} = 6mA bi-directional buffer
  SPISO, SPISI, SPISCK, SPICSB
- N-ch open drain buffer
  PEWAKEB, PECREQB
- 3.3 V oscillator interface
  XT1, XT2
- USB Classic interface
  U2DP(2:1), U2DN(2:1), RREF
- PCI Express Serdes
  PECLKP, PECLKN, PETXP, PETXN, PERXP, PERXN
- USB Superspeed interface
  U3TXDP(2:1), U3TXDN(2:1), U3RXDP(2:1), U3RXDN(2:1)

Terminology

Terms Used in Absolute Maximum Ratings

Parameter	Symbol	Meaning
Power supply voltage	V_{DD33}, V_{DD10}, $U2AV_{DD33}$, $U3AV_{DD33}$	Indicates the voltage range within which damage or reduced reliability will not result when power is applied to a V_{DD} pin.
Input voltage	V_I	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an input pin.
Output voltage	V_O	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an output pin.
Output current	I_O	Indicates absolute tolerance values for DC current to prevent damage or reduced reliability when current flows out of or into output pin.
Operating temperature	T_A	Indicates the ambient temperature range for normal logic operations.
Storage temperature	T_{stg}	Indicates the element temperature range within which damage or reduced reliability will not result while no voltage or current is applied to the device.

Terms Used in Recommended Operating Range

Parameter	Symbol	Meaning
Power supply voltage	V_{DD33}, V_{DD10}, $U2AV_{DD33}$, $U3AV_{DD33}$	Indicates the voltage range for normal logic operations occur when V_{SS} = 0 V.
High-level input voltage	V_{IH}	Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the high level states for normal operation of the input buffer. * If a voltage that is equal to or greater than the “Min.” value is applied, the input voltage is guaranteed as high level voltage.
Low-level input voltage	V_{IL}	Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the low level states for normal operation of the input buffer. * If a voltage that is equal to or lesser than the “Max.” value is applied, the input voltage is guaranteed as low level voltage.

Term Used in DC Characteristics

Parameter	Symbol	Meaning
Off-state output leakage current	I_{OZ}	Indicates the current that flows from the power supply pins when the rated power supply voltage is applied when a 3-state output has high impedance.
Input leakage current	I_I	Indicates the current that flows when the input voltage is supplied to the input pin.

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Units
Power supply voltage	V_{DD33}, $U2AV_{DD33}$ $U3AV_{DD33}$		–0.5 ~ +4.6	V
	V_{DD10}		–0.5 ~ +1.4	V
Input voltage, 3.3 V buffer	V_I	$V_I < V_{DD33} + 0.5V$	–0.5 ~ +4.6	V
Output voltage, 3.3 V buffer	V_O	$V_O < V_{DD33} + 0.5V$	–0.5 ~ +4.6	V
Output current	I_O		15	mA
Storage temperature	T_{stg}		–65 ~ +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameters. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Recommended Operating Ranges

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Operating voltage	V_{DD33}, $U2AV_{DD33}$ $U3AV_{DD33}$		3.0	3.3	3.6	V
	V_{DD10}		0.9975	1.05	1.1025	V
High-level input voltage	V_{IH}		2.0		V_{DD33}+0.3	V
Low-level input voltage	V_{IL}		–0.3		0.8	V
Operating ambient temperature	T_A		0		+85	°C

DC Characteristics (V_{DD33} = 3.3V ± 10%, V_{DD10} = 1.05V ± 5%, T_A = –0 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Units
Off-state output current	I_{OZ}	$V_I = V_{DD}$ or V_{SS}		±10	μA
Input leakage current	I_I	$V_I = V_{DD}$ or V_{SS}		±10	μA
Low-level output voltage	V_{OL}	I_{OL} = 6mA		0.4	V
High-level output voltage	V_{OH}	I_{OH} = –6mA	2.4		V

Pin capacitance

Parameter	Symbol	Condition	Min.	Max.	Units
SPI Interface Pin capacitance	C_{SPI}			5	pF

AC Characteristics (V_{DD33} = 3.3V ± 10%, V_{DD10} = 1.05V ± 5%, T_A = –0 to +85°C)

System clock (XT1/XT2) ratings

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Clock frequency	F_{CLK}	Crystal	–100 ppm	24	+100 ppm	MHz
		Oscillator block	–100 ppm	48	+100 ppm	MHz
Clock duty cycle	T_{DUTY}		40	50	60	%

Remarks 1. Required accuracy of crystal or oscillator block is including initial frequency accuracy, the spread of Crystal capacitor loading, supply voltage, temperature and aging, etc.

Power on Reset (PONRSTB) Timings

Parameter	Symbol	Condition	Min.	Max.	Units
Power on reset time	T_{PONRST}	Figure 2-1	1		ms

Remarks 1. There is no order to power-on of V_{DD33}, $U2AV_{DD33}$, $U3AV_{DD33}$ and V_{DD10}.

2. All power sources should be stable within 100ms from the fastest rising edge of power sources.

3. PONRSTB shall be de-asserted after all power sources and the system clock become stable.

PCI Express Interface - Reference Clock (PECLKP and PECLKN) Timings

Parameter	Symbol	Condition	Min.	Max.	Units
Rising Edge Rate	T_{RISE}	Figure 2-5	0.6	4.0	V/ns
Falling Edge Rate	T_{FALL}	Figure 2-5	0.6	4.0	V/ns
Differential Input High Voltage	V_{IH}	Figure 2-8	+150		mV
Differential Input Low Voltage	V_{IL}	Figure 2-8		–150	mV
Absolute crossing point voltage	V_{CROSS}	Figure 2-3	+250	+550	mV
Variation of V_{CROSS} over all rising clock edge	$V_{CROSS\ DELTA}$	Figure 2-4		+140	mV
Ring-back Voltage Margin	V_{RB}	Figure 2-8	–100	+100	mV
Time before V_{RB} is allowed	T_{STABLE}	Figure 2-8	500		ps
Average Clock Period Accuracy	$T_{PERIOD\ AVG}$		–300	+2800	ppm
Absolute Period (including Jitter and Spread Spectrum)	$T_{PERIOD\ ABS}$		9.847	10.203	ps
Cycle to Cycle Jitter	$V_{CCJITTER}$			150	ps
Absolute Max input voltage	V_{MAX}	Figure 2-3		+1.15	V
Absolute Min input voltage	$V_{MIN\backslash}$	Figure 2-3		–0.3	V
Duty Cycle			40	60	%
Rising edge rate (PECLKP) to falling edge rate (PECLKN) matching				20	%
Clock source DC impedance	Z_{C-DC}	Figure 2-2	40	60	Ω

PCI Express Interface - PERSTB and PEWAKEB Signal Timings

Parameter	Symbol	Condition	Min.	Max.	Units
Power stable to PERSTB inactive	T_{PVPERL}	Figure 2-1	100		ms
PECLKP/PECLKN stable before PERSTB inactive	$T_{PERST-CLK}$	Figure 2-1	100		μs

PCI Express Interface – Power-Up and PECREQB Signal Timings

Parameter	Symbol	Condition	Min.	Max.	Units
Power Valid to PECREQB Output active	T_{PVCRL}	Figure 2-9		100	μs
Power Valid to PERSTB input inactive	T_{PVPGL}	Figure 2-9	1		ms
PECLKP/PECLKN stable before PERSTB inactive	$T_{PE\_RSTB-CLK}$	Figure 2-9	100		μs

PCI Express Interface – PECREQB Clock Control Timings

Parameter	Symbol	Condition	Min.	Max.	Units
PECREQB de-asserted high to clock parked	T_{CRHOFF}	Figure 2-10	0		ns
PECREQB asserted low to clock active	T_{CRLON}	Figure 2-10		400	ns

PCI Express Interface – Differential Transmitter (TX) Specifications
(Refer to PCI Express™ Base Specification Revision 2.0 for more information)

(1/2)

Parameter	Symbol	2.5GT/s	5.0GT/S.	Units
Unit Interval	UI	399.88(min) 400.12(max)	199.94(min) 200.06(max)	ps
Differential Peak to Peak(p-p) Tx voltage swing	$V_{TX-DIFFp-p}$	0.8(min) 1.2(max)	0.8(min) 1.2(max)	V
Low power differential p-p Tx voltage swing	$V_{TX-DIFFp-p-LOW}$	0.4(min) 1.2(max)	0.4(min) 1.2(max)	V
Tx de-emphasis level ration	$V_{TX-DE-RATIO-3.5dB}$	3.0(min) 4.0(max)	3.0(min) 4.0(max)	dB
Tx de-emphasis level ration	$V_{TX-DE-RATIO-6dB}$	Not specified	5.5(min) 6.5(max)	dB
Instantaneous lone pulse width	$T_{MIN-PULSE}$	Not specified	0.9(min)	UI
Transmitter Eye including all jitter sources	T_{TX-EYE}	0.75(min)	0.75(min)	UI
Maximum time between the jitter median and max deviation from the median	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	0.125(max)	Not specified	UI
Tx deterministic jitter >1.5MHz	$T_{TX-HF-DJ-DD}$	Not specified	0.15(max)	UI
Tx RMS jitter > 1.5MHz	$T_{TX-LF-RMS}$	Not specified	3.0	ps RMS
Transmitter rise and fall time	$T_{TX-RISE-FALL}$	0.125(min)	0.15(max)	UI
Tx rise/fall mismatch	$T_{RF-MISMATCH}$	Not specified	0.1(max)	UI
Maximum Tx PLL bandwidth	BW_{TX-PLL}	22(max)	16(max)	MHz
Minimum Tx PLL BW for 3dB peaking	$B_{WTX-PLL-LO-3DB}$	1.5(min)	8(min)	MHz
Minimum Tx PLL BW for 1dB peaking	$B_{WTX-PLL-LO-1DB}$	Not specified	5(min)	MHz
Tx PLL peaking with 8MHz min BW	$P_{KGTX-PLL1}$	Not specified	3.0(max)	dB
Tx PLL peaking with 5MHz min BW	$P_{KGTX-PLL2}$	Not specified	1.0(max)	dB
Tx package plus Si differential return loss	$RL_{TX-DIFF}$	10(min)	10(min) for 0.05 – 1.25GHz 8(min) for 1.25 – 2.5GHz	dB
Tx package plus Si common mode return loss	RL_{TX-CM}	6(min)	6(min)	dB
DC differential Tx impedance	$Z_{TX-DIFF-DC}$	80(min) 120(max)	120(max)	Ω
Tx AC common mode voltage (5GT/s)	$V_{TX-CM-AC-PP}$	Not specified	100(max)	mVPP
Tx AC common mode voltage (2.5GT/s)	$V_{TX-CM-AC-P}$	20	Not specifed	mV
Transmitter short-circuit current limit	$I_{TX-SHORT}$	90(max)	90(max)	mA
Transmitter DC common-mode voltage	$V_{TX-DC-CM}$	0(min) 3.6(max)	0(min) 3.6(max)	V
Absolute Delta of DC Common Mode Voltage during L0 and Electrical Idle	$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	0(min) 100(max)	0(min) 100(max)	mV

(2/2)

Parameter	Symbol	2.5GT/s	5.0GT/S.	Units
Absolute Delta of DC Common Mode Voltage between PETXP and PETXN	$V_{TX-CM-DC-LINE-DELTA}$	0(min) 25(max)	0(min) 25(max)	mV
Electrical Idle Differential Peak Output Voltage	$V_{TX-IDLE-DIFF-AC-p}$	0(min) 20(max)	0(min) 20(max)	mV
DC Electrical Idle Differential Output Voltage	$V_{TX-IDLE-DIFF-DC}$	Not specified	0(min) 5(max)	mV
The amount of voltage change allowed during Receiver Detection	$V_{TX-RCV-DETECT}$	600(max)	600(max)	mV
Minimum time spent in Electrical Idle	$T_{TX-IDLE-MIN}$	20(min)	20(min)	ns
Maximum time to transition to a valid Electrical Idle after sending an EIOS	$T_{TX-IDLE-SET-TO-IDLE}$	8(max)	8(max)	ns
Maximum time to transition to valid diff signaling after leaving Electrical Idle	$T_{TX-IDLE-TO-DIFF-DATA}$	8(max)	8(max)	ns
Crosslink random timeout	$T_{CROSSLINK}$	1.0(max)	1.0(max)	ns
Lane-to-Lane Output Skew	$L_{TX-SKEW}$	500ps + 2UI(max)	500ps + 4UI(max)	ps
AC Coupling Capacitor	C_{TX}	75(min) 200(max)	75(min) 200(max)	nF

PCI Express Interface – Differential Receiver (RX) Specifications

(Refer to PCI Express™ Base Specification Revision 2.0 for more information)

Parameter	Symbol	2.5GT/s	5.0GT/S.	Units
Unit Interval	UI	399.88(min) 400.12(max)	199.94(min) 200.06(max)	ps
Differential Rx peak-peak voltage for common Reference clock Rx architecture	$V_{RX-DIFF-PP-CC}$	0.175(min) 1.2(max)	0.120(min) 1.2(max)	V
Differential Rx peak-peak voltage for data clocked Rx architecture	$V_{RX-DIFF-PP-DC}$	0.175(min) 1.2(max)	0.100(min) 1.2(max)	V
Receiver eye time opening	t_{RX-EYE}	0.40(min)	Not specified	UI
Max Rx inherent timing error	$t_{RX-TJ-CC}$	Not specified	0.40(max)	UI
Max Rx inherent timing error	$t_{RX-TJ-DC}$	Not specified	0.34(max)	UI
Max Rx inherent deterministic timing error	$t_{RX-DJ-DD-CC}$	Not specified	0.30(max)	UI
Max Rx inherent deterministic timing error	$t_{RX-DJ-DD-DC}$	Not specified	0.24(max)	UI
Max time delta between median and deviation from median	$t_{RX-EYE-MEDIAN-to-MAX-JITTER}$	0.3(max)	Not specified	UI
Minimum width pulse at Rx	$t_{RX-MIN-PULSE}$	Not specified	0.6(min)	UI
Min/max pulse voltage on consecutive UI	$t_{RX-MAX-MIN-RATIO}$	Not specified	5(max)	-
Maximum Rx PLL bandwidth	$BW_{RX-PLL-HI}$	22(max)	16(max)	MHz
Minimum Rx PLL BW for 3dB peaking	$BW_{RX-PLL-LO-3DB}$	1.5(min)	8(min)	MHz
Minimum Rx PLL BW for 1dB peaking	$BW_{RX-PLL-LO-1DB}$	Not specified	5(min)	MHz
Rx PLL peaking with 8 MHz min BW	$PKG_{RX-PLL1}$	Not specified	3.0	dB
Rx PLL peaking with 5MHz min BW	$PKG_{RX-PLL2}$	Not specified	1.0	dB
Rx package plus Si differential return loss	$RL_{RX-DIFF}$	10(min)	10(min) for 0.05 – 1.25GHz 8(min) for 1.25 – 2.5GHz	dB
Common mode Rx return loss	RL_{RX-CM}	6(min)	6(min)	dB
Receiver DC single ended impedance	Z_{RX-DC}	40(min) 60(max)	40(min) 60(max)	Ω
DC differential impedance	$Z_{RX-DIFF-DC}$	80(min) 120(max)	Not specified	Ω
Rx AC common mode voltage	$V_{RX-CM-AC-P}$	150(max)	150(max)	mVP
DC input CM input Impedance for V>0 durin Reset or power down	$Z_{RX-HIGH-IMP-DC-POS}$	50k(min)	50k(min)	Ω
DC input CM input Impedance for V<0 during Reset or power down	$Z_{RX-HIGH-IMP-DC-NEG}$	1.0k(min)	1.0k(min)	Ω
Electrical Idle Detect Threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65(min) 175(max)	65(min) 175(max)	mV
Unexpected Electrical Idle Enter Detect Threshold Integration Time	$t_{RX-IDLE-DET-DIFF-ENTERTIME}$	10(max)	10(max)	ms
Lane to Lane skew	$L_{RX-SKEW}$	20(max)	8(max)	ns

USB3.0 SuperSpeed Interface – Differential Transmitter (TX) Specifications
(Refer to Universal Serial Bus 3.0 Specification Revision 1.0 for more information)

Transmitter Normative Electrical Parameters

Parameter	Symbol	Min	Max	Units
Unit Interval	UI	199.94	200.06	ps
Differential p-p Tx voltage swing	$V_{TX-DIFF-PP}$	0.8	1.2	V
Low-Power Differential p-p Tx voltage swing	$V_{TX-DIFF-PP-LOW}$	0.4	1.2	V
Tx de-emphasis	$V_{TX-DE-RATIO}$	3.0	4.0	dB
DC differential impedance	$R_{TX-DIFF-DC}$	72	120	Ω
The amount of voltage change allowed during Receiver Detection	$V_{TX-RCV-DETECT}$		0.6	V
AC Coupling Capacitor	$C_{AC-COUPLING}$	75	200	nF
Maximum slew rate	$t_{CDR-SLEW-MAX}$		10	ms/s

Transmitter Informative Electrical Parameters

Parameter	Symbol	Min	Max	Units
Deterministic min pulse	$t_{MIN-PULSE-Dj}$	0.96		UI
Tx min pulse	$t_{MIN-PULSE-Tj}$	0.90		UI
Transmitter Eye	t_{TX-EYE}	0.625		UI
Tx deterministic jitter	$t_{TX-DJ-DD}$		0.205	UI
Tx input capacitance for return loss	$C_{TX-PARASITIC}$		1.25	pf
Transmitter DC common mode impedance	R_{TX-DC}	18	30	Ω
Transmitter short-circuit current limit	$I_{TX-SHORT}$		60	mA
Transmitter DC common-mode voltage	$V_{TX-DC-CM}$	0	2.2	V
Tx AC common mode voltage	$V_{TX-CM-AC-PP-ACTIVE}$		100	mVp-p
Absolute DC Common Mode Voltage between U1 and U0	$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$		200	mV
Electrical Idle Differential Peak- Peak Output voltage	$V_{TX-IDLE-DIFF-AC-pp}$	0	10	mV
DC Electrical Idle Differential Output Voltage	$V_{TX-IDLE-DIFF-DC}$	0	10	mV

USB3.0 SuperSpeed Interface – Differential Receiver (RX) Specifications
(Refer to Universal Serial Bus 3.0 Specification Revision 1.0 for more information)

Receiver Normative Electrical Parameters

Parameter	Symbol	Min	Max	Units
Unit Interval	UI	199.94	200.06	ps
Receiver DC common mode impedance	R_{RX-DC}	18	30	Ω
DC differential impedance	$R_{RX-DIFF-DC}$	72	120	Ω
DC Input CM Input Impedance for V>0 during Reset of Power down	$Z_{RX-HIGH-IMP-DC-POS}$	25k		Ω
LFPS Detect Threshold	$V_{RX-LFPS-DET-DIFF-p-p}$	100	300	mV

Receiver Informative Electrical Parameters

Parameter	Symbol	Min	Max	Units
Differential Rx peak-to-peak voltage	$V_{RX-DIFF-PP-POST-EQ}$	30		mV
Max Rx inherent timing error	T_{RX-Tj}		0.45	UI
Max Rx inherent deterministic timing error	$T_{RX-DJ-DD}$		0.285	UI
Rx input capacitance for return loss	$C_{RX-PARASITIC}$		1.1	pf
Rx AC common mode voltage	$V_{RX-CM-AC-P}$		150	mVPeak
Rx AC common mode voltage during the U1 to U0 transition	$V_{RX-CM-DC-ACTIVE-IDLE-DELTA-P}$		200	mVPeak

USB2.0 interface

(Refer to Universal Serial Bus Specification Revision 2.0 for more information)

Low-speed Source Electrical Characteristics

Parameter	Symbol	Min	Max	Units
Driver Characteristics:				
Transition Time:				
Rise Time	T_{LR}	75	300	ns
Fall Time	T_{LF}	75	300	ns
Rise and Fall Time Matching	T_{LRFM}	80	125	%
Clock Timings:				
Low-speed Data Rate	$T_{LDRATHS}$	1.49925	1.50075	Mb/s
Low-speed Data Timing:				
Source Jitter for Differential Transition to SE0 Transition	T_{LDEOP}	–40	100	ns
Source Jitter total (including frequency tolerance):				
To Next Transition	T_{DDJ1}	–25	25	ns
For Paired Transitions	T_{DDJ2}	–14	14	ns
Differential Receiver Jitter:				
To Next Transition	T_{UJR1}	–152	152	ns
For Paired Transitions	T_{UJR2}	–200	200	ns
Source SE0 interval of EOP	T_{LEOPT}	1.25	1.50	μs
Receiver SE0 interval of EOP	T_{LEOPR}	670		ns
Width of SE0 interval during differential transition	T_{LST}		210	ns

Full-speed Source Electrical Characteristics

Parameter	Symbol	Min	Max	Units
Driver Characteristics:				
Rise Time	T_{FR}	4	20	ns
Fall Time	T_{FF}	4	20	ns
Differential Rise and Fall Time Matching	T_{FRFM}	90	111.11	%
Clock Timings:				
Full-speed Data Rate	$T_{FDRATHS}$	11.9940	12.0060	Mb/s
Frame Interval	T_{FRAME}	0.9995	1.0005	ms
Consecutive Frame Interval Jitter	T_{RFI}		42	ns
Full-speed Data Timing:				
Source Jitter for Differential Transition to SE0 Transition	T_{FDEOP}	–2	5	ns
Source Jitter total (including frequency tolerance):				
To Next Transition	T_{DJ1}	–3.5	3.5	ns
For Paired Transitions	T_{DJ2}	–4	4	ns
Receiver Jitter:				
To Next Transition	T_{JR1}	–18.5	18.5	ns
For Paired Transitions	T_{JR2}	–9	9	ns
Source SE0 interval of EOP	T_{FEOPT}	160	175	ns
Receiver SE0 interval of EOP	T_{FEOPR}	82		ns
Width of SE0 interval during differential transition	T_{FST}		14	ns

High-speed Source Electrical Characteristics

Parameter	Symbol	Min	Max	Units
Driver Characteristics:				
Rise Time (10% - 90%)	T_{HSR}	500		ps
Fall Time (10% - 90%)	T_{HSF}	500		ps
Driver waveform requirements	Figure 2-14			
Clock Timings:				
High-speed Data Rate	T_{HSDRAT}	497.760	480.240	Mb/s
Microframe Interval	$T_{HSFRAME}$	124.9375	125.0625	μs
Consecutive Microframe Interval Difference	T_{HSRFI}		4 high-speed bit times	
High-speed Data Timing:				
Data source jitter	Figure 2-14			
Receiver jitter tolerance	Figure 2-12			

Hub Event Timings

Parameter	Symbol	Min	Max	Units
Time to detect a downstream facing port connect event	T_{DCNN}	2.5	2000	μs
Time to detect a disconnect event at a hub's downstream facing port	T_{DDIS}	2	2.5	μs
Duration of driving resume to a downstream port	T_{DRSMDN}	20		ms
Time from detecting downstream resume to rebroadcast	T_{URSM}		1.0	ms
Inter-packet delay for packets traveling in same direction	$T_{HSIPDSD}$	88		Bit times
Inter-packet delay for packets traveling in opposite direction	$T_{HSIPDOD}$	8		Bit times
Inter-packet delay for root hub response for high-speed	$T_{HSRSPIPD1}$		192	Bit times
Time for which a Chirp J or Chirp K must be continuously detected by hub during Reset handshake	T_{FILT}	2.5		μs
Time after end of device Chirp K by which hub must start driving first Chirp K in the hub's chirp sequence	T_{DCHBIT}		100	μs
Time for which each individual Chirp J or Chirp K in the chirp sequence is driven downstream by hub during reset	T_{DCHBIT}	40	60	μs
Time before end of reset by which a hub must end its downstream chirp sequence	T_{DCHSE0}	100	500	μs

SPI Type Serial ROM Interface

SPI Type Serial ROM Interface Signals Timing (SPI Mode 0)

Parameter	Symbol	Min.	Max.	Units
SPISCK Clock Frequency			32	MHz
Clock pulses width Low	t_{SCLLOW}			ns
Clock pulses width high	$t_{SCLHIGH}$	9		ns
SPICSB disable time	t_{SCSDIS}	25		ns
SPICSB setup time	t_{SCSSU}	25		ns
SPICSB hold time	t_{SCSH}	10		ns
SPISI setup time to SPISCK rising edge	t_{SDWSU}	5		ns
SPISI hold time from SPISCK rising edge	t_{SDWH}	5		ns
SPISO validate time from SPISCK falling edge	$t_{SDRVALID}$		9	ns
SPISO hold time from SPISCK falling edge	t_{SDRH}	0		ns
SPISO disable time from SPICSB disabled	t_{SDRDIS}		100	ns

Figure 2-1. Power Up and Reset

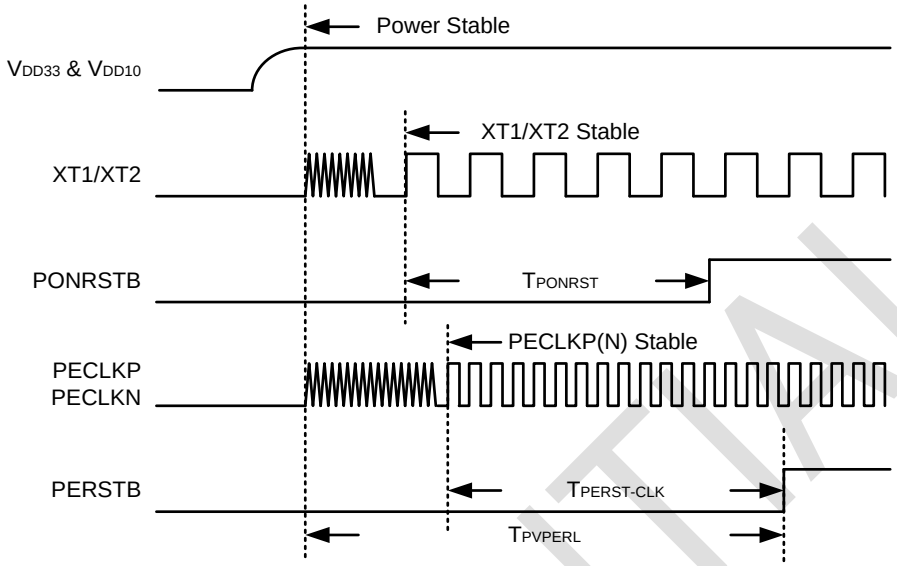


Figure 2-2. PCI Express Single-Ended Measurement Points for Absolute Cross Point and Swing

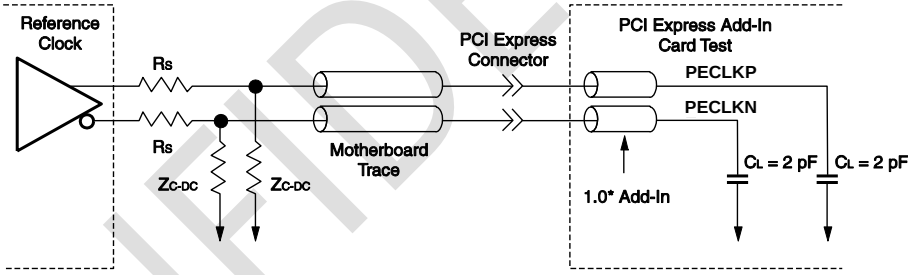


Figure 2-3. PCI Express Single-Ended Measurement Points for Absolute Cross Point and Swing

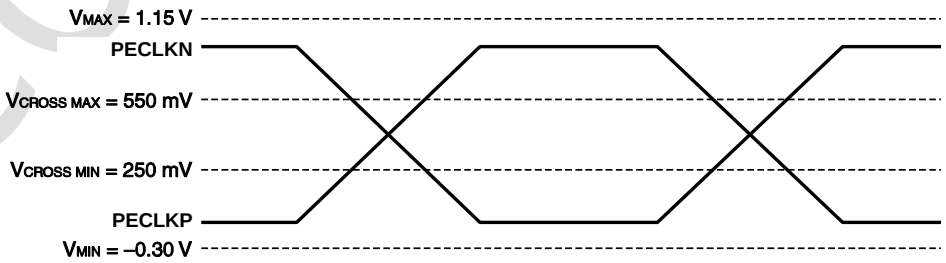


Figure 2-4. PCI Express Single-Ended Measurement Points for Delta Cross Point

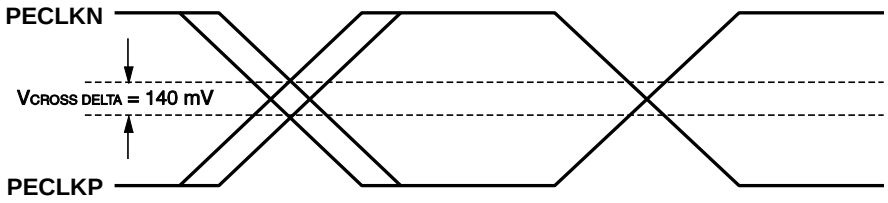


Figure 2-5. PCI Express Single-Ended Measurement Points for Rise and Fall Time Matching

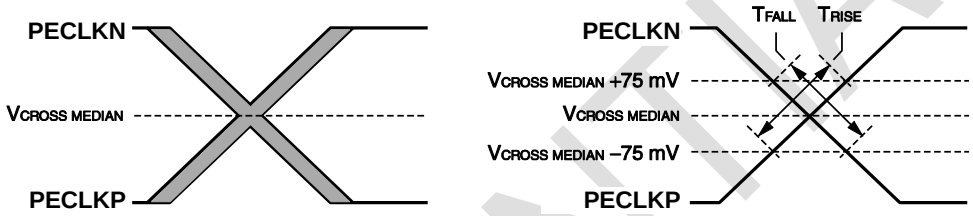


Figure 2-6. PCI Express Differential Measurement Points for Duty Cycle and Period

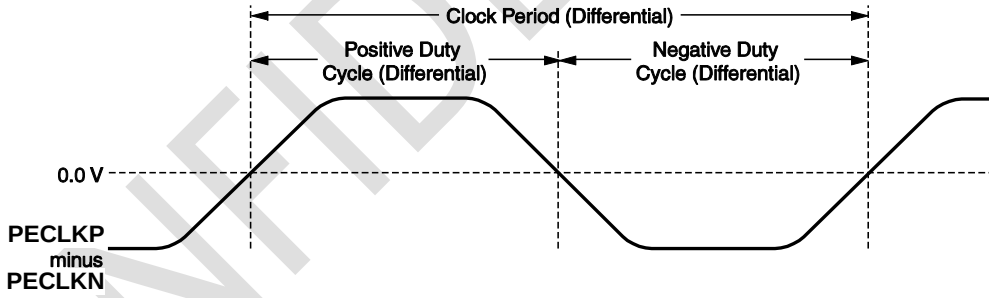


Figure 2-7. PCI Express Differential Measurement Points for Rise and Fall Time

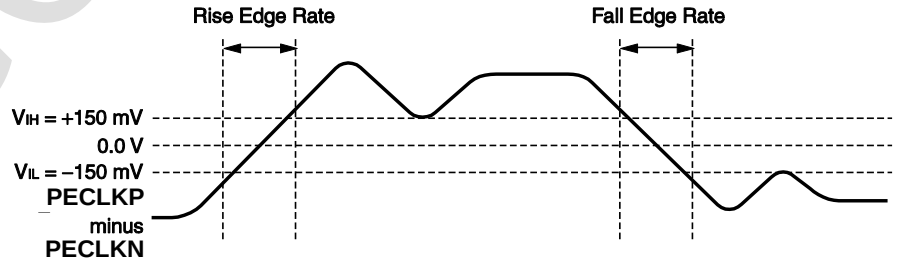


Figure 2-8. PCI Express Differential Measurement Points for Ring-back

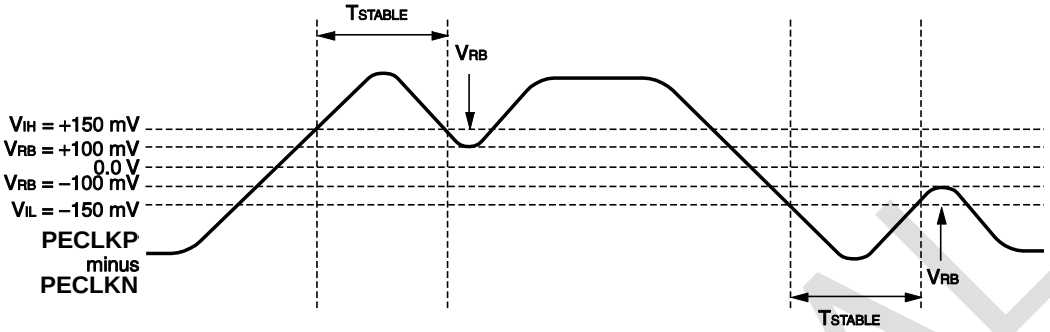
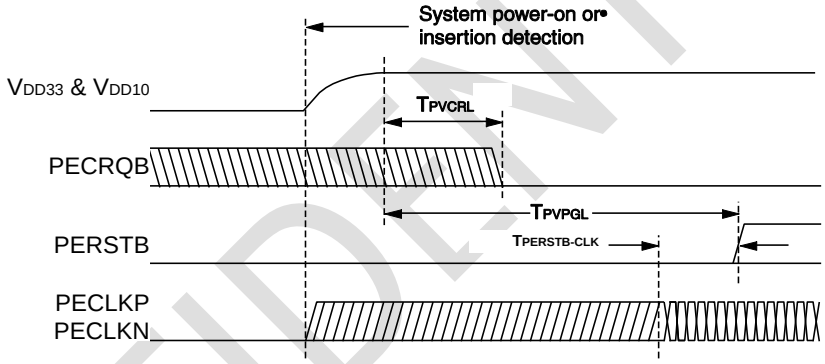


Figure 2-9. PCI Express Power-Up PECREQB Timing



Note • T_{PVCRL} is measured from the later rising edge of either V_{DD33} or V_{DD10}

Figure 2-10. PCI Express PECREQB Clock Control Timing

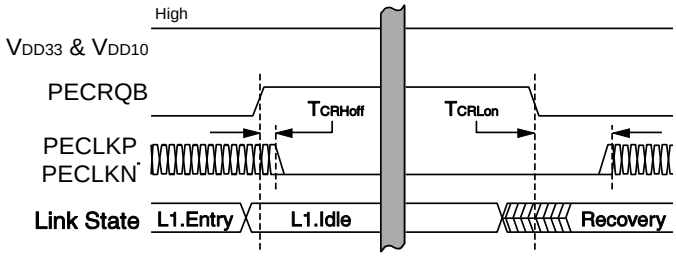


Figure 2-11. Differential Input Sensitivity Range for Low-/Full-speed

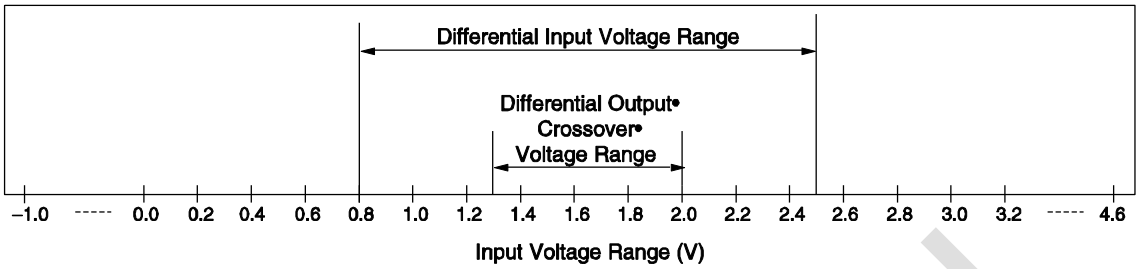


Figure 2-12. Receiver Sensitivity for Transceiver at U2DP/U2DM

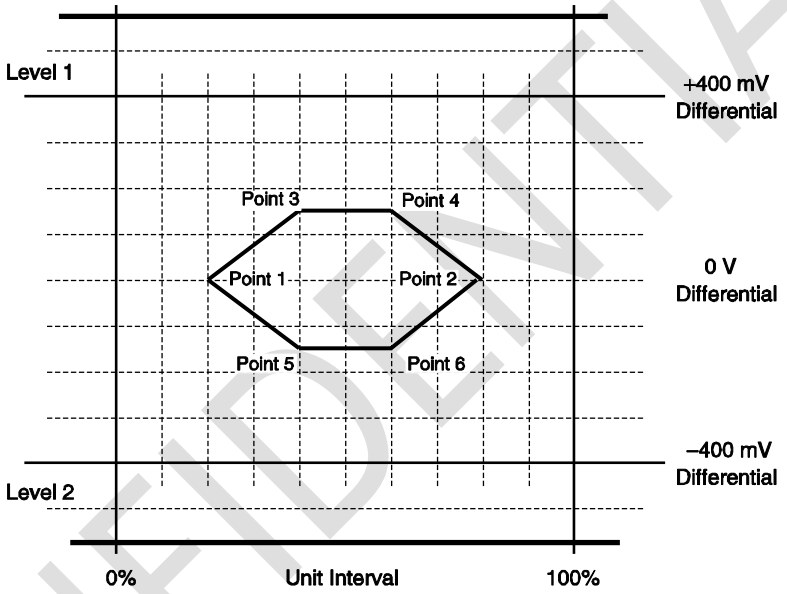


Figure 2-13. Receiver Measurement Fixtures

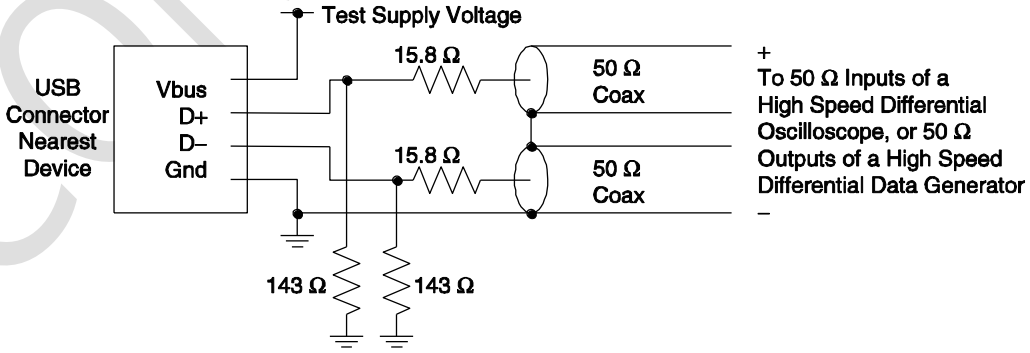


Figure 2-14. Transmit Waveform for Transceiver at U2DP/U2DM

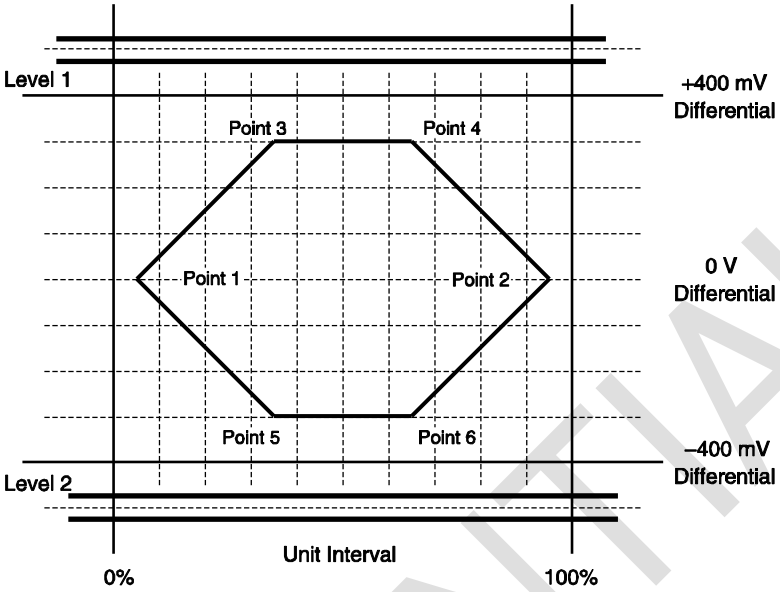


Figure 2-15. Transmitter Measurement Fixtures

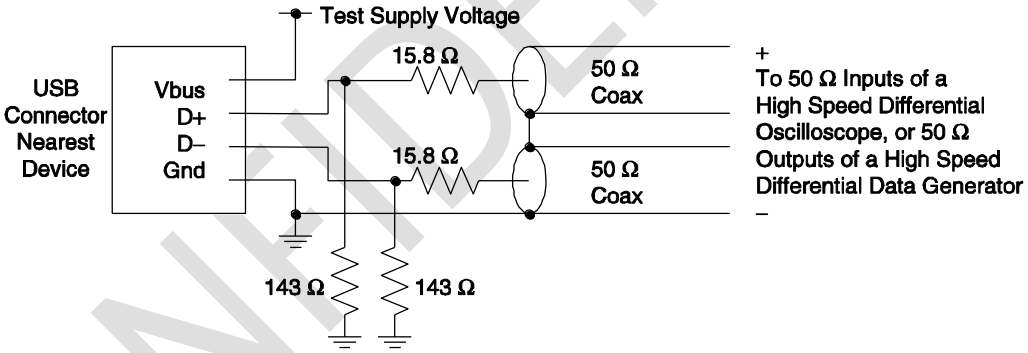


Figure 2-16. Differential data jitter for low-/full-speed

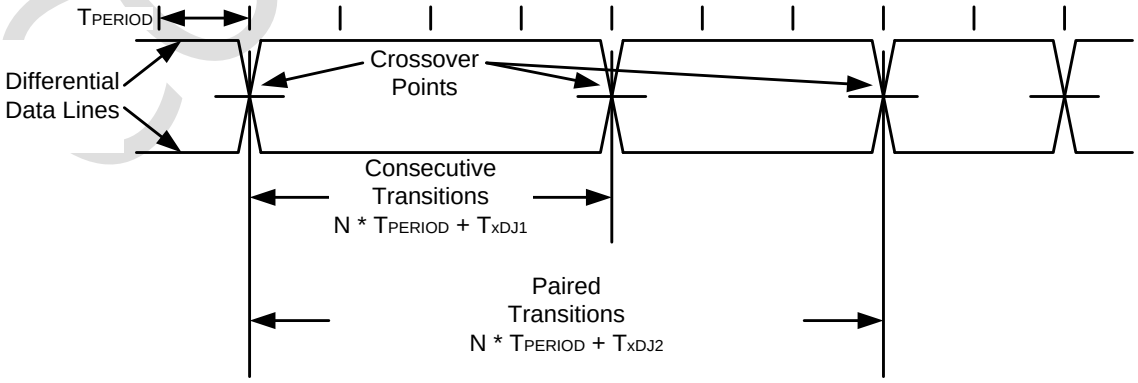


Figure 2-17. Differential-to-EOP transition skew and EOP width for low-/full-speed

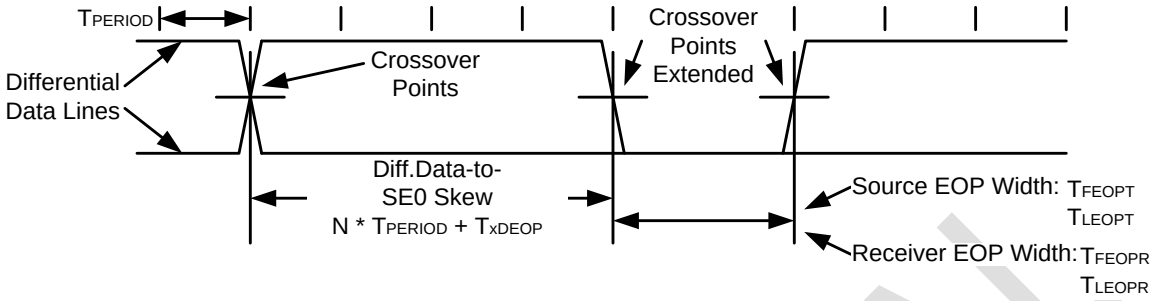


Figure 2-18. Receiver jitter tolerance for low-/full-speed

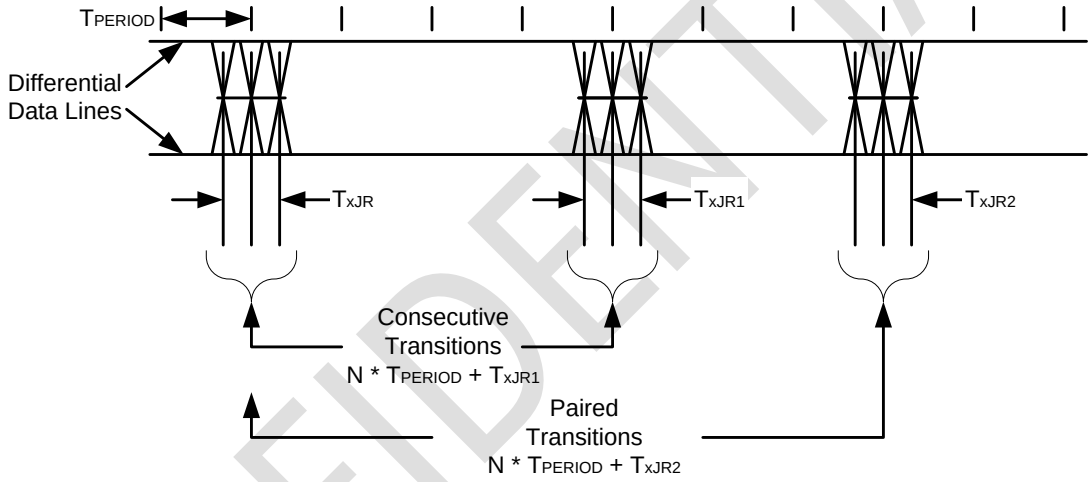
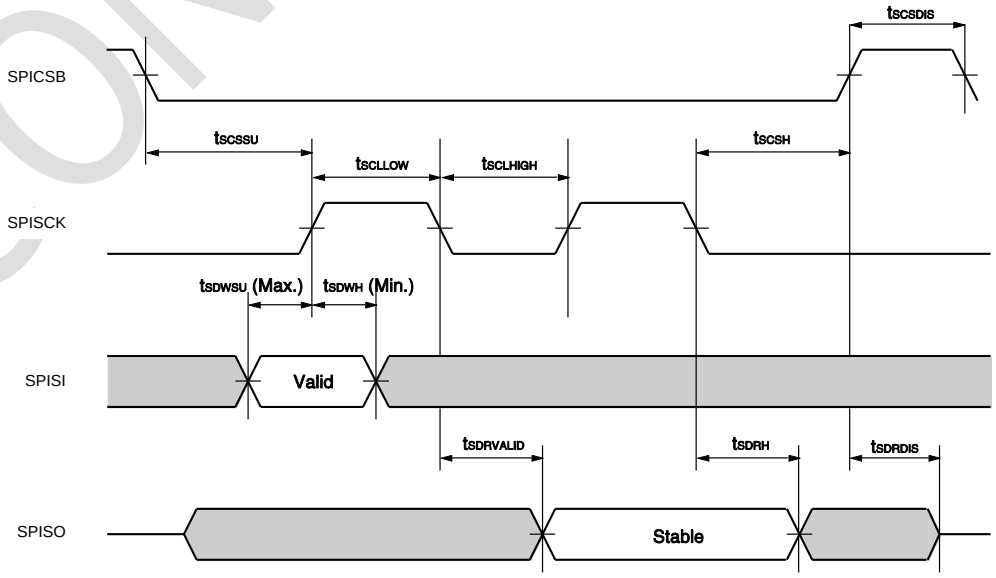
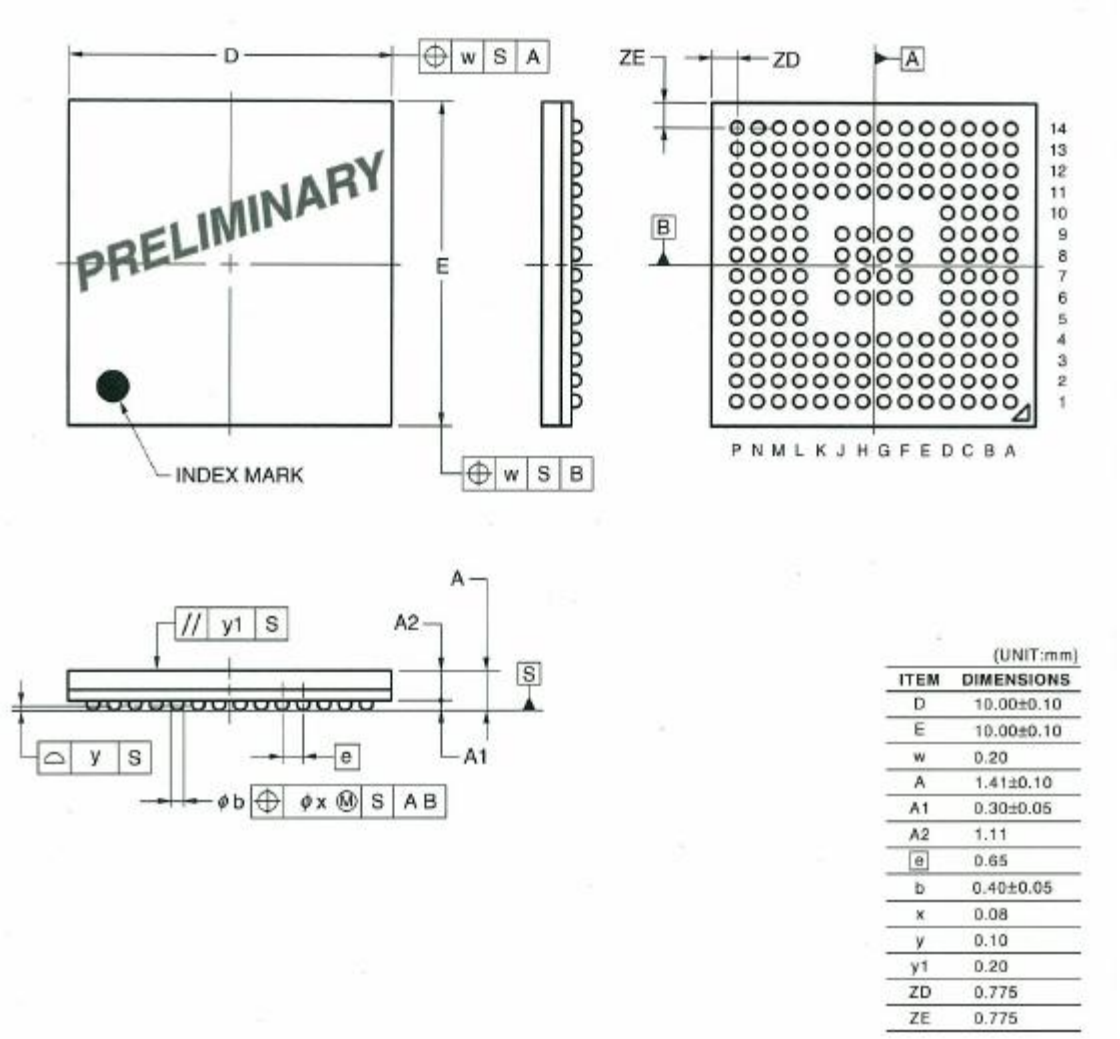


Figure 2-19. SPI Type Serial ROM Signal Timing



3. PACKAGE DRAWINGS

• μPD720200F1-DAK-A



(UNIT:mm)

ITEM	DIMENSIONS
D	10.00±0.10
E	10.00±0.10
w	0.20
A	1.41±0.10
A1	0.30±0.05
A2	1.11
e	0.65
b	0.40±0.05
x	0.08
y	0.10
y1	0.20
ZD	0.775
ZE	0.775

4. RECOMMENDED SOLDERING CONDITIONS

The μPD720200 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

• μPD720200F1-DAK-A: 176-pin plastic FBGA (10 × 10)

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Peak package's surface temperature: 260°C, Reflow time: 60 seconds or less (220°C or higher), Maximum allowable number of reflow processes: 3, Exposure limit Note: 7 days (10 hours pre-backing is required at 125°C afterwards), Flux: Rosin flux with low chlorine (0.2 Wt% or below) recommended. <Caution> Non-heat-resistant trays, such as magazine and taping trays, cannot be baked before unpacking.	IR60-107-3

Note The Maximum number of days during which the product can be stored at a temperature of 25°C and a relative humidity of 65% or less after dry-pack package is opened.

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

- **The information in this document is current as of March, 2007. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC Electronics data sheets or data books, etc., for the most up-to-date specifications of NEC Electronics products. Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.**
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  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support).

  "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

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