PLESSEY
Semiconductors

T-75-11-29

2MBIT PCM SIGNALLING CIRCUIT

MV1441

HDB3 ENCODER/DECODER/CLOCK REGENERATOR

The 2.048MBit PCM Signalling Circuits comprise a group of circuits which will perform the common signalling and error detection functions for a 2.048MBit PCM transmission link operating to the appropriate CCITT recommendations. The circuits are fabricated in CMOS and operate from a single 5 volt supply with relevant inputs and outputs TTL compatible.

The MV1441 is an encoder/decoder for the pseudo-ternary transmission code, HDB3 (CCITT Orange Book Vol.III.2 Annex to Rec. G703). The device encodes and decodes simultaneously and asynchronously. Error monitoring functions are provided to detect violations of HDB3 coding, all ones detection and loss of input (all zeros detection). In addition a loop back function is provided for terminal testing. A clock recovery circuit is provided using a 16.384MHz crystal (12.352MHz for 1.544MHz operation), which may be shared between several separate devices.

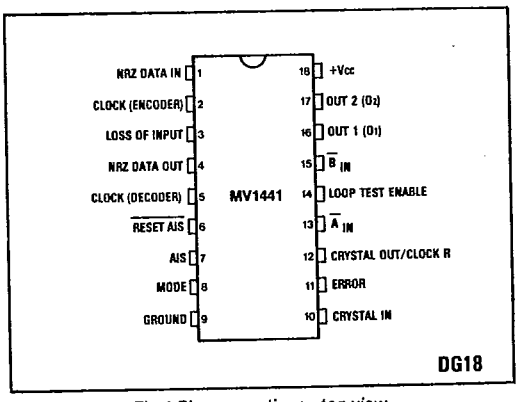

Fig.1 Pin connections - top view

FEATURES

- On-Chip Digital Clock Regenerator
- HDB3 Encoding and Decoding to CCITT rec. G703
- Asynchronous Operation
- Simultaneous Encoding and Decoding
- Clock Recovery Signal allows Off-Chip Clock Regeneration
- Loop Back Control
- HDB3 Error Monitor
- 'All Ones' Error Monitor
- Loss of Input Alarm (All Zeros Detector)
- Decode Data in NRZ Form
- Low Power Operation
- 2.048MHz or 1.544MHz Operation

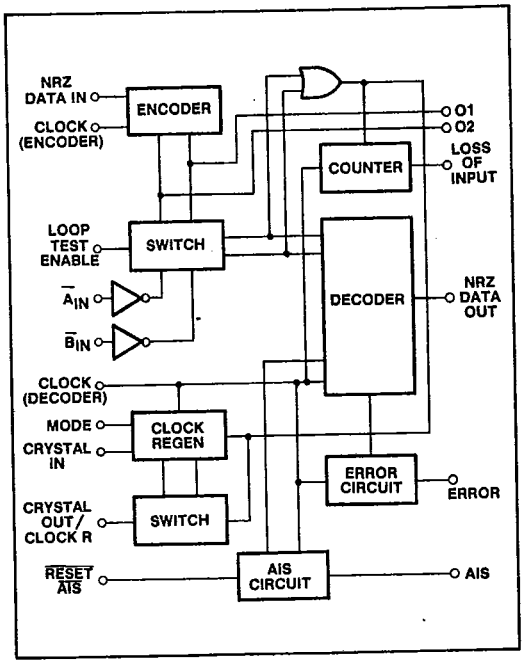

Fig.2 Block diagram

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Electrical Ratings

+Vcc	-0.5V to +7V
Inputs	Vcc +0.5V Gnd -0.3V
Outputs	Vcc, Gnd -0.3V

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ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage V_{CC} = 5V ± 0.5V Ambient temperature T_{amb} = 0°C to +70°C

Static characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min	Typ	Max		
Low level input voltage	V_{IL}	All inputs	-0.3		0.8	V	
Low level input current	I_{IL}				50	μA	V_{IL} = 0V
High level input voltage	V_{IH}		2.0		V_{CC}	V	
High level input current	I_{IH}				50	μA	V_{IH} = 5V
Low level output voltage	V_{OL}	All outputs			0.4	V	I_{sink} = 2.0mA
High level output voltage	V_{OH}		2.8			V	I_{source} = 2mA) both
			Vcc-0.75			V	I_{source} = 1mA) apply
Supply current	I_{CC}			2	4	mA	All inputs to 0V All outputs open circuit

Dynamic Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Max. Clock (Encoder) frequency	f_{maxenc}	4.0	10		MHz	Figs.10,15
Max. Clock (Decoder) frequency	f_{maxdec}	2.2	5		MHz	Figs.11,15
Propagation Delay Clock (Encoder) to O_1, O_2	$t_{pd1A/B}$			100	ns	Figs.8,10,15 See Note 1
Rise and Fall times O_1, O_2				20	ns	Figs.10,15
t_{pd1A} - t_{pd1B} difference				20	ns	Figs.10,15
Propagation Delay Clock (Encoder) to Clock Regenerate	t_{pd3}			150	ns	Loop test enable = '1', Figs.10,15
Setup time of NRZ data in to Clock (Encoder)	t_{s3}	75			ns	Figs.7,10,15
Hold time of NRZ data in	t_{h3}	55			ns	Figs.7,10,15
Propagation delay $\overline{A}_{IN}$, $\overline{B}_{IN}$ to Clock Regenerate	t_{pd2}			150	ns	Loop test enable = '0' Figs.13,15
Propagation delay Clock (Decoder) to error	t_{pd4}			200	ns	Figs.12,15
Propagation delay $\overline{\text{Reset AIS}}$ falling edge to AIS output	t_{pd5}			200	ns	Loop test enable = '0', Figs.14,15
Propagation delay Clock (Decoder) to NRZ data out	t_{pd6}			150	ns	Figs.7,11,15 See Note 2
Setup time of $\overline{A}_{IN}$, $\overline{B}_{IN}$ to Clock (Decoder)	t_{s1}	75			ns	Figs.7,11,15
Hold time of $\overline{A}_{IN}$, $\overline{B}_{IN}$ to Clock (Decoder)	t_{h1}	5			ns	Figs.7,11,15
Hold time of $\overline{\text{Reset AIS}}$ = '0'	t_{h2}	30			ns	Figs.7,14,15
Setup time Clock (Decoder) to $\overline{\text{Reset AIS}}$	t_{s2}	100			ns	Figs.7,14,15
Setup time $\overline{\text{Reset AIS}}$ = 1 to Clock (Decoder)	t_{s2}	0			ns	Figs.14,15
Propagation Delay Clock (Decoder) to LIP				150	ns	

NOTES
1. The Encoded ternary outputs (O_1, O_2) are delayed by 3.5 clock periods from NRZ Data In (Fig.3).
2. The decoded NRZ output is delayed by 3 clock periods from the HDB3 inputs ($\overline{A}_{IN}$, $\overline{B}_{IN}$) (Fig.4).

High Density Bipolar 3 (HDB3) is a pseudo-ternary signal in which the number of consecutive zeros that may occur is restricted to a maximum number of three. In any sequence of four consecutive binary zeros, the ultimate zero is substituted by a 'mark' (+ or -) of the same polarity as the previous mark, i.e. it violates AMI code (Alternate Mark Inversion) and is termed a 'violation'. To ensure parity between marks of opposite polarity, the first zero is substituted by an additional mark when there would otherwise be an even number of marks between 'violations'. Thus violations alternate in polarity.

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FUNCTIONAL DESCRIPTION

Functions Listed by pin number

1. NRZ data in
Input data for encoding into ternary form. The data is clocked by the negative-going edge of the Clock (Encoder).

2. Clock (Encoder)
Clock for encoding data on pin 1.

3. LIP
Loss of input circuit detects eleven consecutive zeros at the decoder input and then gives an output high. Any logic '1' at the input ($\overline{A}_{IN}$ or $\overline{B}_{IN}$ = '0') resets this count.

4. NRZ data out
Decoded binary data from pseudo-ternary inputs $\overline{A}_{IN}$, $\overline{B}_{IN}$

5. Clock (Decoder)
Clock for decoding data on $\overline{A}_{IN}$ and $\overline{B}_{IN}$, or O_1 and O_2 in loop test mode.

6,7. $\overline{\text{Reset AIS}}$, AIS
Logic '0' on $\overline{\text{Reset AIS}}$ resets a decoded zero counter and either resets AIS output to '0' provided 3 or more zeros have been decoded in the preceding $\overline{\text{Reset AIS}}$ = 1 period, or sets AIS to '1' if less than 3 zeros have been decoded in the preceding $\overline{\text{Reset AIS}}$ = 1 period to indicate loss of time slot Zero. Logic '1' on $\overline{\text{Reset AIS}}$ enables the internal decoded zero counter.

8. Mode
Mode at logic '1' selects internal crystal controlled clock regeneration and Mode at logic '0' selects external clock regeneration using, for example, a tuned circuit.

9. Ground
Zero volts.

10. Crystal In
Input to amplifier forming crystal oscillator when crystal is connected between pins 10 and 12. This pin may also be used as a 16.384MHz clock input if one oscillator is to be shared over several HDB3 encoders/decoders.

11. Error
A logic '1' indicates that a violation of the HDB3 encoding law has been detected i.e. 3 '1's of the same polarity.

12. Clock R/Crystal Out
If pin 8 is at '0' pin 12 is Clock Regenerate, giving OR function of $\overline{A}_{IN}$, $\overline{B}_{IN}$ for clock regeneration when pin 14 = '0', OR function of O_1, O_2 when pin 14 = '1'. If pin 8 is at '1' then pin 12 becomes Crystal Out and forms oscillator with pin 10.

13,15. $\overline{A}_{IN}$, $\overline{B}_{IN}$
Inputs representing the received ternary PCM signal. $\overline{A}_{IN}$ = '0' represents a positive going '1', $\overline{B}_{IN}$ = '0' represents a negative going '1'. $\overline{A}_{IN}$ and $\overline{B}_{IN}$ are sampled by the positive going edge of the clock decoder. $\overline{A}_{IN}$ and $\overline{B}_{IN}$ may be interchanged.

14. Loop test enable
TTL input to select normal or loop back operation. Pin 14 = '0' selects normal operation, encode and decode are independent and asynchronous. When pin 14 = '1' O_1, is connected internally to A_{IN} and O_2 to B_{IN}. Clock R becomes the OR function of O_1, O_2. N.B. A decode clock has to be supplied, or regenerated. The delay from NRZ in (pin 1) to NRZ out (pin 4) is about 7½ clock periods in loop back.

16,17. O_1, O_2
Outputs representing the ternary encoded PCM HDB3 signal for line transmission. O_1 and O_2 are in Return to zero form and are clocked out on the positive going edge of the encode clock. The length of O_1 and O_2 pulses is set by the positive clock pulse length. Use suitable line drivers from these two outputs such that O_1 gives positive going pulse and O_2 gives negative going pulse.

18. +Vcc
Positive 5V ± 10% supply.

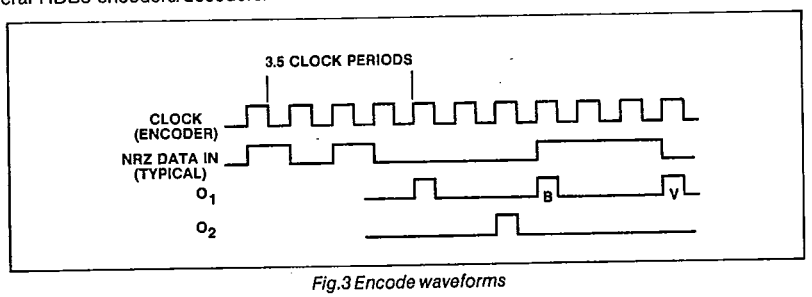

Fig.3 Encode waveforms

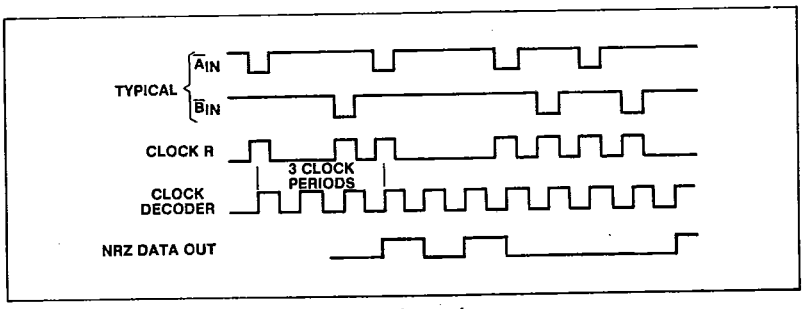

Fig.4 Decode waveforms

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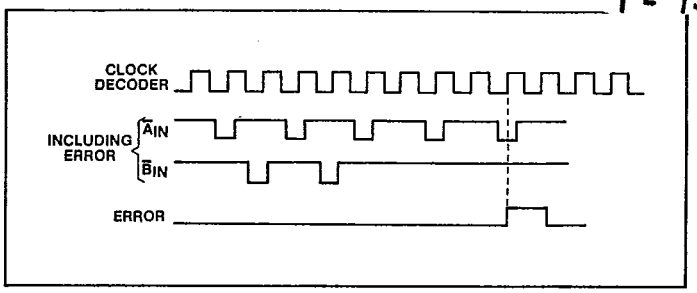

Fig.5 HDB3 error output waveforms

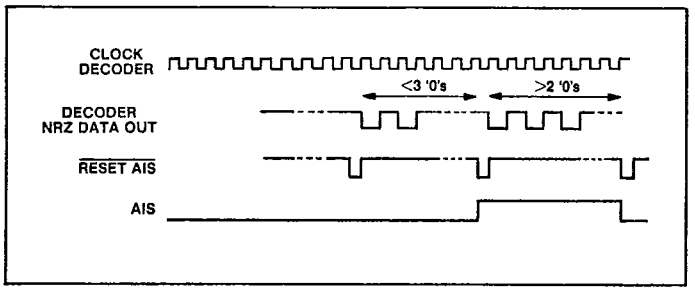

Fig.6 AIS error and Reset waveforms

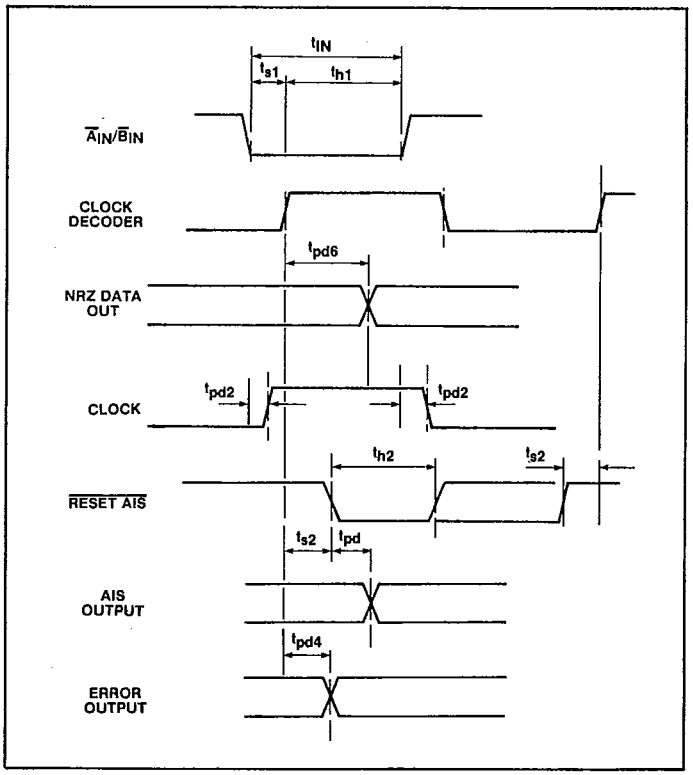

Fig.7 Decoder timing relationship

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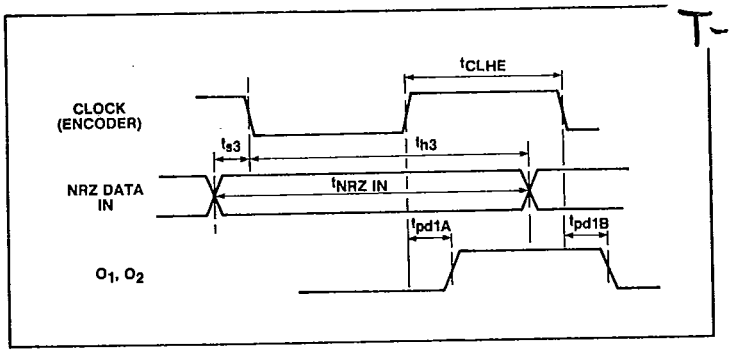

Fig.8 Encoder timing relationship

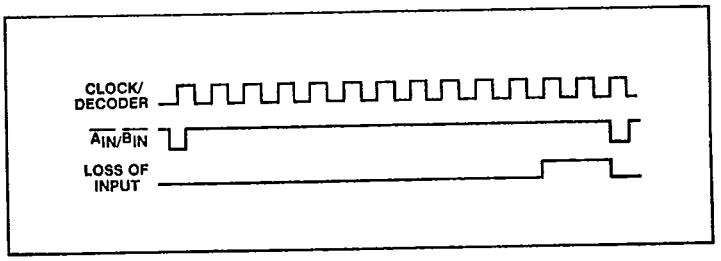

Fig.9 Loss of input waveforms

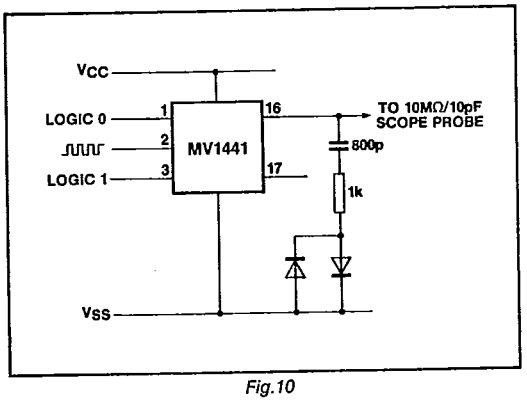

Fig.10

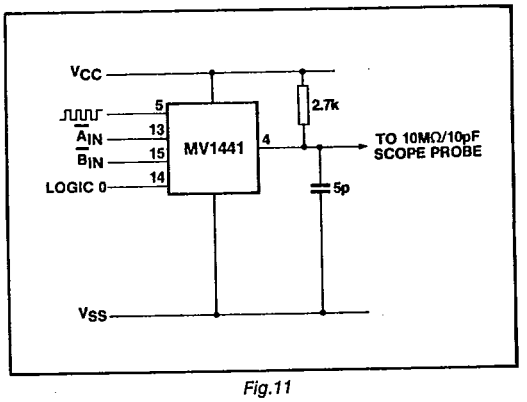

Fig.11

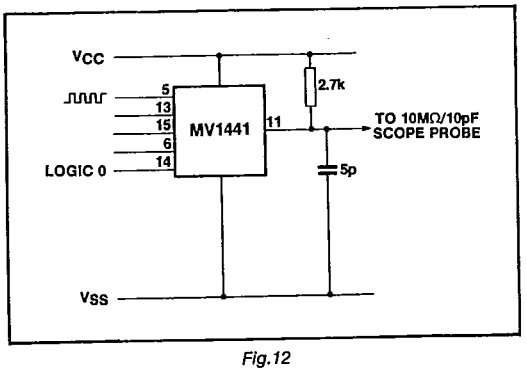

Fig.12

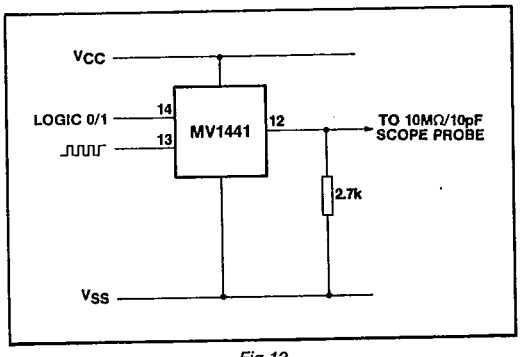

Fig.13

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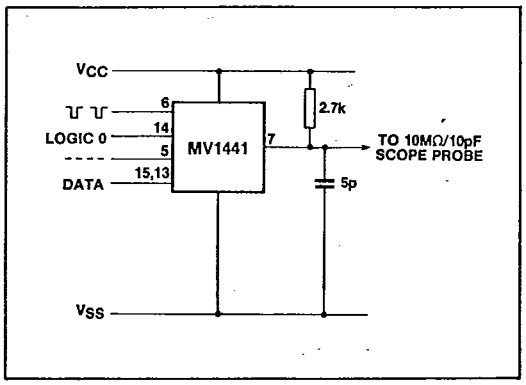

Fig.14

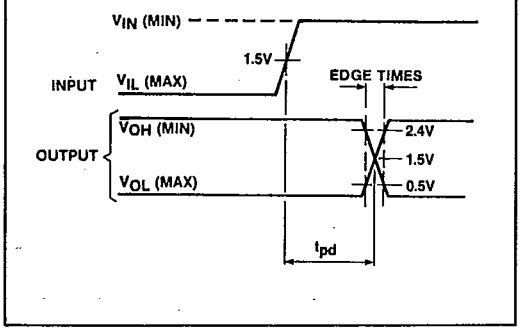

Fig.15 Test timing definitions

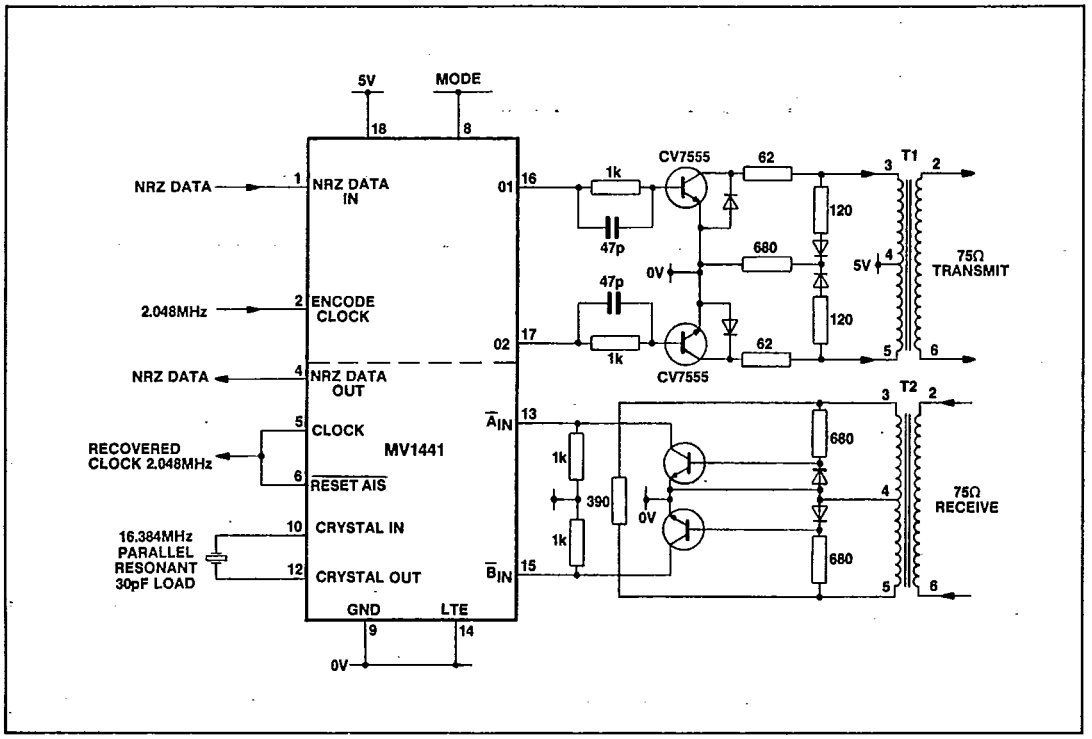

Fig.16 A typical application of the MV1441 with the interfacing to the transmission lines included