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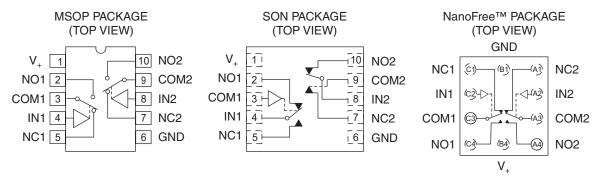
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#### **FEATURES**

- Specified Break-Before-Make Switching
- Low ON-State Resistance (0.3  $\Omega$  Max)
- Low Charge Injection
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion (THD)
- 1.65-V to 3.6-V Single-Supply Operation
- Control Inputs Are 1.8-V Logic Compatible
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

#### **APPLICATIONS**

- Cell Phones
- PDAs
- Portable Instrumentation
- Audio and Video Signal Routing
- Low-Voltage Data-Acquisition Systems
- Communication Circuits
- Modems
- Hard Drives
- Computer Peripherals
- Wireless Terminals and Peripherals



#### **DESCRIPTION/ORDERING INFORMATION**

The TS3A24159 is a dual single-pole double-throw (SPDT) analog switch that is designed to operate from 1.65 V to 3.6 V. It offers low ON-state resistance and excellent ON-state resistance matching with the break-before-make feature, to prevent signal distortion during the transferring of a signal from one channel to another. The device has excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.

#### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE	<u>(</u> 1)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	NanoFree™ (DSBGA) – YZP	Reel of 3000	TS3A24159YZPR	PREVIEW
-40°C to 85°C	VSSOP - DGS (MSOP)	Reel of 2500	TS3A24159DGSR	L8R
	QFN - DRC (SON)	Reel of 3000	TS3A24159DRCR	ZWS

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.





## SUMMARY OF CHARACTERISTICS(1)

Configuration	Dual 2:1 Multiplexer/Demultiplexer (2 × SPDT)
Number of channels	2
ON-state resistance (r <sub>on</sub> )	0.3 Ω Max
ON-state resistance match (Δr <sub>on</sub> )	0.05 Ω Max
ON-state resistance flatness (r <sub>on(flat)</sub> )	0.04 Ω Max
Turn-on/turn-off time (t <sub>ON</sub> /t <sub>OFF</sub> )	20 ns/12 ns
Break-before-make time (t <sub>BBM</sub> )	10 ns
Charge injection (Q <sub>C</sub> )	9 pC
Bandwidth (BW)	23 MHz
OFF isolation (O <sub>ISO</sub> )	–72 dB
Crosstalk (X <sub>TALK</sub> )	−96 dB
Total harmonic distortion (THD)	0.003%
Power-supply current (I <sub>+</sub> )	15 nA
Package options	10-pin MSOP, SON, WCSP

(1)  $V_+ = 2.7 \text{ V}, T_A = 25^{\circ}\text{C}$ 

#### **FUNCTION TABLE**

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
Н	OFF	ON

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## Absolute Maximum Ratings<sup>(1)(2)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT	
V <sub>+</sub>	Supply voltage range <sup>(3)</sup>		-0.5	3.6	V	
$V_{NC} V_{NO} V_{COM}$	Analog voltage range (3)(4)(5)	-0.5	V <sub>+</sub> + 0.5	V		
I <sub>I/OK</sub>	Analog port diode current	$V_{NC}$ , $V_{NO}$ , $V_{COM} < 0$	-50	50	mA	
I <sub>NC</sub>	ON-state switch current		-300	300		
I <sub>NO</sub> I <sub>COM</sub>	ON-state peak switch current <sup>(6)</sup>	$V_{NC}$ , $V_{NO}$ , $V_{COM} = 0$ to $V_{+}$	-500	500	mA	
$V_{I}$	Digital input voltage range		-0.5	3.6	V	
$I_{IK}$	Digital input clamp current (3)(4)	V <sub>1</sub> < 0	-50		mA	
l <sub>+</sub>	Continuous current through V+			100	mA	
I <sub>GND</sub>	Continuous current through GND		-100		mA	
		DGS package		165		
$\theta_{JA}$	Package thermal impedance <sup>(7)</sup>	DRC package		56.5	°C/W	
		YZP package		TBD		
T <sub>stg</sub>	Storage temperature range	-65	150	°C		

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

<sup>(2)</sup> The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

<sup>(3)</sup> All voltages are with respect to ground, unless otherwise specified.

<sup>(4)</sup> The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>(5)</sup> This value is limited to 5.5 V maximum.

<sup>(6)</sup> Pulse at 1-ms duration <10% duty cycle.

<sup>(7)</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

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## Electrical Characteristics for 3-V Supply<sup>(1)</sup>

 $V_{+}$  = 2.7 to 3.6 V,  $T_{A}$  = -40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	IS	T <sub>A</sub>	V <sub>+</sub>	MIN	TYP	MAX	UNIT	
Analog Switch										
Analog signal range	$V_{COM}, V_{NO}, V_{NC}$					0		٧+	٧	
Peak ON	r .	$0 \le (V_{NO} \text{ or } V_{NC}) \le V_+,$	Switch ON,	25°C	2.7 V		0.2	0.3	Ω	
resistance	r <sub>peak</sub>	$I_{COM} = -100 \text{ mA},$	See Figure 10	Full	2.1 V			0.35	22	
ON-state	r	$V_{NO}$ or $V_{NC} = 2 V$ ,	Switch ON,	25°C	2.7 V		0.26	0.3	Ω	
resistance	r <sub>on</sub>	$I_{COM} = -100 \text{ mA},$ See Figure 10		Full	Z.1 V			0.34	32	
ON-state	<b>.</b>	$V_{NO}$ or $V_{NC} = 2 \text{ V}, 0.8 \text{ V},$	Switch ON,	25°C	0.7.1/		0.01	0.05	0	
resistance match between channels	$\Delta r_{\sf on}$	$I_{COM} = -100 \text{ mA},$			2.7 V			0.05	Ω	
ON-state		$0 \le (V_{NO} \text{ or } V_{NC}) \le V_+,$ $I_{COM} = -100 \text{ mA},$	Switch ON, See Figure 10	25°C			0.13		Ω	
resistance flatness	r <sub>on(flat)</sub>	$V_{NO}$ or $V_{NC} = 2 \text{ V}, 0.8 \text{ V},$	Switch ON,	25°C	2.7 V		0.01	0.04	Ω	
		$I_{COM} = -100 \text{ mA},$ See Figure 10		Full				0.05	52	
NC, NO	I <sub>NC(OFF)</sub> ,	$V_{NC}$ or $V_{NO} = 1$ V, $V_{COM} = 3$ V,	Switch OFF.	25°C		-10		10		
OFF leakage current	I <sub>NO(OFF)</sub>	or $V_{NC}$ or $V_{NO} = 3 \text{ V}$ , $V_{COM} = 1 \text{ V}$ ,	See Figure 11	Full	3.6 V	-50		50	nA	
NC, NO	I <sub>NC(ON)</sub> ,	$V_{NC}$ or $V_{NO} = 1 V$ , $V_{COM} = Open$ ,	Switch ON.	25°C		-10		10	nA	
ON leakage current	I <sub>NO(ON)</sub>	or $V_{NC}$ or $V_{NO} = 3 \text{ V}$ , $V_{COM} = \text{Open}$ ,	See Figure 12	Full	3.6 V	-100		100		
COM		$V_{NC}$ or $V_{NO}$ = Open, $V_{COM}$ = 1 V,	Switch ON.	25°C		-10		10		
ON leakage current	(200 leaves) Or		See Figure 12	Full	3.6 V	-100		100	nA	
Digital Control Inpu	uts (IN1, IN2) <sup>(2</sup>	)								
Input logic high	$V_{IH}$			Full		1.4			٧	
Input logic low	$V_{IL}$			Full				0.5	<b>V</b>	
Input leakage	la. la	V <sub>1</sub> = 3.6 V or 0		25°C	25°C 3.6 V	-40	5	40	nA	
current	I <sub>IH</sub> , I <sub>IL</sub>	V1 = 3.5 V 01 0		Full	3.0 V	-50		50	ш	

 <sup>(1)</sup> The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
 (2) All unused digital inputs of the device must be held at V<sub>+</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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## Electrical Characteristics for 3-V Supply<sup>(1)</sup> (Continued)

 $V_{+} = 2.7$  to 3.6 V,  $T_{A} = -40^{\circ}$ C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CON	DITIONS	T <sub>A</sub>	٧,	MIN	TYP	MAX	UNIT
Dynamic				<u> </u>				•	
		V V	C 25 x 5	25°C	3 V		20	35	1
Turn-on time	t <sub>ON</sub>	$V_{COM} = V_+,$ $R_L = 50 \Omega,$	C <sub>L</sub> = 35 pF, See Figure 14	Full	2.7 V to 3.6 V			40	ns
		$V_{COM} = V_+,$	C <sub>L</sub> = 35 pF,	25°C	3 V		12	25	
Turn-off time	t <sub>OFF</sub>	$R_L = 50 \Omega,$	See Figure 14	Full	2.7 V to 3.6 V			30	ns
Break-before-		$\mathcal{A} = \mathcal{A} = \mathcal{A}$	C <sub>L</sub> = 35 pF,	25°C	3 V	1	10	25	
make time	t <sub>BBM</sub>	$V_{NC} = V_{NO} = V_+,$ $R_L = 50 \Omega,$	See Figure 15	Full	2.7 V to 3.6 V	0.5		30	ns
Charge injection	Q <sub>C</sub>	$V_{GEN} = 0,$ $R_{GEN} = 0,$	C <sub>L</sub> = 1 nF, See Figure 19	25°C	3 V		9		рC
NC, NO OFF capacitance	C <sub>NC(OFF)</sub> , C <sub>NO(OFF)</sub>	$V_{NC}$ or $V_{NO} = V_{+}$ or GND, Switch OFF,	See Figure 13	25°C	3 V		90		pF
NC, NO ON capacitance	C <sub>NC(ON)</sub> , C <sub>NO(ON)</sub>	$V_{NC}$ or $V_{NO} = V_{+}$ or GND, Switch ON,	See Figure 13	25°C	3 V		224		pF
COM ON capacitance	C <sub>COM(ON)</sub>	V <sub>COM</sub> = V <sub>+</sub> or GND, Switch ON,	See Figure 13	25°C	3 V		250		pF
Digital input capacitance	C <sub>I</sub>	$V_I = V_+ \text{ or GND},$	See Figure 13	25°C	3 V		2		pF
Bandwidth	BW	$R_L = 50 \Omega$ , Switch ON,	SeeFigure 16	25°C	3 V		23		MHz
OFF isolation	O <sub>ISO</sub>	$R_L = 50 \Omega$ , f = 1 MHz,	See Figure 17	25°C	3 V		-72		dB
Crosstalk	X <sub>TALK</sub>	$R_L = 50 \Omega$ , f = 1 MHz,	See Figure 18	25°C	3 V		-96		dB
Total harmonic distortion	THD	$R_L = 600 \Omega,$ $C_L = 50 \text{ pF},$	f = 20 Hz to 20 kHz, See Figure 20	25°C	3 V		0.003		%
Supply									
Positive supply current	I <sub>+</sub>	V <sub>I</sub> = V <sub>+</sub> or GND		25°C Full	3.6 V		15	100	nA μA

<sup>(1)</sup> The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

# TS3A24159 0.3-Ω DUAL SPDT ANALOG SWITCH DUAL-CHANNEL 2:1 MULTIPLEXER/DEMULTIPLEXER

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## Electrical Characteristics for 2.5-V Supply<sup>(1)</sup>

 $\rm V_{\scriptscriptstyle +} = 2.3~to~2.7~V,~T_{\rm A} = -40^{\circ}C~to~85^{\circ}C$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	3	T <sub>A</sub>	V <sub>+</sub>	MIN	TYP	MAX	UNIT	
Analog Switch	I.									
Analog signal range	$V_{COM}, V_{NO}, V_{NC}$					0		V <sub>+</sub>	V	
Peak ON	r .	$0 \le (V_{NO} \text{ or } V_{NC}) \le V_+,$	Switch ON,	25°C	2.3 V			0.35	Ω	
resistance	r <sub>peak</sub>	$I_{COM} = -8 \text{ mA},$	See Figure 10	Full	2.5 V			0.45	52	
ON-state	r <sub>on</sub>	$V_{NO}$ or $V_{NC} = 1.8 \text{ V}$ ,	Switch ON,	25°C	2.3 V				Ω	
resistance	$I_{COM} = -8 \text{ mA},$ See Figure 10		Full	2.5 V			0.4	52		
ON-state		$V_{NO}$ or $V_{NC} = 1.8 \text{ V}, 0.8 \text{ V},$	Switch ON,	25°C	001/		0.01	0.05		
resistance match between channels	$\Delta r_{\sf on}$	$I_{COM} = -8 \text{ mA},$			2.3 V		0.05	0.05	Ω	
ON-state		$0 \le (V_{NO} \text{ or } V_{NC}) \le V_+,$ $I_{COM} = -8 \text{ mA},$	Switch ON, See Figure 10	25°C			0.05		Ω	
resistance flatness	r <sub>on(flat)</sub>	$V_{NO}$ or $V_{NC} = 0.8 \text{ V}, 1.8 \text{ V},$	Switch ON,	25°C	2.3 V		0.03	0.08		
	$I_{COM} = -8 \text{ mA},$ See Figure 10	Full				0.1	Ì			
NC, NO	I <sub>NC(OFF)</sub> ,	$V_{NC}$ or $V_{NO} = 0.5 \text{ V}$ , $V_{COM} = 2.2 \text{ V}$ ,	Switch OFF.	25°C		-10		10		
OFF leakage current	I <sub>NO(OFF)</sub>	or $V_{NC}$ or $V_{NO} = 2.2 \text{ V}, V_{COM} = 0.5 \text{ V},$	See Figure 11	Full	2.7 V	-50		50	nA	
NC, NO	I <sub>NC(ON)</sub> ,	$V_{NC}$ or $V_{NO} = 0.5 \text{ V}$ , $V_{COM} = \text{Open}$ ,	Switch ON,	25°C		-10		10		
ON leakage current	I <sub>NO(ON)</sub>	or $V_{NC}$ or $V_{NO} = 2.2 \text{ V}$ , $V_{COM} = \text{Open}$ ,	See Figure 12	Full	2.7 V	-100		100	nA	
СОМ		$V_{NC}$ or $V_{NO}$ = Open, $V_{COM}$ = 0.5 V,	Switch ON,	25°C		-10		10		
ON leakage current	I <sub>COM(ON)</sub>	$I_{COM(ON)}$ or $V_{NC}$ or $V_{NO}$ = Open, $V_{COM}$ = 2.2 V, See Figure 12		Full	2.7 V	-100		100	nA	
Digital Control Inpu	uts (IN1, IN2) <sup>(2</sup>	)				•				
Input logic high	$V_{IH}$			Full		1.25			V	
Input logic low	$V_{IL}$			Full				0.5	<b>V</b>	
Input leakage		V <sub>I</sub> = 2.7 V or 0		25°C	2.7 V	-40	5	40	nA	
current	I <sub>IH</sub> , I <sub>IL</sub>	V  - 2.7 V 01 0		Full	Z.1 V	-50		50	11/1	

 <sup>(1)</sup> The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
 (2) All unused digital inputs of the device must be held at V<sub>+</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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## Electrical Characteristics for 2.5-V Supply<sup>(1)</sup> (Continued)

 $V_{+} = 2.3$  to 2.7 V,  $T_{A} = -40^{\circ}$ C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CON	IDITIONS	T <sub>A</sub>	٧,	MIN	TYP	MAX	UNIT
Dynamic					,				
		V V	0 25 5	25°C	2.5 V		23	45	
Turn-on time	t <sub>ON</sub>	$V_{COM} = V_+,$ $R_L = 50 \Omega,$	C <sub>L</sub> = 35 pF, See Figure 14	Full	2.3 V to 2.7 V			50	ns
		V - V	C = 25 pE	25°C	2.5 V		17	27	
Turn-off time	t <sub>OFF</sub>	$V_{COM} = V_+,$ $R_L = 50 \Omega,$	C <sub>L</sub> = 35 pF, See Figure 14		2.3 V to 2.7 V			30	ns
Dunal, hafana		\(\lambda \) \(\lambda \)	0 25 -5	25°C	2.5 V	2	14	30	
Break-before- make time	t <sub>BBM</sub>	$V_{NC} = V_{NO} = V_+,$ $R_L = 50 \Omega,$	C <sub>L</sub> = 35 pF, See Figure 15	Full	2.3 V to 2.7 V	1		35	ns
Charge injection	Q <sub>C</sub>	V <sub>GEN</sub> = 0, R <sub>GEN</sub> = 0,	C <sub>L</sub> = 1 nF, See Figure 19	25°C	2.5 V		8		рС
NC, NO OFF capacitance	C <sub>NC(OFF)</sub> , C <sub>NO(OFF)</sub>	$V_{NC}$ or $V_{NO} = V_{+}$ or GND, Switch OFF,	See Figure 13	25°C	2.5 V		90		pF
NC, NO ON capacitance	C <sub>NC(ON)</sub> , C <sub>NO(ON)</sub>	$V_{NC}$ or $V_{NO} = V_{+}$ or GND, Switch ON,	See Figure 13	25°C	2.5 V		250		pF
COM ON capacitance	C <sub>COM(ON)</sub>	V <sub>COM</sub> = V <sub>+</sub> or GND, Switch ON,	See Figure 13	25°C	2.5 V		250		pF
Digital input capacitance	C <sub>I</sub>	$V_I = V_+ \text{ or GND},$	See Figure 13	25°C	2.5 V		2		pF
Bandwidth	BW	$R_L = 50 \Omega$ , Switch ON,	See Figure 16	25°C	2.5 V		23		MHz
OFF isolation	O <sub>ISO</sub>	$R_L = 50 \Omega$ , f = 1 MHz,	See Figure 17	25°C	2.5 V		-72		dB
Crosstalk	X <sub>TALK</sub>	$R_L = 50 \Omega$ , f = 1 MHz,	See Figure 18	25°C	2.5 V		-96		dB
Total harmonic distortion	THD	$R_L = 600 \Omega,$ $C_L = 50 pF,$	f = 20 Hz to 20 kHz, See Figure 20	25°C	2.5 V		0.003		%
Supply	·			,	·				
Positive supply		V V or CND		25°C	271/		10	100	<b>~</b> ^
current	I <sub>+</sub>	$V_I = V_+ \text{ or GND}$		Full	2.7 V			700	nA

<sup>(1)</sup> The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

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## Electrical Characteristics for 1.8-V Supply<sup>(1)</sup>

 $V_{+}$  = 1.65 to 1.95 V,  $T_{A}$  = -40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	;	T <sub>A</sub>	V <sub>+</sub>	MIN	TYP	MAX	UNIT	
Analog Switch	-							·		
Analog signal range	$V_{COM}, V_{NO}, V_{NC}$					0		V <sub>+</sub>	V	
Peak ON	r .	$0 \le (V_{NO} \text{ or } V_{NC}) \le V_+,$	Switch ON,	25°C	1.65 V		0.4	0.9	Ω	
resistance	r <sub>peak</sub>	$I_{COM} = -2 \text{ mA},$	See Figure 10	Full	1.00 V			8.0	22	
ON-state	r	$V_{NO}$ or $V_{NC} = 1.5 V$ ,	Switch ON,	25°C	1.65 V		0.3	0.45	Ω	
resistance	r <sub>on</sub>	$I_{COM} = -2 \text{ mA},$	See Figure 10	Full	1.05 V			0.5	22	
ON-state			0 11 011	25°C			0.02	0.04		
resistance match between channels	$\Delta r_{\sf on}$	$V_{NO}$ or $V_{NC} = 0.6 \text{ V}$ , 1.5 V, $I_{COM} = -2 \text{ mA}$ ,	Switch ON, See Figure 10	Full	1.65 V			0.05	Ω	
ON-state		$0 \le (V_{NO} \text{ or } V_{NC}) \le V_+,$ $I_{COM} = -2 \text{ mA},$	Switch ON, See Figure 10	25°C			0.13			
resistance flatness	On(nat)	$V_{NO}$ or $V_{NC} = 0.6 \text{ V}, 1.5 \text{ V},$	Switch ON,	25°C	1.65 V		0.08	0.15	Ω	
nati icos		$I_{COM} = -8 \text{ mA},$	See Figure 10	Full				0.2		
NC, NO	I <sub>NC(OFF)</sub> ,	$V_{NC}$ or $V_{NO} = 0.3 \text{ V}$ , $V_{COM} = 1.65 \text{ V}$ ,	Switch OFF.	25°C		-10		10		
OFF leakage current	I <sub>NO(OFF)</sub>	or $V_{NC}$ or $V_{NO} = 1.65 \text{ V}$ , $V_{COM} = 0.3 \text{ V}$ ,	See Figure 11	Full	1.95	-50		50	nA	
NC, NO	I <sub>NC(ON)</sub> ,	$V_{NC}$ or $V_{NO} = 0.3 \text{ V}$ , $V_{COM} = \text{Open}$ ,	Switch ON,	25°C	4.05.1/	-10		10		
ON leakage current	I <sub>NO(ON)</sub>	or $V_{NC}$ or $V_{NO} = 1.65 \text{ V}$ , $V_{COM} = \text{Open}$ ,	See Figure 12	Full	1.95 V	-100		100	nA	
COM		$V_{NC}$ or $V_{NO}$ = Open, $V_{COM}$ = 0.3 V,	Switch ON.	25°C		-10		10		
ON leakage current	January Or Switch ON,		See Figure 12	Full	1.95 V	-100		100	100 nA	
Digital Control Inp	outs (IN1, IN2)	(2)								
Input logic high	$V_{IH}$		<u> </u>	Full		1			V	
Input logic low	V <sub>IL</sub>			Full				0.4	V	
Input leakage		V <sub>I</sub> = 1.95 V or 0		25°C	1.95 V	-40	5	40	nA	
current	l <sub>IH</sub> , l <sub>IL</sub>	V  = 1.33 V OI U		Full	1.95 V	-50		50	IIA	

<sup>(1)</sup> The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

<sup>(2)</sup> All unused digital inputs of the device must be held at V<sub>+</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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## Electrical Characteristics for 1.8-V Supply<sup>(1)</sup> (Continued)

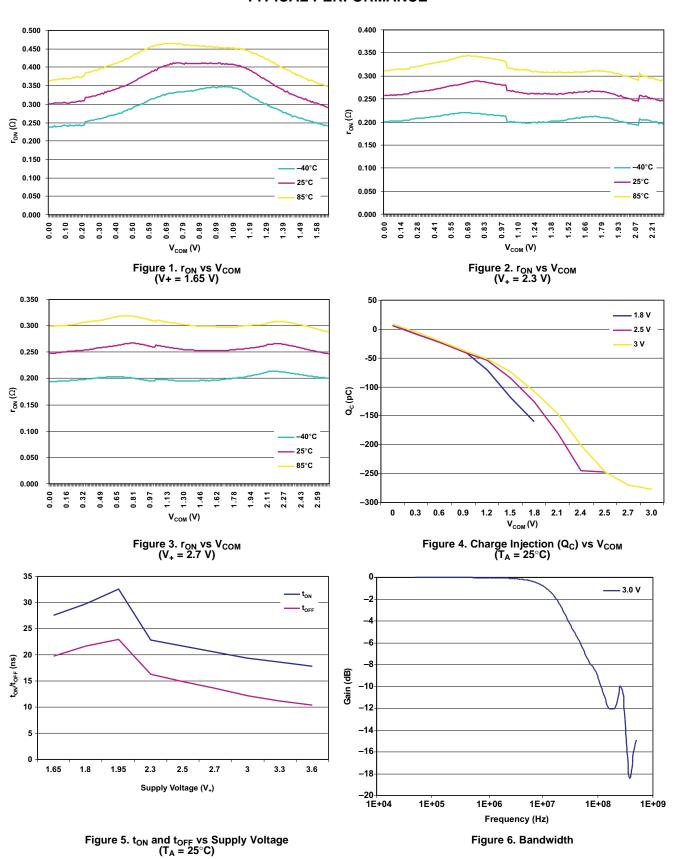
 $V_{+}$  = 1.65 to 1.95 V,  $T_{A}$  = -40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CON	DITIONS	T <sub>A</sub>	V <sub>+</sub>	MIN	TYP	MAX	UNIT
Dynamic									
		V V	0 05 = 5	25°C	1.8 V		53	75	
Turn-on time	t <sub>ON</sub>	$V_{COM} = V_+,$ $R_L = 50 \Omega,$	C <sub>L</sub> = 35 pF, See Figure 14	Full	1.65 V to 1.95 V			30	ns
		V - V	C = 25 pE	25°C	1.8 V		24	35	
Turn-off time	t <sub>OFF</sub>	$V_{COM} = V_+,$ $R_L = 50 \Omega,$	C <sub>L</sub> = 35 pF, See Figure 14		1.65 V to 1.95 V			40	ns
Break-before-	., .,	W W W	C 25 nF	25°C	1.8 V	2	30	40	
make time	t <sub>BBM</sub>	$V_{NC} = V_{NO} = V_+,$ $R_L = 50 \Omega,$	C <sub>L</sub> = 35 pF, See Figure 15	Full	1.65 V to 1.95 V	1		50	ns
Charge injection	Q <sub>C</sub>	$V_{GEN} = 0,$ $R_{GEN} = 0,$	C <sub>L</sub> = 1 nF, SeeFigure 19	25°C	1.8 V		5		pC
NC, NO OFF capacitance	$C_{NC(OFF)}, \\ C_{NO(OFF)}$	$V_{NC}$ or $V_{NO} = V_{+}$ or GND, Switch OFF,	See Figure 13	25°C	1.8 V		90		pF
NC, NO ON capacitance	$C_{NC(ON)}, \\ C_{NO(ON)}$	$V_{NC}$ or $V_{NO} = V_{+}$ or GND, Switch ON,	See Figure 13	25°C	1.8 V		250		pF
COM ON capacitance	C <sub>COM(ON)</sub>	V <sub>COM</sub> = V <sub>+</sub> or GND, Switch ON,	See Figure 13	25°C	1.8 V		250		pF
Digital input capacitance	C <sub>I</sub>	$V_I = V_+ \text{ or GND},$	See Figure 13	25°C	1.8 V		2		pF
Bandwidth	BW	$R_L = 50 \Omega$ , Switch ON,	See Figure 16	25°C	1.8 V		23		MHz
OFF isolation	O <sub>ISO</sub>	$R_L = 50 \Omega$ , f = 1 MHz,	See Figure 17	25°C	1.8 V		-73		dB
Crosstalk	X <sub>TALK</sub>	$R_L = 50 \Omega$ , f = 1 MHz,	See Figure 18	25°C	1.8 V		-97		dB
Total harmonic distortion	THD	$R_L = 600 \Omega,$ $C_L = 50 pF,$	f = 20 Hz to 20 kHz, See Figure 20	25°C	1.8 V		0.005		%
Supply		•		•	,				
Positive supply		V V as CND		25°C	4.05.1/		100	50	^
current	I <sub>+</sub>	$V_1 = V_+ \text{ or GND}$		Full	1.95 V			700	nA

<sup>(1)</sup> The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

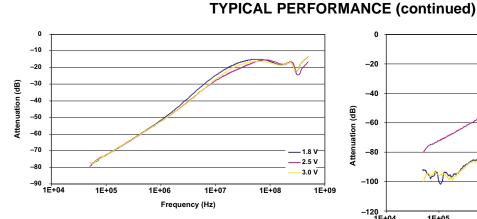


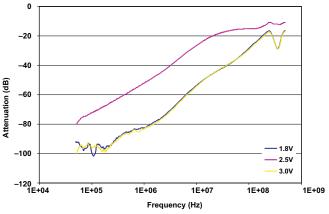
#### **TYPICAL PERFORMANCE**











SCDS238-MARCH 2007

Figure 7. OFF Isolation

Figure 8. Crosstalk

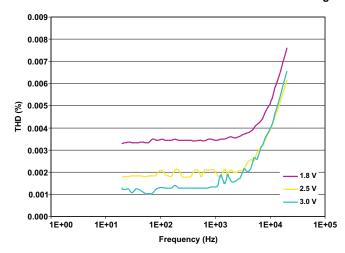


Figure 9. Total Harmonic Distortion vs Frequency



#### PARAMETER MEASUREMENT INFORMATION

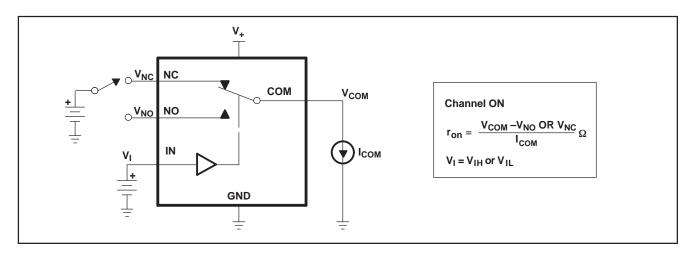


Figure 10. ON-State Resistance

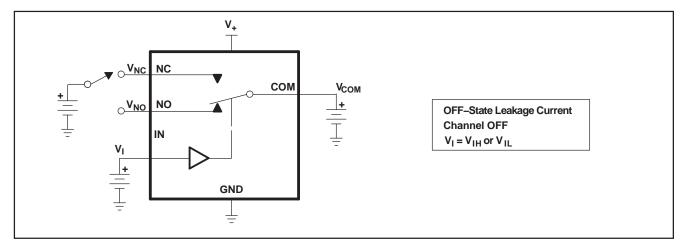


Figure 11. OFF-State Leakage Current (I<sub>NC(OFF)</sub>, I<sub>NO(OFF)</sub>, I<sub>NO(OFF)</sub>, I<sub>NO(OFF)</sub>, I<sub>COM(OFF)</sub>, I<sub>COM(PWROFF)</sub>)

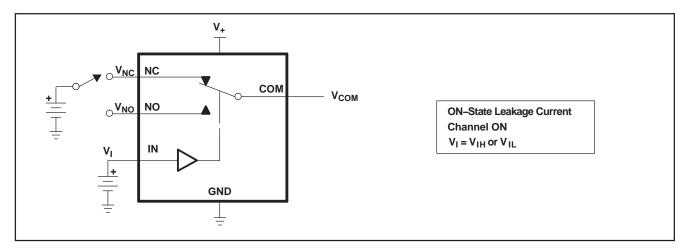


Figure 12. ON-State Leakage Current (I<sub>COM(ON)</sub>, I<sub>NC(ON)</sub>, I<sub>NO(ON)</sub>)





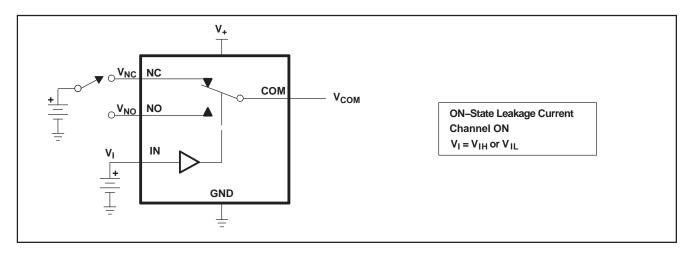
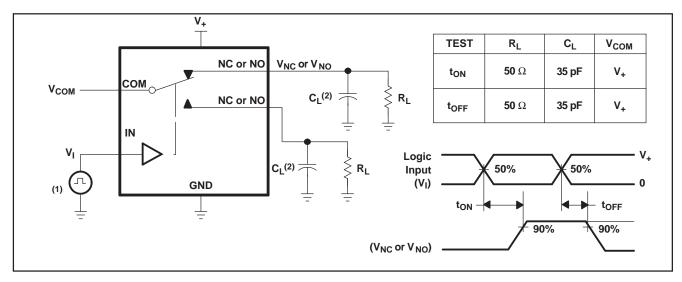


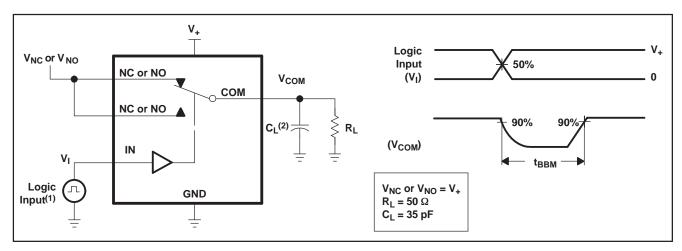
Figure 13. Capacitance (C<sub>I</sub>, C<sub>NC(OFF)</sub>, C<sub>NO(OFF)</sub>, C<sub>NC(ON)</sub>, C<sub>NO(ON)</sub>)



- (1) All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5 \text{ ns}$ ,  $t_f < 5 \text{ ns}$ .
- (2) C<sub>L</sub> includes probe and jig capacitance.

Figure 14. Turn-On (t<sub>ON</sub>) and Turn-Off Time (t<sub>OFF</sub>)





- (1) All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5$  ns,  $t_f < 5$  ns.
- (2)  $C_L$  includes probe and jig capacitance.

Figure 15. Break-Before-Make Time (t<sub>BBM</sub>)

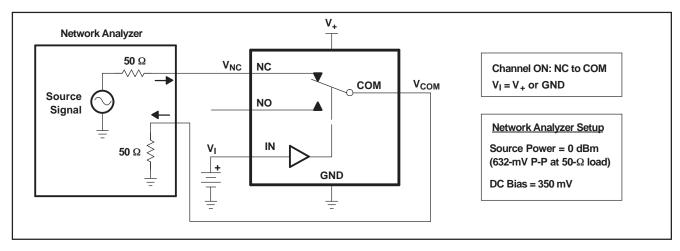


Figure 16. Bandwidth (BW)





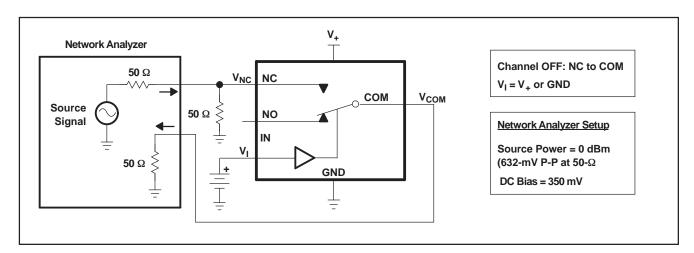


Figure 17. OFF Isolation (O<sub>ISO</sub>)

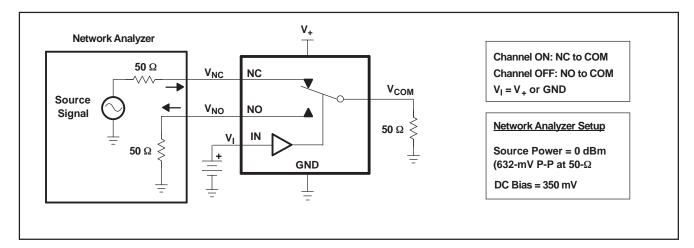
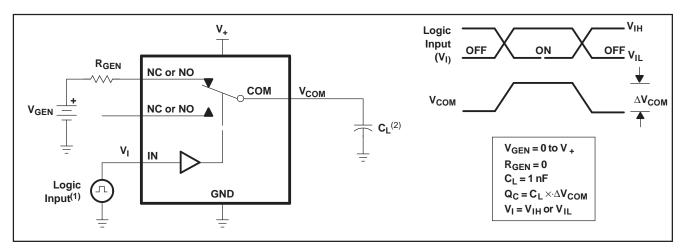


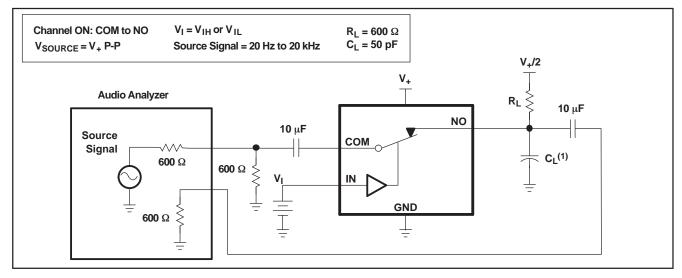
Figure 18. Crosstalk (X<sub>TALK</sub>)





- (1) All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5 \text{ ns}$ ,  $t_f < 5 \text{ ns}$ .
- (2)  $C_L$  includes probe and jig capacitance.

Figure 19. Charge Injection (Q<sub>C</sub>)



(1) C<sub>I</sub> includes probe and jig capacitance.

Figure 20. Total Harmonic Distortion (THD)





com 17-May-2007

#### PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TS3A24159DGSR	ACTIVE	MSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3A24159DGSRG4	ACTIVE	MSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3A24159DRCR	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TS3A24159DRCRG4	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## DGS (S-PDSO-G10)

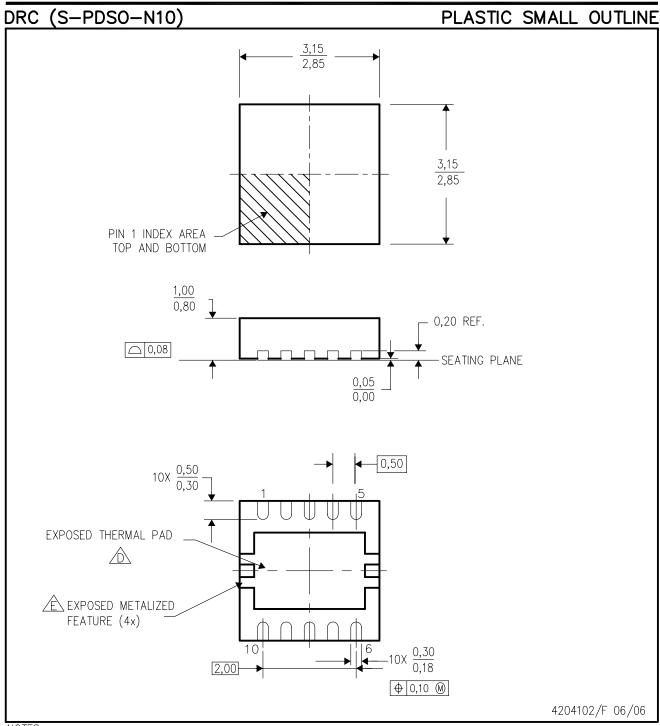
## PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Falls within JEDEC MO-187 variation BA.





NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.

- B. This drawing is subject to change without notice.
- C. Small Outline No-Lead (SON) package configuration.

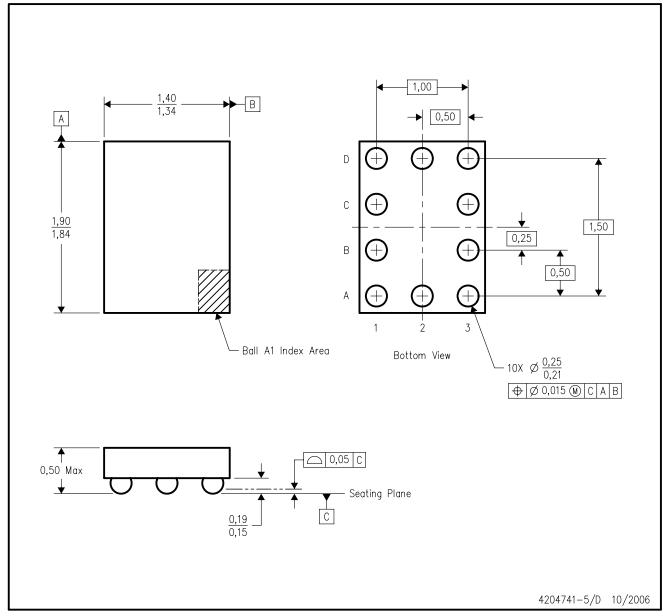
The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

Æ Metalized features are supplier options and may not be on the package.



## YZP (R-XBGA-N10)

## DIE-SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. NanoFree  $^{\text{TM}}$  package configuration.
- D. This package is a lead-free solder ball design.

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