

54FCT373

Octal Transparent Latch with TRI-STATE® Outputs

General Description

The 54FCT373 consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state.

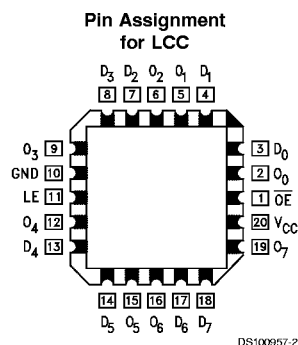
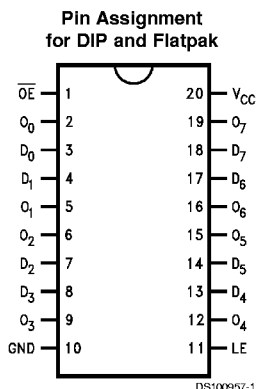
Features

- TRI-STATE outputs for bus interfacing
- TTL input and output level compatible
- CMOS power consumption
- Output sink capability of 32 mA, source capability of 12 mA
- Standard Microcircuit Drawing (SMD) 5962-8764401

Ordering Code

Military	Package Number	Package Description
54FCT373DMQB	J20A	20-Lead Ceramic Dual-In-Line
54FCT373FMQB	W20A	20-Lead Cerpack
54FCT373LMQB	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Connection Diagrams



Pin Names	Description
D ₀ –D ₇	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	Output Enable Input (Active LOW)
O ₀ –O ₇	TRI-STATE Latch Outputs

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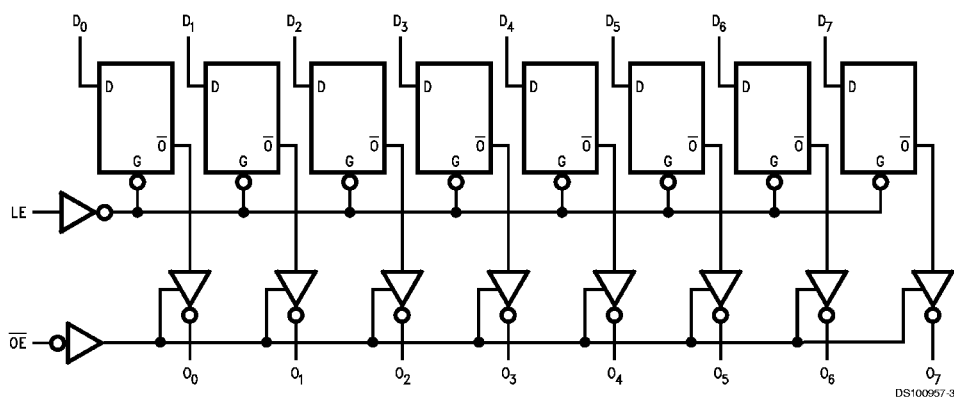
Functional Description

The 54FCT373 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Inputs			Output
LE	$\overline{OE}$	D_n	O_n
H	L	H	H
H	L	L	L
L	L	X	O_n (no change)
X	H	X	Z

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance State

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	–65°C to +150°C
Ambient Temperature under Bias	–55°C to +125°C
Junction Temperature under Bias Ceramic	–55°C to +175°C
V _{CC} Pin Potential to Ground Pin	–0.5V to +7.0V
Input Voltage (Note 2)	–0.5V to +7.0V
Input Current (Note 2)	–30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State	–0.5V to +5.5V

in the HIGH State
Current Applied to Output
in LOW State (Max) –0.5V to V_{CC}
twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature Military	–55°C to +125°C
Supply Voltage Military	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		FCT240		Units	V _{CC}	Conditions
			Min	Max			
V _{IH}	Input HIGH Voltage		2.0		V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage			–1.2	V	Min	I _{IN} = –18 mA
V _{OH}	Output HIGH Voltage	54FCT	4.3		V	Min	I _{OH} = –300 μ A
		54FCT	2.4		V	Min	I _{OH} = –12 mA
V _{OL}	Output LOW Voltage	54FCT		0.2	V	Min	I _{OL} = 300 μ A
		54FCT		0.5	V	Min	I _{OL} = 32 mA
I _{IH}	Input HIGH Current			5	μ A	Max	V _{IN} = 5.5V
I _{IL}	Input LOW Current			–5	μ A	Max	V _{IN} = 0.0V
I _{OZH}	High Impedance Output Current			10	μ A	Max	V _{IN} = 5.5V
I _{OZL}	High Impedance Output Current			–10	μ A	Max	V _{IN} = 0.0V
I _{OS}	Output Short-Circuit Current			–60	mA	Max	V _{OUT} = 0.0V
I _{CCQ}	Power Supply Current			1.5	mA	Max	V _{IN} = 0.2V or V _{IN} = 5.3V
Δ I _{CC}	Power Supply Current			2.0	mA	Max	V _{IN} = 3.4V
I _{CCT}	Total Power Supply Current			5.6	mA	Max	V _{IN} = 3.4V or V _{IN} = GND, $\overline{OE}$ = GND, f _i = 10Mhz, outputs open, one bit toggling, 50% duty cycle
				4.0	mA	Max	V _{IN} = 5.3V or V _{IN} = 0.2V, $\overline{OE}$ = GND, f _i = 10Mhz, outputs open, one bit toggling, 50% duty cycle
I _{CCD}	Dynamic I _{CC}			0.25	mA/MHz	Max	Outputs Open, $\overline{OE}$ = GND, one bit toggling, 50% duty Cycle

AC Electrical Characteristics

Symbol	Parameter	54FCT		Units	Fig. No.
		$T_A = -55^{\circ}\text{C to }+125^{\circ}\text{C}$ $V_{CC} = 4.5\text{V to }5.5\text{V}$ $C_L = 50\text{ pF}$			
		Min	Max		
t_{PLH}	Propagation Delay	1.5	8.5	ns	Figure 4
t_{PHL}	D_n to O_n	1.5	8.5		
t_{PLH}	Propagation Delay	2.0	15.0	ns	Figure 4
t_{PHL}	LE to O_n	2.0	15.0		
t_{PZH}	Output Enable Time	1.5	13.5	ns	Figure 6
t_{PZL}		1.5	13.5		
t_{PHZ}	Output Disable Time	1.5	12.5	ns	Figure 6
t_{PLZ}		1.5	12.5		

AC Operating Requirements

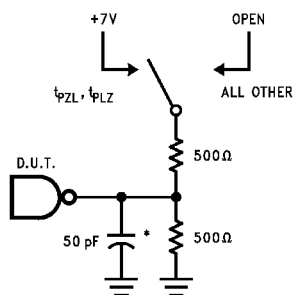
Symbol	Parameter	54FCT		Units	Fig. No.
		T _A = −55° C to +125° C V _{CC} = 4.5V to 5.5V C _L = 50 pF			
		Min	Max		
t _s (H)	Setup Time, HIGH	2.0		ns	Figure 7
t _s (L)	or LOW D _n to LE	2.0			
t _h (H)	Hold Time, HIGH	3.0		ns	Figure 7
t _h (L)	or LOW D _n to LE	3.0			
t _w (H)	Pulse Width, LE HIGH	6.0		ns	Figure 5

Capacitance

Symbol	Parameter	Max	Units	Conditions ($T_A = 25^{\circ}\text{C}$)
C_{IN}	Input Capacitance	10	pF	$V_{CC} = 0\text{V}$
C_{OUT} (Note 3)	Output Capacitance	12	pF	$V_{CC} = 5.0\text{V}$

Note 3: C_{OUT} is measured at frequency $f = 1\text{ MHz}$, per MIL-STD-883B, Method 3012.

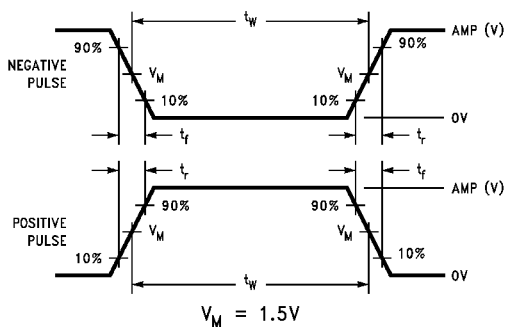
AC Loading



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*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

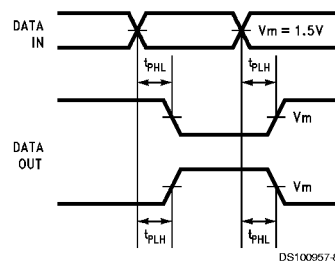


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FIGURE 2. Test Input Signal Levels

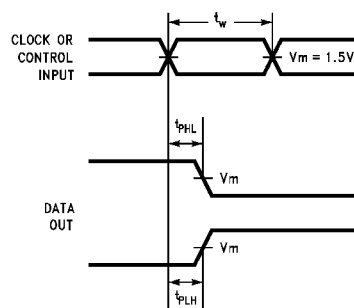
Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements



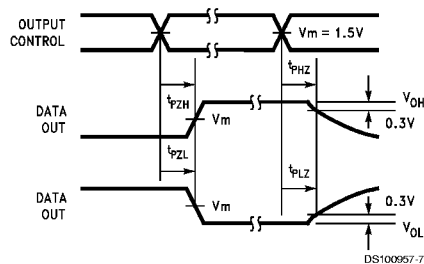
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FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions



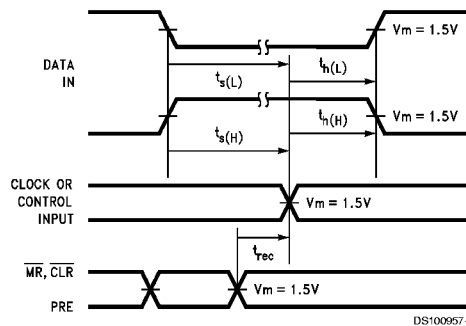
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FIGURE 5. Propagation Delay, Pulse Width Waveforms



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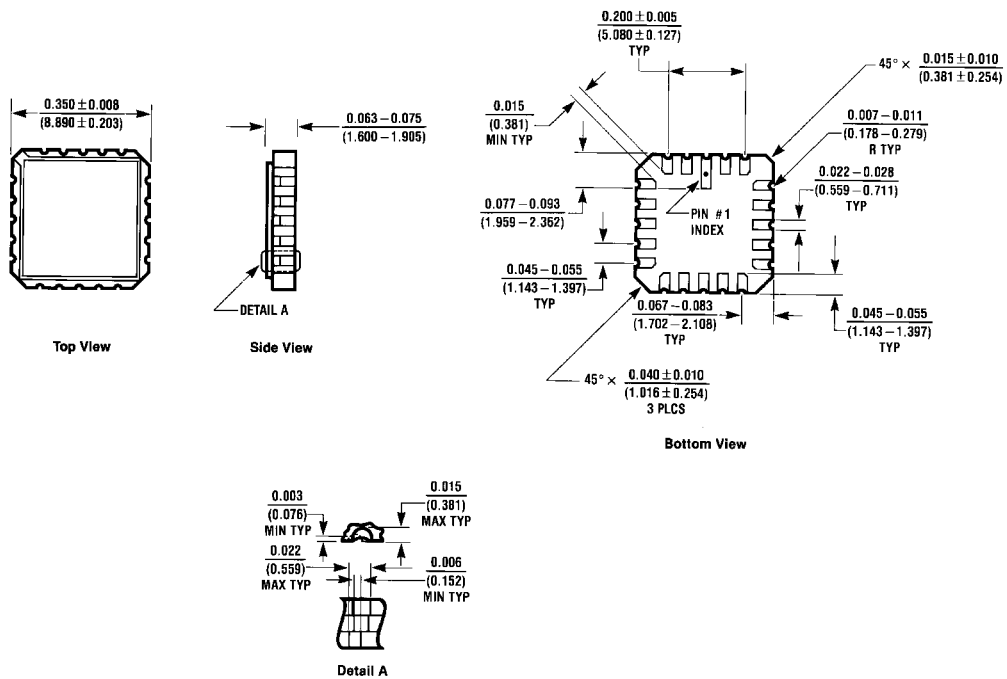
FIGURE 6. TRI-STATE Output HIGH and LOW Enable and Disable Times



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FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

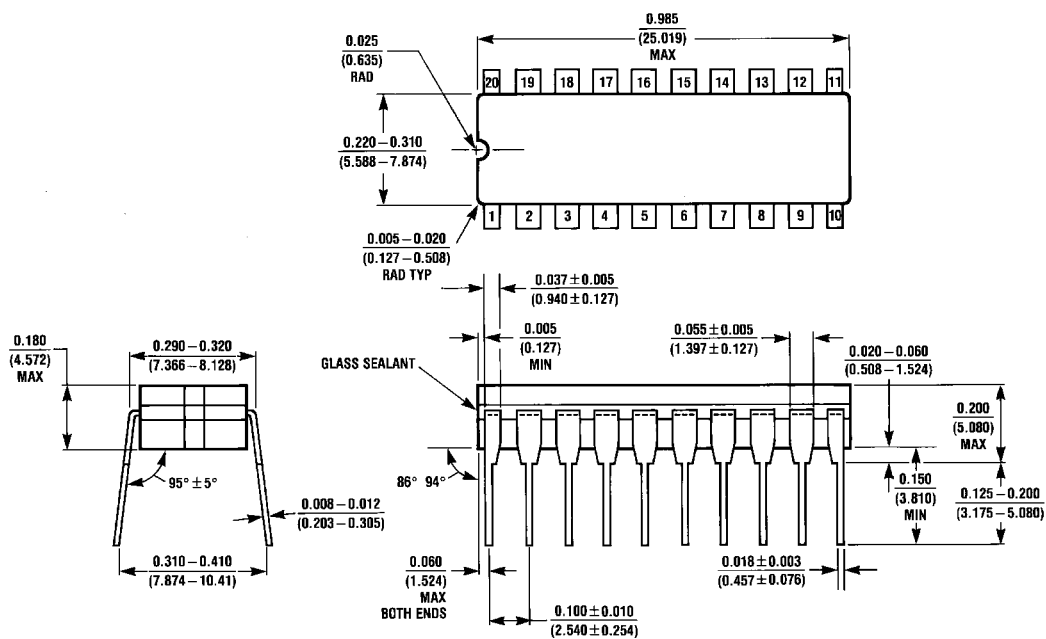
Physical Dimensions inches (millimeters) unless otherwise noted



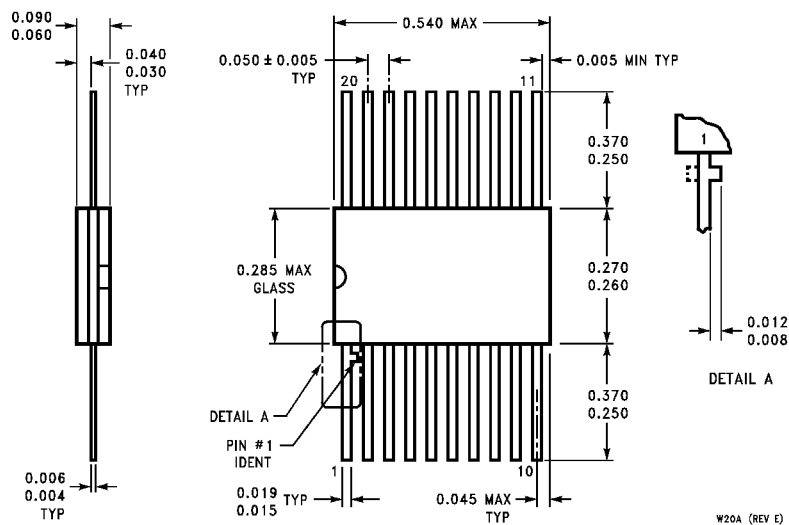
E20A (REV D)

20-Terminal Ceramic Chip Carrier (L)
NS Package Number E20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Ceramic Dual-In-Line (D)
NS Package Number J20A



20-Lead Ceramic Flatpak (F)
NS Package Number W20A