Marconi
Electronic Devices

54 HST 630

Radiation Hard 16-Bit Parallel Error Detection & Correction

FEATURES

- Radiation Hard to 1 MRad (Si)
- High SEU immunity, latch up free
- CMOS-SOS technology
- All inputs & outputs fully TTL & CMOS compatible
- Low power
- Detects and corrects single-bit errors
- Detects and flags dual-bit errors
- High speed:
  Write cycle- Generate checkword in 40ns typ.
  Read cycle- Flags errors in 20ns typ.

BLOCK DIAGRAM

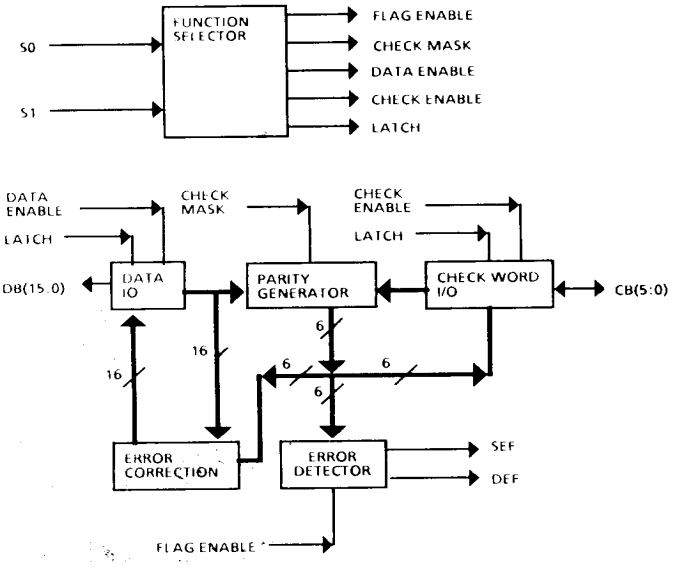

Figure 1

GENERAL DESCRIPTION

The 54HST630 is a 16-bit parallel Error Detection and Correction circuit. It uses a modified Hamming code to generate a 6-bit check word from each 16-bit data word. The check word is stored with the data word during a memory write cycle. During a memory read cycle a 22-bit word is taken from memory and checked for errors.

Single bit errors in data words are flagged and corrected. Single bit errors in check words are flagged but not corrected. The position of the incorrect bit is pinpointed, in both cases, by the 6-bit error syndrome code which is output during the error correction cycle.

Two bit errors are flagged but not corrected. Any combination of two bit errors occurring within the 22-bit word read from memory (ie two errors in the 16-bit data word, two bits in the 16-bit check word or one error in each) will be correctly identified.

The gross errors of all bits, low or high, will be deleted.

The control signals S1 and S0 select the function to be performed by the EDAC. They control the generation of check words and the latching and correction of data (see table 1). When errors are detected, flags are placed on outputs SEF and DEF (see table 2).

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C600D Issue 1 Nov. 1988

GENERAL DESCRIPTION (cont.)

TABLE 1 - CONTROL FUNCTIONS

MEMORY CYCLE	CONTROL		EDAC FUNCTION	DATA I/O	CHECKWORD	ERROR FLAGS	
	S1	S0				SEF	DEF
WRITE	Low	Low	Generates Checkword	Input Data	Output Checkword	Low	Low
READ	Low	High	Read Data &Checkword	Input Data	Input Checkword	Low	Low
READ	High	High	Latch & Flag Error	Latch Data	Latch Checkword	Enabled	Enabled
READ	High	Low	Correct Data Word & Generate Syndrome Bits	Output Corrected Data	Output Syndrome Bits	Enabled	Enabled

TABLE 2 - ERROR FUNCTIONS

TOTAL NUMBER OF ERRORS		ERROR FLAGS		DATA CORRECTION
16-BIT DATA	6-BIT CHECKWORD	SEF	DEF	
0	0	Low	Low	Not Applicable
1	0	High	Low	Correction
0	1	High	Low	Correction
1	1	High	High	Interrupt
2	0	High	High	Interrupt
0	2	High	High	Interrupt

ERROR DETECTION & CORRECTION

During a memory write cycle, six check bits (CB0-CB5) are generated by eight-input parity generators using the data bits as defined in Table 3. overleaf. During a memory read cycle, the 6-bit checkword is retrieved along with the actual data.

Error detection is accomplished as the 6-bit checkword and the 16-bit data word from memory are applied to internal parity generators/checkers. If the parity of all six groupings of data and check bits are correct, it is assumed that no error has occurred and both error flags will be low. (It should be noted that the sense of two of the check bits, bits CB0 and CB1, is inverted to ensure that the gross-error condition of all lows and all highs is detected).

If the parity of one or more of the check groups is incorrect, an error has occurred and the proper error flag or flags will be set high. Any single error in the 16-bit data word will change the sense of exactly three bits of the 6-bit checkword. Any single error in the 6-bit checkword changes the sense of only that one bit. In either case, the single error flag will be set high while the dual error flag will remain low.

ERROR DETECTION & CORRECTION (cont.)

Any two-bit error will change the sense of an even number of check bits. The two-bit error is not correctable since the parity tree can only identify single-bit errors. Both error flags are set high when any two-bit error is detected.

Three or more simultaneous bit errors can fool the EDAC into believing that no error, a correctable error, or an uncorrectable error has occurred and produce erroneous results in all three cases.

Error correction is accomplished by identifying the bad bit and inverting it. Identification of the erroneous bit is achieved by comparing the 16-bit word and 6-bit checkword from memory with the new checkword with one (checkword error) or three (data word error) inverted bits.

As the corrected word is made available on the data word I/O port, the checkword I/O port presents a 6-bit syndrome error code. This syndrome code can be used to identify the corrupted bit in memory (see Table 4. below).

TABLE 3- CHECK WORD GENERATION

CHECKWORD BIT	16-BIT DATA WORD															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CB0	X	X		X	X				X	X	X			X		
CB1	X		X	X		X	X		X			X			X	
CB2		X	X		X	X		X		X			X			X
CB3	X	X	X				X	X			X	X	X			
CB4				X	X	X	X	X						X	X	X
CB5									X	X	X	X	X	X	X	X

The six check bits are parity bits derived from the matrix of data bits as indicated by 'X' for each bit.

TABLE 4- ERROR SYNDROME CODES

SYNDROME ERROE CODE	ERROR LOCATION																					
	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	DB8	DB9	DB10	DB11	DB12	DB13	DB14	DB15	CB0	CB1	CB2	CB3	CB4	CB5	NO ERROR
CB0	L	L	H	L	L	H	H	H	L	L	L	H	H	L	H	H	L	H	H	H	H	H	H
CB1	L	H	L	L	H	L	L	H	L	H	H	L	H	H	L	H	H	L	H	H	H	H	H
CB2	H	L	L	H	L	L	H	L	H	L	H	H	L	H	H	L	H	H	L	H	H	H	H
CB3	L	L	L	H	H	H	L	L	H	H	L	L	L	H	H	H	H	H	H	L	H	H	H
CB4	H	H	H	L	L	L	L	L	H	H	H	H	H	L	L	L	H	H	H	H	L	H	H
CB5	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	H	H	H	H	H	L	H

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APPLICATIONS

Although most semiconductor memories have separate input and output pins, it is possible to design the error detection and correction function using a single EDAC . EDAC data and check bit pins function as inputs or outputs dependent upon the state of control signals S0 and S1. It becomes necessary to use wired AND logic, with fairly complex system timing, to control the EDAC and data bus. This scheme becomes difficult to implement both in terms of board layout and timing. System performance is also adversely affected. See Figure 2.

Optimized systems can be implemented using two EDAC's in parallel. One of the units is used strictly as an encoder during the memory write cycle. Both controls S0 and S1 are grounded. The encoder chip will generate the 6-bit check word for memory storage along with the 16-bit data.

The second of the two EDAC's will be used as a decoder during the memory read cycle.

This decoder chip does require timing pulses for proper operation. Control SI is set low and S0 high as the memory read cycle begins. After the memory output data is valid, the control SI input is moved from the low to a high. This low-to-high transition latches the 22-bit word from memory into internal registers of this second EDAC and enables the two error flags. If no error occurs, the CPU can accept the 16-bit word directly from memory. If a single error has occurred the CPU must move the control SO input from the high to a low to output corrected data and the error syndrome bits. Any dual error should be an interrupt condition.

In most applications, status registers will be used to keep tabs on error flags and error syndrome bits. If repeated patterns of error flags and syndrome bits occur, the CPU will be able to recognize these symptoms as a "hard" error. The syndrome bits can be used to pinpoint the faulty memory chip. See Figure 3.

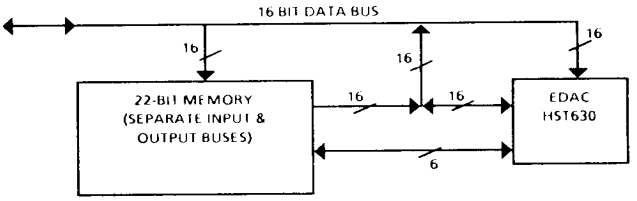
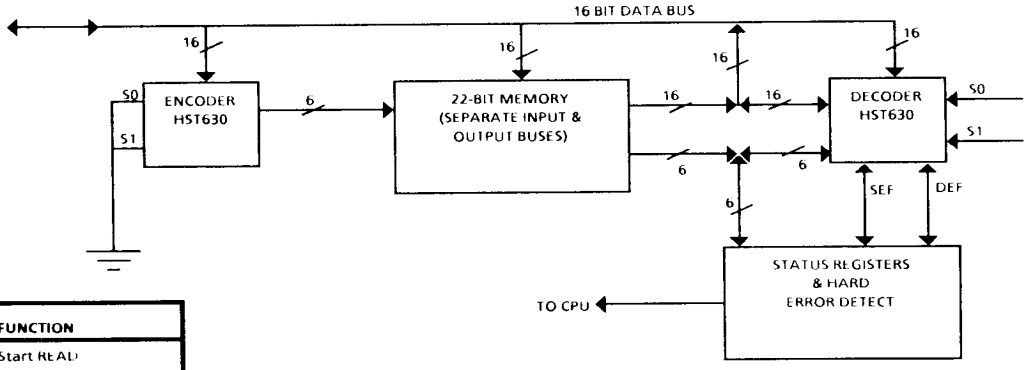


Figure 2 Error Detection and Correction using a single EDAC Unit



S1	S0	FUNCTION
L	H	Start READ
H	H	Latch data & flag errors
H	L	Correct data & output syndrome bits

Figure 3 Error Detection and Correction using two EDAC Units

ABSOLUTE MAXIMUM RATINGS

PARAMETER	MIN	MAX	UNITS
SUPPLY VOLTAGE	-0.5	10	V
INPUT VOLTAGE	V_{SS}-0.3	V_{DD} + 0.3	V
CURRENT THROUGH ANY PIN	-20	20	mA
OPERATING TEMP	-55	125	°C
STORAGE TEMP	-65	150	°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

OPERATING DC ELECTRICAL CHARACTERISTICS

V_{DD} = 5V ± 10%. Over full operating temperature range.

SYMBOL	PARAMETER	TOTAL DOSE RADIATION NOT EXCEEDING $3x10^5$ RAD (Si)			TOTAL DOSE ≤ 1 MRAD (Si)		UNITS	CONDITION
		MIN	TYP	MAX	MIN	MAX		
V_{DD}	SUPPLY VOLTAGE	4.5	5.0	5.5	4.5	5.5	V	
V_{IH1}	TTL Input High Voltage	2.0			2.0		V	
V_{IL1}	TTL Input Low Voltage			0.8		0.3	V	
V_{OH1}	TTL Output High Voltage	2.4			2.4		V	I_{OH} = -1mA
V_{OL1}	TTL Output low Voltage			0.4		0.4	V	I_{OL} = 12mA (CB or DB), I_{OL} = 4mA(SEF or DEF)
I_{IL}	Input Low Ccurrent			± 10		100	uA	V_{DD} = 5.5, V_{IN} = V_{SS}
I_{IH}	Input High Current			± 10		100	uA	V_{DD} = 5.5, V_{IN} = V_{DD}
I_{DD}	Power Supply Current			1		10	mA	V_{DD} = Max, S0 & S1 at 4.5V, All CB & DB pins grounded, DEF & SEF open

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AC ELECTRICAL CHARACTERISTICS

V_{DD} = 5V ± 10%. C_{CL} = 50pF. Over full operating temperature range.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNITS	CONDITIONS
t_{PLH} Propagation delay time, low-to-high-level output (note 3)	DB	CB	-	58	ns	S0 = 0V, S1 = 0V (fig. 4)
t_{PHL} Propagation delay time, high-to-low-level output (note 3)	DB	CB	-	58	ns	S0 = 0V, S1 = 0V (fig. 4)
t_{PLH} Propagation delay time, low-to-high-level output (note 4)	S1 ↑	DEF	-	29	ns	S0 = 3V (fig. 4)
t_{PLH} Propagation delay time, low-to-high-level output (note 4)	S1 ↑	SEF	-	29	ns	S0 = 3V (fig. 4)
t_{PZH} Output enable time to high level (note 5)	S0 ↓	CB, DB	-	40	ns	S1 = 3V (fig. 5)
t_{PZL} Output enable time to low level (note 5)	S0 ↓	CB, DB	-	45	ns	S1 = 3V (fig. 4)
t_{PHZ} Output disable time from high level (note 6)	S0 ↑	CB, DB	-	45	ns	S1 = 3V (fig. 5)
t_{PLZ} Output disable time from low level (note 6)	S0 ↑	CB, DB	-	65	ns	S1 = 3V (fig. 4)
t_S Set-up time to S1 ↑	CB, DB	-	30	-	ns	-
t_h Hold time after S1 ↑	CB, DB	-	15	-	ns	-

1. Input Pulse V_{SS} to 3.0 Volts.
2. Times Measurement Reference Level 1.5 Volts.
3. These parameters describe the time intervals taken to generate the check word during the memory write cycle.
4. These parameters describe the time intervals taken to flag errors during memory read cycle.
5. These parameters describe the time intervals taken to correct and output the data word and to generate and output the syndrome error code during the memory read cycle.
6. These parameters describe the time intervals taken to disable the CB & DB buses in preperation for a new data word during the memory read

Parameter Measurement Information

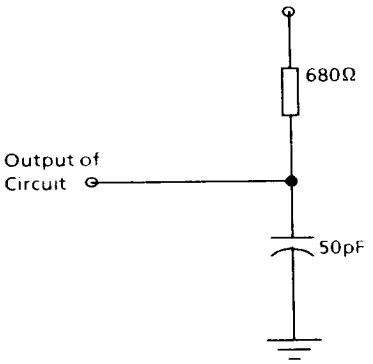

Figure 4. Output Load Circuit

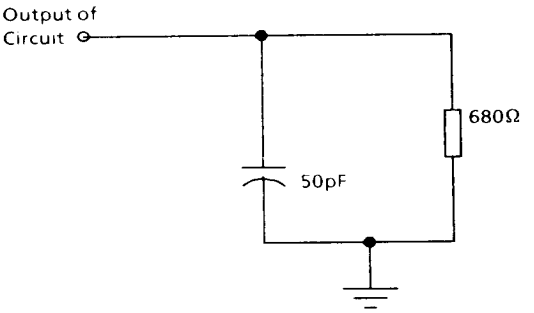

Figure 5. Output Load Circuit

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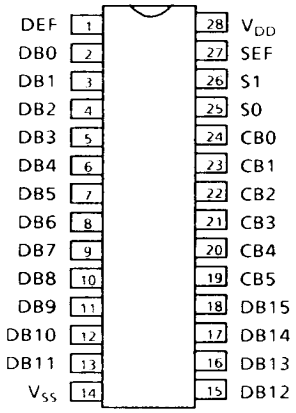
PIN ASSIGNMENTS

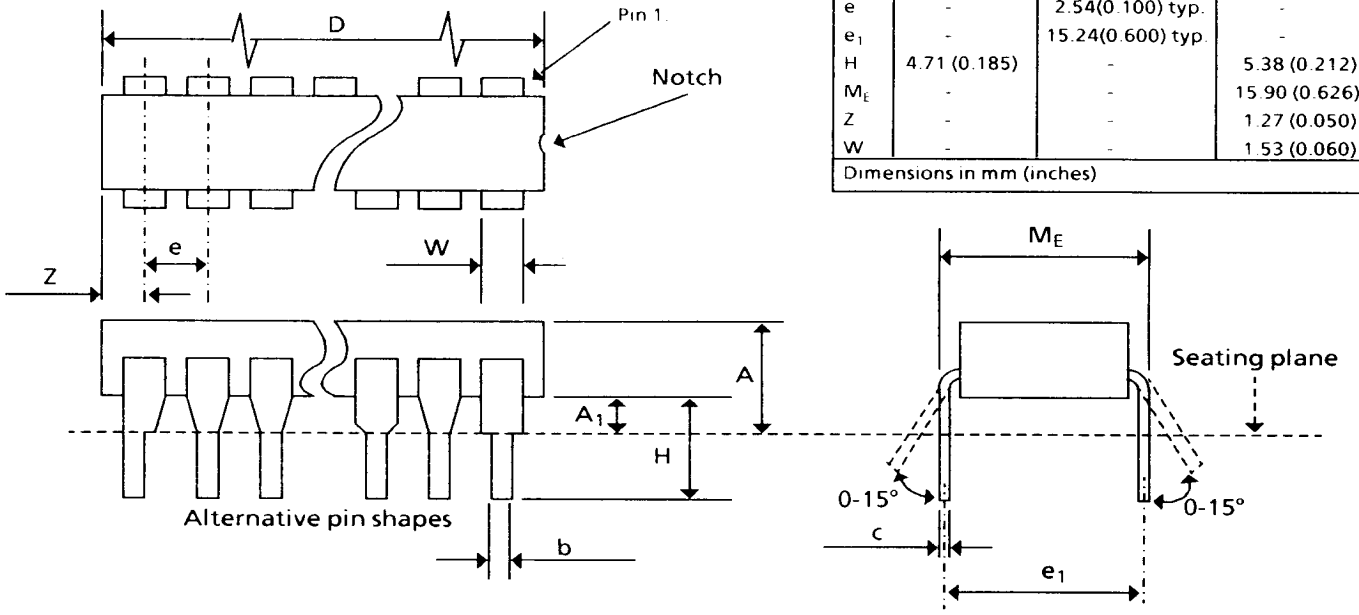
28 Pin Ceramic DIL



PACKAGE OUTLINE

Ref.	Min.	Nom.	Max.
A	-	-	5.60 (0.220)
A_1	0.83 (0.015)	-	1.53 (0.060)
b	0.35 (0.014)	-	0.59 (0.023)
c	0.20 (0.008)	-	0.36 (0.014)
D	-	-	36.02 (1.418)
e	-	2.54(0.100) typ.	-
e_1	-	15.24(0.600) typ.	-
H	4.71 (0.185)	-	5.38 (0.212)
M_E	-	-	15.90 (0.626)
Z	-	-	1.27 (0.050)
W	-	-	1.53 (0.060)

Dimensions in mm (inches)



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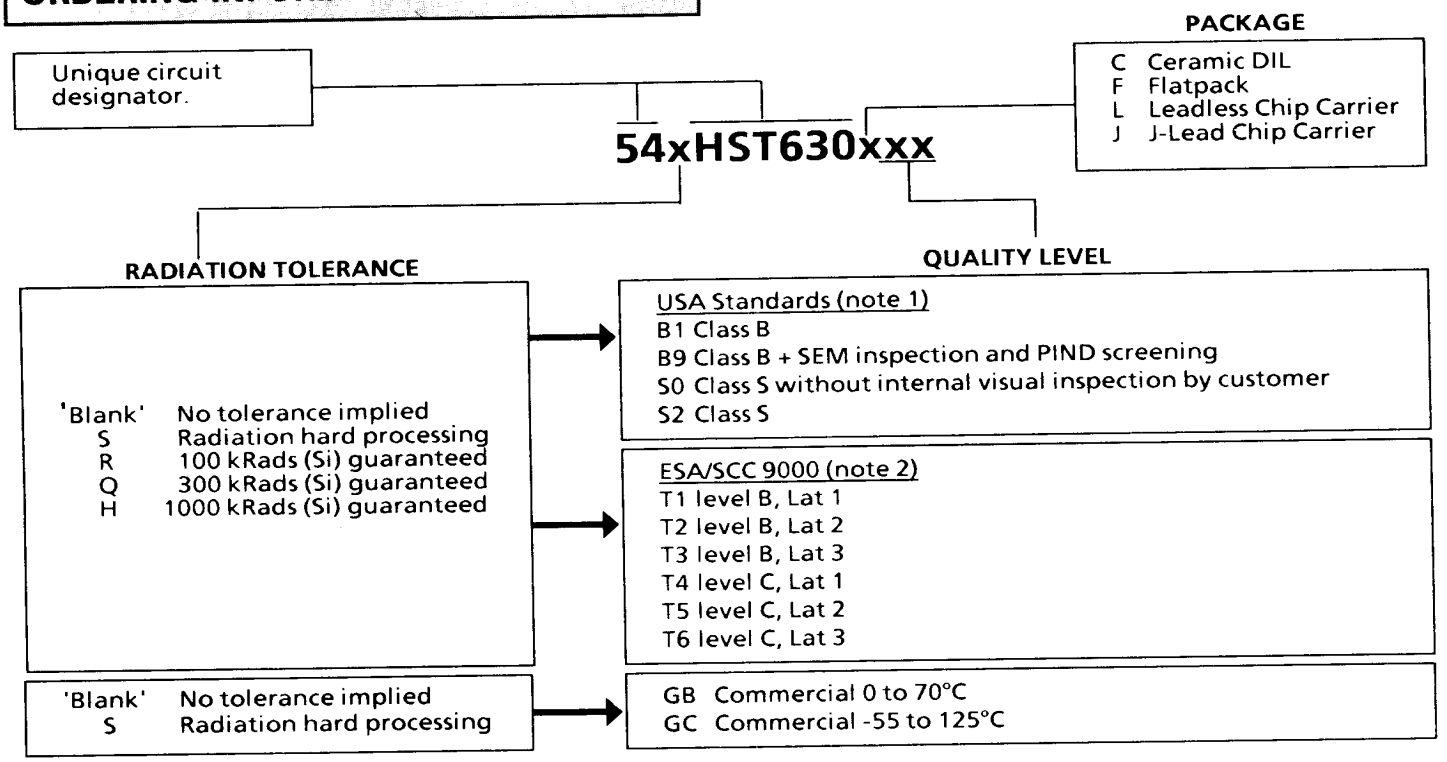
ORDERING INFORMATION



1 Marconi Electronic Devices quality levels conform to MIL STD 883C class B/S, screening method 5004 and Quality Conformance Inspection method 5005 . This does not imply DESC certification, however MIL-M-38510 qualified product listing is being sought.

2 Marconi's specifications for European Space manufacturing flows, including their associated screening procedures, conform to ESA/SCC Generic Specification No.9000. A Process Identification Document, describing the manufacture of these devices, has been approved by the European Space Agency.

TOTAL DOSE RADIATION TESTING

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

Marconi Electronic Devices can provide radiation testing compliant with MIL STD 883C remote sensing method 1019 notice 5.

RADIATION PERFORMANCE

Total Dose (Function to spec)	$3x10^5$ Rad (Si)
Total Dose (Function to 1MRad (Si) spec)	$1x10^6$ Rad (Si)
Transient Upset (stored data loss)	$3x10^{10}$ Rad (Si) /s
Transient Upset (survivability)	$>1x10^{12}$ Rad (Si)/s
Neutron Hardness (Function to spec)	$1x10^{15}$ neutrons/cm^2
Latch-up	Not possible

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