Order this data sheet by H4C/D

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

H4C SERIES

Advance Information

H4C SERIES™ CMOS ARRAYS and the CDA™ ARCHITECTURE

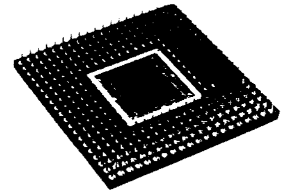
HIGH PERFORMANCE TRIPLE LAYER METAL

SUB–MICRON CMOS ARRAYS

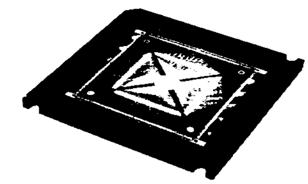
The sub–micron H4C Series™ CMOS gate array family and the new Customer Defined Array™ (CDA) architecture represent the next generation in state–of–the–art ASIC technology. The new fabrication process of the H4C Series enables densities up to 317,968 available gates and supports speed requirements of 60 MHz processors with a power dissipation of 3 μW/gate/MHz.

The CDA architecture offers the versatility and efficiency of system design on a single chip by providing large, fully–diffused architectural blocks like microprocessors, SRAMs, and arithmetic functions. In addition, several design–for–test implementations and clock skew management macros are available to ensure high quality ASIC system designs.

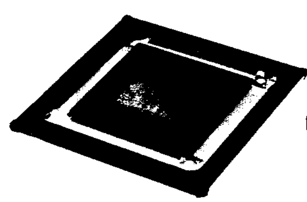
- 27,000 to 318,000 available gates
- Compatible channelless, sea–of–gates and CDA architectures
- 0.7 micron effective gate length
- Triple layer metal signal routing and power distribution
- Up to 70% gate utilization (smaller arrays)
- Eight transistor, fully utilizable, oxide isolated primary cell
- 180 picosecond typical gate delay (2–input NAND)
- User configurable, fully diffused SRAM blocks up to 256K bits
- 3.3 V and 5.0 V CMOS and TTL compatible I/O cells
- Low power consumption, 3 μW/gate/MHz
- Parallelable I/O cells for up to 48 mA drive on a single pin
- Up to 556 power/ground and signal pads
- JTAG (IEEE 1149.1) and LSSD/ESSD scan supported
- High performance packaging
- Extended workstation based CAD support for embedded functions



PGA



TAB



MicroCool QFP

TYPICAL H4C SERIES PACKAGES

TABLE 1 – H4C SERIES ARRAY FEATURES

Array	# of Available Gates	# of Die Pads (Wirebond)	# of Die Pads (TAB)
H4C027	27,048	160	188
H4C035	35,392	176	208
H4C057*	**57,368**	**216**	**256**
H4C086	85,956	256	304
H4C123*	**123,136**	**304**	**360**
H4C161	161,364	344	408
H4C195*	**195,452**	**376**	**444**
H4C318	317,968	468	556

*Now Available – other densities to be available 3Q91

This document contains information on a new product. Specifications and information herein are subject to change without notice.
H4C Series, CDA and Customer Defined Array are trademarks of Motorola Inc.

MOTOROLA

REV 1

PRODUCT DESCRIPTION

The H4C Series CMOS array family meets the challenges of the most demanding applications with advanced sub-micron technology and a high performance Customer Defined Array (CDA) architecture.

SUPERIOR TECHNOLOGY

The H4C Series are 0.7 micron Leff, channelless sea-of-gates arrays with three layers of metal for signal routing and power distribution. Typical gate delays are 180 picoseconds for a 2-input NAND gate.

State-of-the-Art Process

The fabrication of the H4C Series CMOS arrays uses a 0.7 micron channel, self-aligned, twin tub process, Figure 1. Both n-type and p-type well implants are driven together to form deep, balanced wells which improve short n-channel transistor performance. Also, a lightly doped drain (LDD) diffusion is used to reduce hot carrier injection effects in the short channel transistors. A highly reliable multi-layer metal structure is achieved by a planarization technique using tapered contacts and vias.

The combination of a small feature size and a thin oxide coating provides both high gate density and low power dissipation. The typical power dissipation for internal gate is only 3 µW/gate/MHz with a load of 0.06 pF (fanout = 1).

Motorola high quality manufacturing and process experience enables tight control of the H4C process parameters, resulting in the reduced best to worst case condition deviation. Customers benefit from this in optimizing system and chip performance. The H4C process exhibits best to worst case condition deviation of less than 3 times.

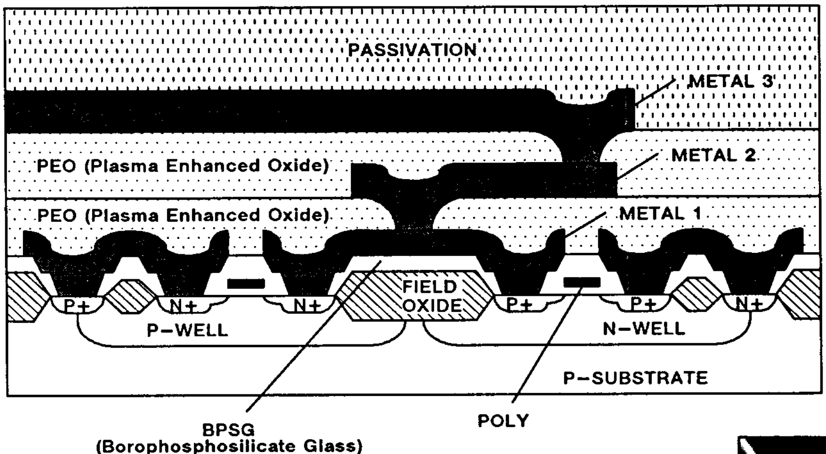


FIGURE 1 — Triple Layer Metal Cross Section

H4C TECHNOLOGY FEATURES

- 0.7 µ Effective Gate Length (Leff)
- Three Layer Minimum Metal Pitch
  - 2.0 µ Metal 1 Pitch
  - 2.8 µ Metal 2 Pitch
  - 2.8 µ Metal 3 Pitch

Triple-Layer Metal Routing

Several years of manufacturing experience in both CMOS and ECL triple-layer metal arrays enables Motorola to produce superior interconnect and power bus routability, and higher gate utilization than two-layer metal structures. High gate utilization is obtainable by the availability of all three metal layers for power and signal routing, see Figure 2.

An early partnership between Motorola and Tangent Systems (now part of Cadence) provided the groundwork for TANGATE™, a placement and routing system, for gate array design. TANGATE (now known as Gate Ensemble™) takes full advantage of Motorola's triple-layer metal routing and has a capacity of at least 250,000 gates. Some of Gate Ensemble's capabilities include timing driven layout (net and path constrained), soft/firm grouping of macros, clock-tree synthesis, incremental layout changes, and highly accurate distributed RC calculations. All these features are available with Motorola's H4C Series gate array based and CDA based designs.

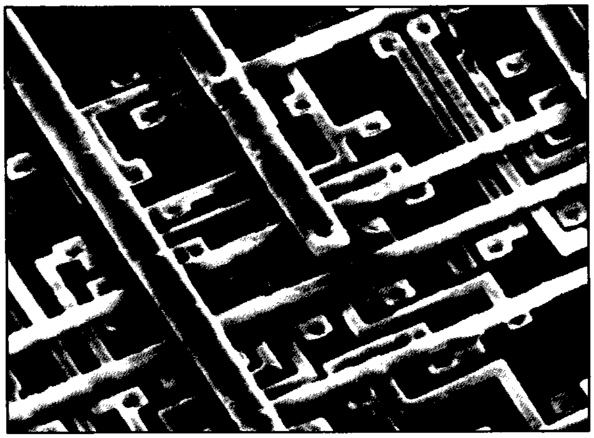


FIGURE 2 — Triple-Layer Metallization (Photo)

Utilization of H4C

Gate utilization varies among ASIC applications and depends on architecture, bus structure, large block usage, target array, etc. Estimated gate utilization for an application can be determined by a feasibility analysis with a Motorola Design Center. Average utilization factors used to match an application to the best array solution are based on design experience developed using the CAD tools.

AN EXTENSIVE LIBRARY

The H4C Series library contains in excess of 280 internal macrocells (over 150 different functions), nearly 800 periphery cell combinations, and a growing list of megafunctions.

Macrocells

Internal macrocells include both combinatorial and sequential functions with complexities ranging from simple logic gates to larger functions such as full adders, decoders and metallized SRAM's. Many of the macrocells include high drive, balanced slew rate, and complementary output versions. The benefit of high drive over standard drive is a greater fanout capacity with less of an impact on propagation delay, see Figure 3. Balanced slew rate versions of macrocells provide symmetrical rise and fall slew rates.

In addition, JTAG (IEEE 1149.1) and ESSD/LSSD scan macrocells are available for designs requiring scan design–for–test methodology.

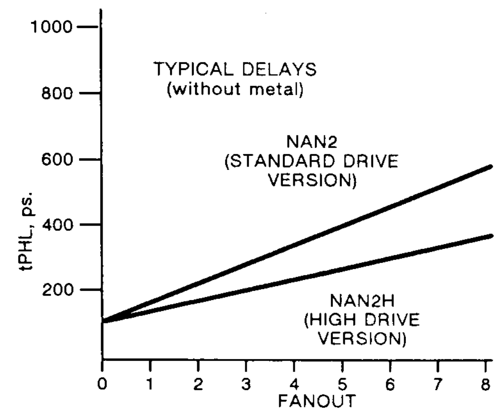


FIGURE 3 – Gate Delay Comparison of High Drive vs. Standard Drive Macrocells

Megafunctions

Megafunctions include embedded and metallized large functions such as SRAMs, microprocessors and arithmetic functions. Embedded functions are fully–diffused functional blocks that are integrated within a host gate array. Embedded functions allow greater density, higher performance and reduced layout complexity than gate array implementations.

Embedded SRAMs up to 256K–bits are user definable using Motorola's Memorist™, SRAM Compiler, available with the Open Architecture CAD System (OACS™). Several hundred thousand different physical SRAM configurations are possible with Memorist. Embedded SRAMs are available in single and dual port configurations.

Additional megafunctions under development include a CPU and commonly used arithmetic and peripheral functions.

GATE ARRAY VS. CDA ARCHITECTURE

The H4C Series can be implemented in either a conventional gate array or a Customer Defined Array (CDA). The CDA was developed to satisfy the most demanding requirements for high performance applications.

The CDA is an architectural hybrid, taking the best of both gate array and standard cell methodologies, see Figure 4. As in standard cell implementations optimized, embedded blocks or megafunctions are used in a CDA to provide performance unattainable in a gate array. Also, the CDA exploits the ease and low cost of manufacturing a gate array by using a fixed I/O ring and die size.

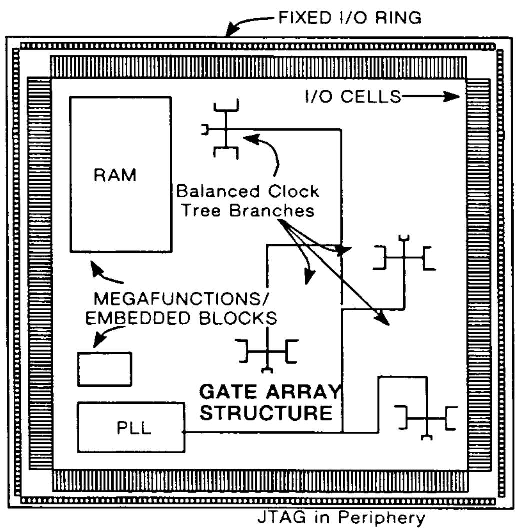


FIGURE 4 – The CDA Concept: Megafunctions and Embedded Blocks Within a Gate Array

The result is an architecture which has a high level of functionality and performance with fast, cost–efficient manufacturing.

In addition to CMOS, the CDA concept supports further expansion using BiCMOS and bipolar technologies.

LEADING EDGE PACKAGING

A variety of high performance, high pin count packages are offered including Tape Automated Bonding (TAB), Quad Flat Package (QFP), Molded Carrier Ring QFP (MCR–QFP), and Pin Grid Arrays (PGA). Pin counts range from 128 to over 500.

CLOCK SKEW MANAGEMENT

ASICs (Application Specific Integrated Circuits) are becoming an integral part of system design and are regularly found interfacing with multiple chips including other ASICs, microprocessors and SRAMs. Optimizing performance of such systems rests on maximizing communication between chips using synchronous interfaces. Clock skew control and distribution (both on–chip and between chips) is of critical importance.

Motorola's tighter control of process variation is key to consistency and predictability in silicon performance. Also, Motorola has developed special macros and methodologies to manage clock skew. For example, balanced clock trees can optionally be implemented within an ASIC to provide on–chip clock skew control while on–chip PLLs (phase locked loop) manage inter–chip clock skew, Figure 5.

Clock Tree Synthesis

Clock tree synthesis can be performed during layout to build balanced clock tree networks with minimal effect on design routability. Also, the clock trees do not interfere with critical data paths, timing driven layout or floorplanning. This method of clock distribution allows embedded block design and layout critical to the CDA architecture while minimizing both clock skew across chip and clock insertion delay.

Phase Locked Loop

A unique, fully digital PLL is available to control inter–chip clock skew. The PLL megafunction compensates for insertion delay and process variation by synchronizing internal storage elements with the external system clock. Several specially designed macrocells make up the PLL for flexibility in placement.

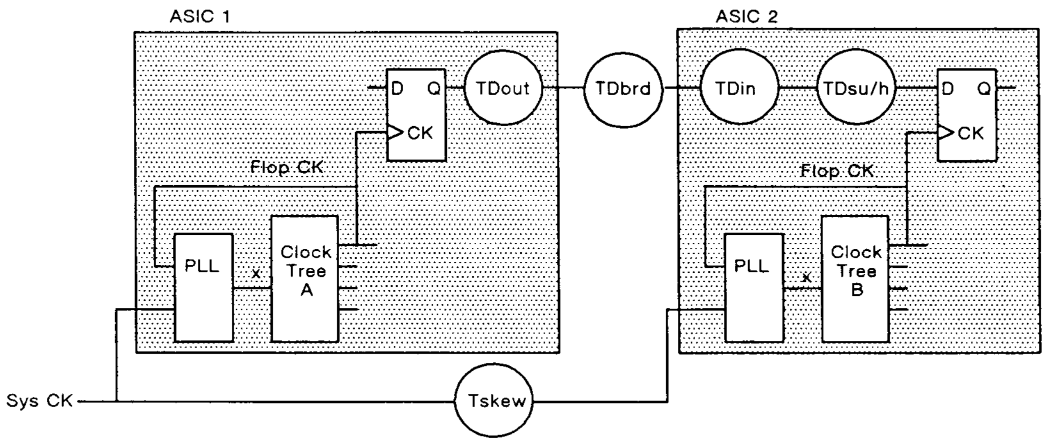


FIGURE 5 — An Example of Clock Skew Management Between Two ASIC Chips

DESIGN FOR TESTABILITY

The time and cost to test an ASIC increases exponentially as the complexity and size of the ASIC grows. Using a design for testability (DFT) methodology allows large, complex ASICs to be efficiently and economically tested.

Motorola supports several DFT methodologies, including JTAG boundary scan and edge and level sensitive design (ESSD/LSSD) scan, by providing the necessary macrocells. Also, Motorola is involved with developing a low cost, high speed scan tester.

ESSD/LSSD Scan Macrocells

The H4C library provides all existing D and JK Flip–Flop macros in scan versions together with special Level–Sensitive and Scan Design (ESSD/LSSD) macros. A licensed Scan Macro is available which eliminates the additional propagation delay usually associated with the implementation of scan circuitry.

JTAG Boundary Scan Macrocells

Motorola provides special design H4C I/O and internal macrocells to provide full IEEE 1149.1 compliant JTAG boundary scan. The JTAG I/O macrocells are implemented in the periphery region of the array to minimize performance impact and silicon overhead. JTAG signal distribution is accomplished by the abutment of common I/O ports on JTAG macrocells and connection to JTAG specific routing tracks in the I/O ring. Internal macrocells are used to implement the TAP controller function and the bypass, ID code and instruction registers with compatibility to Motorola's Mustang ATPG tool and checked during ERC for correct implementation.

The ISS2000™

In 1988 Motorola entered into partnership with Schlumberger Technologies, ATE Division, to develop the ISS2000 (code name: Typhoon) – a high pin count, scan–based, cost–efficient tester for ASICs. The ISS2000 features up to 1024 signal pins with 64 scan channels that supports scan data rates up to 40MHz. The hardware also supports a high speed clock burst pin to enable BIST (Built in Self Test) logic for use with SRAM and other large functions.

HIGHLY VERSATILE I/O RING

Programmable Power and Ground Pins

The H4C arrays each have 4 separate power buses. Each I/O cell site features a universal buffer (see Figure 6) which is fully programmable as a power or ground pin or one of 779 periphery cell combinations giving the designer full flexibility in pinout. All H4C arrays have a set of fixed power and ground pads. For non-standard power and ground implementations please consult the factory.

The number of VDD and VSS pins required is calculated from a set of rules based on the number of internal gates and outputs that are switching simultaneously. This simultaneous switching consideration can be cumulative when using the BOTHVSS and BOTHVDD commands which link the Internal and Output power and ground buses together. A pair of power and ground pins is required for every 2000 internal gates that are switching simultaneously. In addition, for every 10–8mA outputs at least one VDD pin is required, and for every 12–8mA outputs at least one VSS pin is required (assuming simultaneously switching outputs driving 50 pF loads).

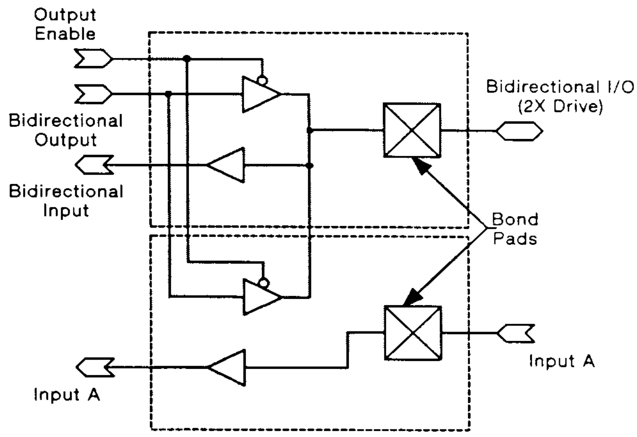


FIGURE 7 – Example of Bidirectional I/O (2X Drive)

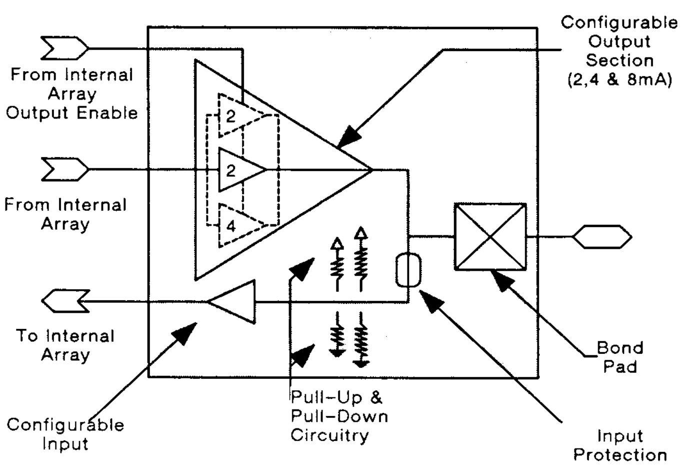


FIGURE 6 – Universal Buffer Structure

Selectable Output Drive

All I/O macrocells are programmable for minimum drive currents of 2, 4 or 8 mA (actual currents are significantly higher, see D.C. Electrical Specification on page 19). Non-JTAG I/O output macrocells can be paralleled internally to deliver up to 48 mA of output current (source or sink) through a single pin. JTAG I/O macrocells are available in drive versions up to 48 mA. In Figure 7 two buffers have been paralleled. If not needed as output buffers, cells can also be used as buffers to drive a high fanout load of internal cells.

Slew Rate Control I/O

The H4C Series designer has the option of configuring outputs with slew rate control to slow down the output falling-edge rates of signals going off-chip. This feature helps decrease system noise over and undershoot of output signals caused by fast rise and fall times of H4C output buffers.

Two slew rates (S2 and S4) are provided for all 4 and 8 mA output buffer types. The choice of slew rates depends upon circuit design requirements. The S4 option has the higher slew rate and the S2 option has a moderate slew rate.

H4C Oscillators

Three different oscillator I/O macros are available on the H4C Series arrays: non-inverting buffer, clock buffer, and schmitt trigger versions. These macros can be configured for ceramic resonators from 32 KHz to above 60 MHz with quartz crystals.

REDUCED POWER DISSIPATION

In designing the H4C Series, as with the HDC Series, Motorola has continued optimizing both gate density and power dissipation. In the HDC Series process the internal gates contribute 6μW/gate/MHz where as in the H4C process the internal gates contribute 3μW/gate/MHz.

The power consumption of the arrays will vary due to circuit and array conditions. Figure 8 is a comparison of the typical curves depicting power consumption of both H4C and HDC arrays. The following assumptions were made in deriving this graph: 25% of usable gates in the array are switching simultaneously at 30 MHz and 25% of available I/O pads are connected as 8 mA drivers, driving 50 pF loads at 30 MHz.

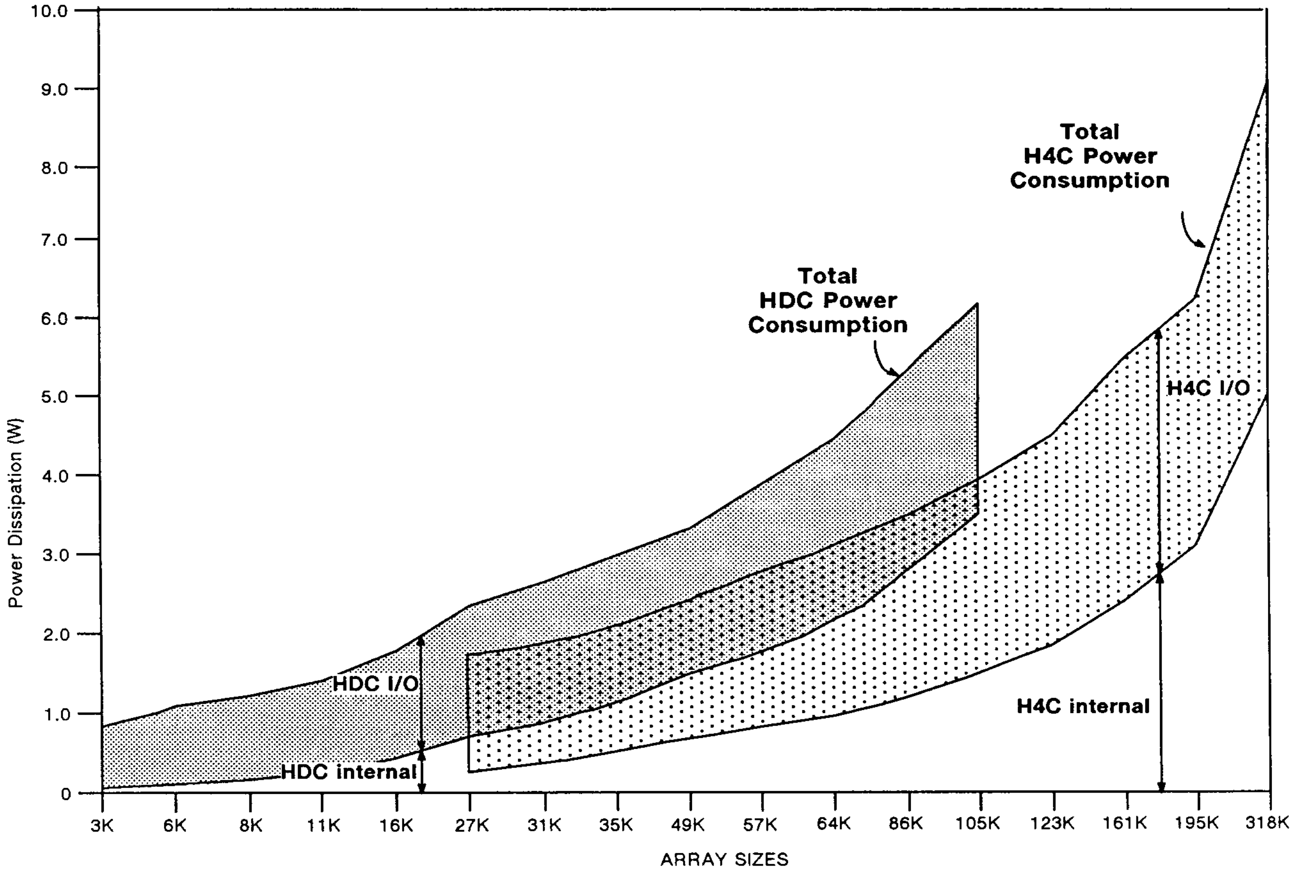


FIGURE 8 – Power Consumption of H4C VS. HDC Arrays

THE MACROCELL LIBRARY

The following tables detail the elements which make up the H4C Series library. The elements are organized into four categories: Input/Output Macrocells, JTAG Macrocells, Internal Macrocells, and Clock Skew Management Macrocells. Internal Macrocells are provided with their equivalent gate count.

INPUT/OUTPUT MACROCELLS

INPUTS

NAME	SWITCHING LEVELS	RELATIVE POLARITY	CLOCK DRIVER
ICI	CMOS	Inverting	–
ICIH	CMOS	Inverting	YES
ICN	CMOS	Non-inverting	–
ICNH	CMOS	Non-inverting	YES
ISN	CMOS Schmitt	Non-inverting	–
ISNH	CMOS Schmitt	Non-inverting	YES
ITN	TTL	Non-inverting	–
ITNH	TTL	Non-inverting	YES
ITSN	TTL Schmitt	Non-inverting	–
ITSNH	TTL Schmitt	Non-inverting	YES

OUTPUTS

NAME	TYPE	CURRENT DRIVE (mA)	PARALLEL UP TO 4X
ON2	Standard	2	–
ON4	Standard	4	–
ON8	Standard	8	YES
ON2T	3-State	2	–
ON4T	3-State	4	–
ON8T	3-State	8	YES
ON2OD	Open-Drain	2(Sink)	–
ON4OD	Open-Drain	4(Sink)	–
ON8OD	Open-Drain	8(Sink)	YES
ON4S2	Slew	4	–
ON8S2	Slew	8	YES
ON4S4	Slew	4	–
ON8S4	Slew	8	YES
ON4TS2	3-State/Slew	4	–
ON8TS2	3-State/Slew	8	YES
ON4TS4	3-State/Slew	4	–
ON8TS4	3-State/Slew	8	YES
ON4ODS2	Open-Drain/Slew	4(Sink)	–
ON8ODS2	Open-Drain/Slew	8(Sink)	YES
ON4ODS4	Open-Drain/Slew	4(Sink)	–
ON8ODS4	Open-Drain/Slew	8(Sink)	YES

Clock drivers ("H" suffixed inputs) and standard outputs are not used as bidirectionals.

BIDIRECTIONALS

OUTPUT CHOICES	INPUT CHOICES				
	BICI	BICN	BITN	BISN	BITSN
BON2T	Y	Y	Y	Y	Y
BON4T	Y	Y	Y	Y	Y
BON8T	Y	Y	Y	Y	Y
BON2OD	Y	Y	Y	Y	Y
BON4OD	Y	Y	Y	Y	Y
BON8OD	Y	Y	Y	Y	Y
BON4TS2	Y	Y	Y	Y	Y
BON8TS2	Y	Y	Y	Y	Y
BON4TS4	Y	Y	Y	Y	Y
BON8TS4	Y	Y	Y	Y	Y
BON4ODS2	Y	Y	Y	Y	Y
BON8ODS2	Y	Y	Y	Y	Y
BON4ODS4	Y	Y	Y	Y	Y
BON8ODS4	Y	Y	Y	Y	Y

INPUT/OUTPUT MACROCELLS

PULL RESISTOR TYPES

PDL	Pull-Down, Low current/speed
PDH	Pull-Down, High current/speed
PUL	Pull-Up, Low current/speed
PUH	Pull-Up, High current/speed

Any of the above pull resistors can be used with any of the inputs and/or outputs.

OSCILLATOR TYPES

OSCPB	Standard Oscillator
OSCPHB	Oscillator with Clock Driver Buffer
OSCPSB	Oscillator with Schmitt Trigger Buffer

JTAG 1149.1 INPUT/OUTPUT MACROCELLS

JTAG 1149.1 INPUTS*

NAME	SWITCHING LEVELS	RELATIVE POLARITY	CLOCK DRIVER
ICNCKHJ	CMOS	Non-inverting	YES
ICNJ	CMOS	Non-inverting	–
ICNJA	CMOS	Non-inverting	–
ISNCKHJ	CMOS Schmitt	Non-inverting	YES
ISNJ	CMOS Schmitt	Non-inverting	–
ITNCKHJ	TTL	Non-inverting	YES
ITNJ	TTL	Non-inverting	–
ITSNCKHJ	TTL Schmitt	Non-inverting	YES
ITSNJ	TTL Schmitt	Non-inverting	–

JTAG 1149.1 OUTPUTS*

NAME	TYPE	CURRENT DRIVE (mA)
ON2J	Standard	2
ON4J	Standard	4
ON8J**	Standard	8
ON2TJ	3-State	2
ON4TJ	3-State	4
ON8TJ**	3-State	8
ON2ODJ	Open-Drain	2(Sink)
ON4ODJ	Open-Drain	4(Sink)
ON8ODJ**	Open-Drain	8(Sink)
ON4S2J	Slew	4
ON8S2J	Slew	8
ON4S4J	Slew	4
ON8S4J**	Slew	8
ON4TS2J	3-State/Slew	4
ON8TS2J**	3-State/Slew	8
ON4TS4J	3-State/Slew	4
ON8TS4J**	3-State/Slew	8
ON4ODS2J	Open-Drain/Slew	4(Sink)
ON8ODS2J**	Open-Drain/Slew	8(Sink)
ON4ODS4J	Open-Drain/Slew	4(Sink)
ON8ODS4J**	Open-Drain/Slew	8(Sink)

* Available in Phase 2.
**Versions up to 4X

JTAG 1149.1 INPUT/OUTPUT MACROCELLS

JTAG 1149.1 BIDIRECTIONALS*

OUTPUT CHOICES	INPUT CHOICES			
	BICNJ	BITNJ	BISNJ	BITSNJ
BN2TJ	Y	Y	Y	Y
BN4TJ	Y	Y	Y	Y
BN8TJ**	Y	Y	Y	Y
BN2ODJ	Y	Y	Y	Y
BN4ODJ	Y	Y	Y	Y
BN8ODJ**	Y	Y	Y	Y
BN4TS2J	Y	Y	Y	Y
BN8TS2J**	Y	Y	Y	Y
BN4TS4J	Y	Y	Y	Y
BN8TS4J**	Y	Y	Y	Y
BN4ODS2J	Y	Y	Y	Y
BN8ODS2J**	Y	Y	Y	Y
BN4ODS4J	Y	Y	Y	Y
BN8ODS4J**	Y	Y	Y	Y

** Versions up to 4X

TAP INPUT/OUTPUT MACROCELLS — I/O**

TAP INPUTS/OUTPUTS*

TCK	Test Clock	1/0
TCKH	Test Clock, High Drive	1/1
TCKT	Test Clock, TTL Levels	1/0
TCKHT	Test Clock, TTL Levels, High Drive	1/1
TDI	Test Data Input	1/0
TDIT	Test Data Input, TTL Levels	1/0
TDO	Test Data Output	1/1
TDOA	Test Data Output	1/1
TMS	Test Mode Select	1/0
TMST	Test Mode Select, TTL Levels	1/0
TRSTB	Test Reset (Bar)	1/0
TRSTBT	Test Reset (Bar), TTL Levels	1/0

MISCELLANEOUS BOUNDARY–SCAN MACROCELLS*

CKDR, CKDRP	B-S Register Clock Driver – JTAG (Pwr/Gnd Site)	0/1
CKDRMID, CKDRMIDP	B-S Register Clock Driver – JTAG (Pwr/Gnd Site)	0/1
CKDRCC1, CKDRCC1P	B-S Register Clock Driver – JTAG (Pwr/Gnd Site)	0/1
CKDRCC2, CKDRCC2P	B-S Register Clock Driver – JTAG (Pwr/Gnd Site)	0/1
ENSCANJ, ENSCANP	B-S Register Enable Scan Macro – JTAG (Pwr/Gnd Site)	0/1
IMCDR, IMCDRP	B-S Register Input Mode Control Driver – JTAG (Pwr/Gnd Site)	0/1
OMCDR, OMCDRP	B-S Register Output Mode Control Driver – JTAG (Pwr/Gnd Site)	0/1
OSCPBJ, OSCPHBJ, OSCPSBJ	B-S Register Oscillator w/Non-Inverting Input/Osc. w/Clock Buffer Input/ Osc. w/Schmitt Trigger Input – JTAG	2/2
SHDR, SHDRP	B-S Register Shift Driver – JTAG (Pwr/Gnd Site)	0/1
UDDR, UDDRP	B-S Register Update Driver – JTAG (Pwr/Gnd Site)	0/1

** Number of input/output drivers used for function.

JTAG 1149.1 INTERNAL MACROCELLS — GATES

TAP CONTROL MACRO FUNCTIONS*

BPREG	1-bit Bypass Register	~10
ENSCANI	Enable Boundary Scan Macro (Internal)	~19
IDREG	32-bit Device Identification Code Register	~360
MC_IREG	1-bit of Instruction Register (Soft Macro)	~32
MC_IREG4	4-bit of Instruction Register (Soft Macro)	~128
MC_TAPC	Tap Controller (Soft Macro)	~263

INTERNAL MACROCELLS — GATES

INVERTING BUFFERS

INV	Inverter	1
INVB	Inverter, Balanced (Symetrical Rise & Fall)	1
INV2	2–Inverters in parallel	1
INV2B	2–Inverters in parallel, Balanced (Symetrical Rise & Fall)	2
INV3	3–Inverters in parallel	2
INV3B	3–Inverters in parallel, Balanced (Symetrical Rise & Fall)	3
INV4	4–Inverters in parallel	2
INV4B	4–Inverters in parallel, Balanced (Symetrical Rise & Fall)	4
INV8	8–Inverters in parallel	4
INV8B	8–Inverters in parallel , Balanced (Symetrical Rise & Fall)	8
INVX	Inverted Output buffer used to drive internal logic	--
INVXP	Inverted Output buffer used to drive internal logic (Pwr/Gnd Site)	--

NON–INVERTING BUFFERS

BUF	1x drive buffer	1
BUF2	2x drive buffer	2
BUF2B	2x drive buffer, Balanced (Symetrical Rise & Fall)	3
BUF2C	2x drive buffer,1x Complementary Output	2
BUF3	3x drive buffer	2
BUF3B	3x drive buffer, Balanced (Symetrical Rise & Fall)	4
BUF3C	3x drive buffer,1x Complementary Output	2
BUF4	4x drive buffer	3
BUF4B	4x drive buffer, Balanced (Symetrical Rise & Fall)	5
BUF8	8x drive buffer	5
BUF8B	8x drive buffer, Balanced (Symetrical Rise & Fall)	9
BUFX	Output buffer used to drive internal logic	--
BUFXP	Output buffer used to drive internal logic (Pwr/Gnd Site)	--

SCHMITT TRIGGER BUFFERS

DS1536	Schmitt Trigger Buffer	3
DS1536H	Schmitt Trigger Buffer, 2x Drive	3
DS1536I	Inverting Schmitt Trigger Buffer	3
DS1536IH	Inverting Schmitt Trigger Buffer, 2x Drive	4

* Available in Phase 2.

INTERNAL MACROCELLS		GATES
3–STATE BUFFERS		
TBUFP	3–state Buffer, Active High Enable	4
TBUFPH	3–state Buffer, Active High Enable,2x Drive	5
TBUF	3–state Buffer, Active Low Enable	4
TBUFH	3–state Buffer, Active Low Enable, 2x Drive	5
TDBUF	3–state Buffer, Active Low Enable	4
TDBUFH	3–state Buffer, Active Low Enable, 2x Drive	5
INVTP	Inverting 3–state Buffer,Active High Enable	3
INVTPH	Inverting 3–state Buffer, Active High Enable, 2x Drive	4
INVT	Inverting 3–state Buffer, Active Low Enable	2
INVTH	Inverting 3–state Buffer, Active Low Enable, 2x Drive	3
AND GATES		
AND2	2–Input And Gate	2
AND2H	2–Input And Gate, 2x Drive	2
AND3	3–Input And Gate	2
AND3H	3–Input And Gate, 2x Drive	3
AND4	4–Input And Gate	3
AND4H	4–Input And Gate, 2x Drive	3
AND8H	8–Input And Gate, 2x Drive	6
NAND GATES		
NAN2	2–Input Nand Gate	1
NAN2H	2–Input Nand Gate 2x Drive	2
NAN2B	2–Input Nand Gate, Balanced	2
NAN3	3–Input Nand Gate	2
NAN3H	3–Input Nand Gate, 2x Drive	3
NAN4	4–Input Nand Gate	2
NAN4H	4–Input Nand Gate, 2x Drive	4
NAN5	5–Input Nand Gate	4
NAN5H	5–Input Nand Gate, 2x Drive	5
NAN6CH	6–Input Nand Gate, 2x Drive, 1x Complementary Output	6
NAN8CH	8–Input Nand Gate, 2x Drive, 1x Complementary Output	7
NAN8H	8–Input Nand Gate, 2x Drive	7
OR GATES		
OR2	2–Input Or Gate	2
OR2H	2–Input Or Gate, 2x Drive	2
OR3	3–Input Or Gate	2
OR3H	3–Input Or Gate, 2x Drive	3
OR4	4–Input Or Gate	3
OR4H	4–Input Or Gate, 2x Drive	3
OR8H	8–Input Or Gate, 2x Drive	8

INTERNAL MACROCELLS		GATES
NOR GATES		
NOR2	2–Input Nor Gate	1
NOR2H	2–Input Nor Gate, 2x Drive	2
NOR2B	2–Input Nor Gate, Balanced	2
NOR3	3–Input Nor Gate	2
NOR3H	3–Input Nor Gate, 2x Drive	4
NOR4	4–Input Nor Gate	4
NOR4H	4–Input Nor Gate, 2x Drive	4
NOR5	5–Input Nor Gate	4
NOR5H	5–Input Nor Gate, 2x Drive	5
NOR6CH	6–Input Nor Gate, 2x Drive, 1x Complementary Output	6
NOR8H	8–Input Nor Gate, 2x Drive,	7
NOR8CH	8–Input Nor Gate, 2x Drive, 1x Complementary Output	7
EXCLUSIVE OR/EXCLUSIVE NOR GATES		
EXOR	2–Input Exclusive Or	4
EXORH	2–Input Exclusive Or, 2x Drive	4
EXORA	2–Input Exclusive Or, Unbuffered Inputs	3
EXOR3	3–Input Exclusive Or	7
EXOR3H	3–Input Exclusive Or, 2x Drive	7
EXOR4	4–Input Exclusive Or	9
EXOR4H	4–Input Exclusive Or, 2x Drive	10
EXOR9H	9–Input Exclusive Or	24
EXNOR	2–Input Exclusive Nor	4
EXNORA	2–Input Exclusive Nor, Unbuffered Inputs	3
EXNORH	2–Input Exclusive Nor, 2x Drive	4
EXNOR3	3–Input Exclusive Nor	7
EXNOR3H	3–Input Exclusive Nor, 2x Drive	8
AND/NOR, AND/OR, OR/NAND, & OR/AND GATES		
AO21H	2–Input And, 1–wide, Into 2–Input Or, 2x Drive	3
AO22H	2–input And, 2–wide, Into 2–Input Or, 2x Drive	3
AO321H	3,2,1–input And–Or Gate, 2x Drive	5
AO4321H	4,3,2,1–input And–Or Gate, 2x Drive	8
AOI21	2–Input And, 1–wide, Into 2–Input Nor	2
AOI21H	2–Input And, 1–wide, Into 2–Input Nor, 2x Drive	3
AOI211	2–input And, 1–wide, Into 3–Input Nor	2
AOI211H	2–input And, 1–wide, Into 3–Input Nor, 2x Drive	4
AOI22	2–input And, 2–wide, Into 2–Input Nor	2
AOI22H	2–input And, 2–wide, Into 2–Input Nor, 2x Drive	4
ANDOI22	2–Input And + 2–Input Nor, Into 2–Input Nor	3

INTERNAL MACROCELLS		GATES

AND/NOR, AND/OR, OR/NAND, & OR/AND GATES (continued)

ANDOI22H	2-Input And + 2-Input Nor, Into 2-Input Nor, 2x Drive	4
MAJ3	2 of 3 Majority, Inverting Output	3
MAJ3H	2 of 3 Majority, Inverting Output, 2x Drive	4
NR24	2-Input, 4-wide, Nor, Partial Product Generator	4
OA21H	2-Input Or, 1-wide, Into 2-Input And, 2x Drive	3
OA22H	2-Input Or, 2-wide, Into 2-Input And, 2x Drive	3
OA211H	2-Input Or, 1-wide, Into 3-Input And, 2x Drive	3
OAI21	2-Input Or, 1-wide, Into 2-Input Nand	2
OAI21H	2-Input Or, 1-wide, Into 2-Input Nand, 2x Drive	3
OAI211	2-Input Or, 1-wide, Into 3-Input Nand	2
OAI211H	2-Input Or, 1-wide, Into 3-Input Nand, 2x Drive	4
OAI22	2-Input Or, 2-wide, Into 2-Input Nand	2
OAI22H	2-Input Or, 2-wide, Into 2-Input Nand, 2x Drive	4
ONDAI22	2-Input Or + 2-Input Nand, Into 2-Input Nand	3
ONDAI22H	2-Input Or + 2-Input Nand, Into 2-Input Nand, 2x Drive	4

D TYPE FLIP-FLOPS

DFF1	Scan D Flip-Flop	12
DFF4	4-Bit Scan D Flip-Flop	38
DFF8	8-Bit D-Flip-Flop wth Scan	80
DFFMX1	Scan D Flip-Flop with Mux Input	15
DFFMX4	4-Bit Scan D Flip-Flop with Mux Input	47
DFFP	D Flip-Flop	8
DFFPH	DFFP with 2x Drive	8
DFFLP	D Flip-Flop, Multiplexed (or Scan) Input	11
DFFLPH	DFFLP with 2x Drive	11
DFFRP	D Flip-Flop with Reset	8
DFFRPH	DFFRP with 2x Drive	10
DFFRLP	D Flip-Flop with Reset, Multiplexed (or Scan) Input	11
DFFLPA	D Flip-Flop, DFFLP with Unbuffered Input/Clock	8
DFFLPAH	DFFLPA with 2x Drive	9
DFFLPB	D Flip-Flop	10
DFFLPBH	DFFLPB with 2x Drive	11
DFFRLPH	DFFRLP with 2x Drive	11
DFFRSPB	D Flip-Flop with Set and Reset	10

INTERNAL MACROCELLS		GATES

D TYPE FLIP-FLOPS (continued)

DFFRSPHB	DFFRSP with 2x Drive	10
DFFRSLPB	D Flip-Flop with Set and Reset, Multiplexed (or Scan) Input	14
DRSLPHB	DFFRSLPB with 2x Drive	14
DFFSP	D Flip-Flop with Set	8
DFFSPH	DFFSP with 2x Drive	10
DFFSLP	D Flip-Flop with Set, Multiplexed (or Scan) Input	12
DFFSLPH	DFFSLP with 2x Drive	12
DFFRTPA	D Flip-Flop with Reset, Q and 3-state Q Outputs	10
DFFRTPHA	DFFRTPA with 2x Drive	12
DFFP4	4-Bit DFFP	23
DFFP4H	DFFP4 with 2x Drive	24
DFFR1*	D Flip-Flop with Reset and Scan	13
DFFR1H*	DFFR1 with 2x Drive	13
DFFR4*	4-Bit D Flip-Flop with Scan	41
DFFR4H*	DFFR4 with 2x Drive	41
DFFRP4	4-Bit DFFRP	28
DFFRP4H	DFFRP4 with 2x Drive	32
DFFSC	Scan D Flip-Flop	16
DFFSCH	DFFSC with 2x Drive	18
DFFSCA	Muxed DFFSC	18
DFFSCAH	DFFSCA with 2x Drive	20

JK TYPE FLIP-FLOPS

JKFFP	J-K Flip-Flop	10
JKFFPH	JKFFP with 2x Drive	10
JKFFLP	J-K Flip Flop, Multiplexed (or Scan) Input	14
JKFFLPH	JKFFLP with 2x Drive	14
JKFFRP	J-K Flip Flop with Reset	12
JKFFRPH	JKFFRP with 2x Drive	12
JKFFRLP	J-K Flip Flop with Reset, Multiplexed (or Scan) Input	14
JKFFRLPH	JKFFRLPH with 2x Drive	14
JKFFRSPB	J-K Flip Flop with Set and Reset	12
JKRSPHB	JKFFRSPB with 2x Drive	13
JKRSLPB	J-K Flip Flop with Set and Reset, Multiplexed (or Scan) Input	16
JKRSLPHB	JKFFRSLPB with 2x Drive	16

TOGGLE FLIP-FLOPS

TFFRPA	Toggle Flip-Flop with Reset	8
TFFRPHA	TFFRPA with 2x Drive	10
TFFSP	Toggle Flip-Flop with Set	8
TFFSPH	TFFSP with 2x Drive	10

* Available in Phase 2.

INTERNAL MACROCELLS		GATES

LATCHES

LATN	D-Type Latch, Neg Gate Latched	5
LATNH	LATN with 2x Drive	6
LATP	D-Type Latch, Pos Gate Latched	5
LATPH	LATP with 2x Drive	6
LATRN	D-Type Latch with Reset, Neg Gate Latched	6
LATRNH	LATRN with 2x Drive	7
LATRP	D-Type Latch with Reset, Pos Gate Latched	6
LATRPH	LATRP with 2x Drive	7
LAT4T	4-Bit D Latch with 3-State Output	19
LAT4TH	LAT4T with 2x Drive	23
LATP4	4-Bit Latch with Non-Inverting Output	14
LATP4H	LATP4 with 2x Drive	14
LATPA	Non-Inverting Latch, Pos Gate Latched	4
LATPAH	LATPA with 2x Drive	5
LATPI4	4-Bit Latch with Inverting Output	14
LATPI4H	LATPI4 with 2x Drive	14
CCNDRS	S-R Latch with Set, Reset and Separate Gated Inputs	4
CCNDRSG	S-R Latch with Set, Reset and Common Gated Inputs	4
L1LSSD	D-Type Latch with Scan Test Inputs	8
L1LSSDH	L1LSSD with 2x Drive	8
LSSD1A	LSSD Latch with Scan	12
LSSD1AH	LSSD1A Latch with 2x Drive	14
LSSD2	LSSD2 Latch with Scan	16
LSSD2H	LSSD2 Latch with 2x Drive	18
SRLSSD1	D-Type Latch with Scan into D-Type Latch	12
SRLSSD1H	SRLSSD1 with 2x Drive	13

MULTIPLEXERS

MUX2A*	2-Input Multiplexer	3
MUX2H	2-Input Multiplexer with 2x Drive	3
MUX2I	2-Input Multiplexer, Inverted Output	3
MUX2IH	MUX2I with 2x Drive	3
MUX4*	4-Input Multiplexer	8
MUX4H	MUX4 with 2x Drive	8
MX41*	4-Input Multiplexer with Individual Selects	5
MX41H*	MX41 with, 2x Drive	6
MX61	6-Input Multiplexer with Individual Selects	8
MX61H	MX61 with, 2x Drive	9
MX81*	8-Input Multiplexer with Individual Selects	10
MX81H	MX81 with, 2x Drive	12
MUX8H	8-Input Multiplexer with 2x Drive	14

INTERNAL MACROCELLS		GATES

MULTIPLEXERS (continued)

MUX41	Four 2-1 MUX with Common Select	10
MUX41H	MUX41 with 2x Drive	12
MUX41I*	MUX41, Inverted Output	8
MUX41IH*	MUX41I with 2x Drive	10
MUXE41	MUX41 with Common Enable	12
MUXE41H	MUXE41 with 2x Drive	14

DECODERS

DEC4	1 of 4 Decoder, Active Low Outputs	5
DEC4H	DEC4 with 2x Drive	9
DEC4A	1 of 4 Decoder, Active High Outputs	10
DEC4AH	DEC4A with 2x Drive	14
DEC1OF8	1of 8 Decoder with Enable, Active Low Outputs	16
DEC8	1 of 8 Decoder	16
DEC8A	1 of 8 Decoder with Enable, Active High Outputs	30
DEC8AH	DEC8A with 2x Drive	30

ARITHMETIC CIRCUITS

ADFUL	Full Adder	10
ADFULH	ADFUL with 2x Drive	10
ADFULHA	ADFUL with 2x Drive	10
ADHALF	Half Adder	6
ADHALFH	ADHALF with 2x Drive	6
AD4FUL	Full 4-Bit Adder	40
AD4FULA	Full 4-Bit Adder with 2x Drive	40
AD4PG	Full 4-Bit Adder with Propagate & Generate	94
ADD5	Add 5-Bits	20
ADD5A	Add 5-Bits	20
LACG4	4-Bit Look-Ahead-Carry Generator	32
MCOMP2	2-bit Magnitude Comparator	18
MCOMP4	4-bit Magnitude Comparator	35
MUL8X8	8-bit Multiplier	1106
ECOMP4	4-Bit Equality Comparator	16
SBHALF	Half Subtracter	6
SBHALFH	SBHALF with 2x Drive	6

MISCELLANEOUS

DLY8	8-Stage Inverter Delay	4
DLY100*	100-Stage Inverter Delay	50
DCR4	4-Bit Decrementer	26
DCR4H	DCR4 with 2x Drive	28
INC4	4-Bit Incrementer	27
INC4H	INC4 with 2x Drive	28
PAR4	4-Bit Parity Checker	14
ROT8	8-Bit Rotate	72
ROT8A*	8-Bit Rotate, Low Power	54
SHIFT8	8-Bit Shift Register	45

* Available in Phase 2.

INTERNAL MACROCELLS		GATES

BIST SOFT MACROS*

ADDR_CELL	Address Counter Cell	~ 20
DATA_CELL	Pattern Generator & Signature Analysis	~ 25

METALLIZED RAMS

RSA8x8*	Single Port RAM, Low Power	198
RSA8x18	Single Port RAM, Low Power	440
RSA16x8*	16x8 Single Port RAM, Low Power	342
RSA16x18	16x18 Single Port RAM, Low Power	760
RSA16x36	16x36 Single Port RAM, Low Power	1440
RSA32x8	32x8 Single Port RAM, Low Power	630
RSA32x18	32x18 Single Port RAM, Low Power	1400
RSA32x36	32x36 Single Port RAM, Low Power	2660
RSA64x18	64x18 Single Port RAM, Low Power	2680
RSA64x36	64x36 Single Port RAM, Low Power	5092
RDA8x9	8x9 High Speed Dual Port RAM	356
RDA8x18	8x18 High Speed Dual Port RAM	608
RDA8x36	8x36 High Speed Dual Port RAM	1112
RDA8x72	8x72 High Speed Dual Port RAM	2156
RDA16x9	16x9 High Speed Dual Port RAM	725
RDA16x18	16x18 High Speed Dual Port RAM	1193
RDA16x36	16x36 High Speed Dual Port RAM	2129
RDA16x72	16x72 High Speed Dual Port RAM	4050
RDA32x9	32x9 High Speed Dual Port RAM	1400
RDA32x18	32x18 High Speed Dual Port RAM	2300
RDA32x36	32x36 High Speed Dual Port RAM	4100
RDA32x72	32x72 High Speed Dual Port RAM	7798
RQ16x18*	16x18 Quad Dual Port RAM	2200
RQ16x36*	16x36 Quad Dual Port RAM	3766
RQ32x18*	32x18 Quad Dual Port RAM	4762
RQ32x36*	32x36 Quad Dual Port RAM	7738

CLOCK SKEW MANAGEMENT		GATES

PHASE LOCKED LOOP MACROCELLS*

DLYLN6	6-Bit Delay Line	462
DLYLN7	7-Bit Delay Line	702
PHSDET	Phase Detector	162
PLLCTR7	7-Bit Counter	288

* Available in Phase 2.

LIBRARY SUMMARY	FUNCTIONS

INTERNAL MACROS

Inverters	1
Buffers	2
3-State Inverters and Buffers	4
Schmitt Trigger Buffers	2
And & Nand Gates	10
Or & Nor Gates	10
Exor & Exnor Gates	6
And/Nor, And/Or, Or/Nand & Or/And Gates	17
D Flip-Flops	21
JK Flip-Flops	6
Toggle Flip-Flops	2
Latches	14
Multiplexers	10
Decoders	5
Arithmetic Functions	14
Miscellaneous	9
RAMs (Metallized)	26
Clock Skew Management (Phase Locked Loop)	4
Soft Macros	5
JTAG Control Functions	6
JTAG Boundary Scan Functions	9

Total number of internal library cells: 287 (as a result of high drive, complementary output, etc.)

Ex: NAN2, NAN2H and NAN2B count as only one function, but are three different library cells. INV, INVB, INV2, INV2B, INV3, INV3B, INV4, INV4B, INV8, INV8B and INVX also count as only one function. This relationship extends throughout the library, along with descriptions of all cell capabilities (high drive, etc.), in the listings on Pages 8 through 11 of this Data Sheet.

Total number of non-JTAG periphery cell combinations: 421

- Input Cell
  Combinations: 50
- Output Cell
  Combinations: 21
- Bidirectional Cell
  Combinations: 350

Total number of JTAG periphery cell combinations: 358

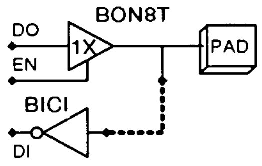
- Input Cell
  Combinations: 45 + 10
- Output Cell
  Combinations: 21 + 2
- Bidirectional Cell
  Combinations: 280

MACROCELL EXAMPLES

INPUT/OUTPUT MACROCELLS

BON8T/BICI – Non–Inverting Bidirectional Buffer with CMOS Input Switching Levels

The BON8T and BICI cells are used together to form a complete bidirectional macrocell. A "weak" or "strong" pullup/pulldown resistor can optionally be attached (at the dotted line) during schematic capture.



Normal Bidirectional

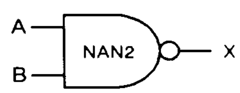
CMOS SWITCHING CHARACTERISTICS (Input t_r, t_f = 1.0 ns; V_{DD} = 5 V; T_A = 25°C; typical process; C_L = as shown)

Symbol	Parameter	Typ	Unit
t_{PLH}	Propagation Delay, BON8T: DO to PAD C_L = 50 pF	3.10	ns
t_{PHL}		2.67	
t_{PLZ}	Propagation Delay, BON8T: EN to PAD C_L = 50 pF R_L = 500 Ω	3.16	ns
t_{PZL}		2.32	
t_{PZH}		6.21	
t_{PHZ}		2.30	
t_{PLH}	Propagation Delay, BICI: PAD to DI C_L = 0.13 pF	0.24	ns
t_{PHL}		0.19	

FUNCTION TABLE

EN	PAD	DO	DI	PAD	Function
L	L/H	X	H/L	Z	The pin functions as an input. Data from the internal array is disabled and data from the PAD input is enabled.
H	L/H	L/H	L/H	L/H	The pin functions as an output, with data originating from the internal array at point DO. The data at point DO appears at the PAD output and at point DI.

INTERNAL MACROCELLS (COMBINATORIAL)



$X = \overline{A \bullet B}$

2–Input NAND Gate
NAN2 – 1/2 Cell – 1 Equivalent Gate
NAN2H – 1 Cell – 2 Equivalent Gates (High Drive)
NAN2B – 1 Cell – 2 Equivalent Gates (Balanced Drive)

CMOS SWITCHING CHARACTERISTICS (Input Edge Rate: t_r,t_f, = 1.0ns) Rev. 1.18

SYM	Parameter	Nom. V_{DD} = 5.0 V, T_J = 25 °C							
		FO=0	FO=1	FO=2	FO=4	FO=8	Unit	K	Unit
	NAN2								
t_{PLH}	Propagation Delay, A to X	0.17	0.26	0.34	0.50	0.84	ns	1.38	ns/pF
t_{PHL}		0.12	0.18	0.24	0.35	0.57	ns	0.94	ns/pF
t_{PLH}	Propagation Delay, B to X	0.20	0.29	0.37	0.53	0.86	ns	1.37	ns/pF
t_{PHL}		0.11	0.17	0.23	0.34	0.56	ns	0.94	ns/pF
t_r	Output Rise Time, X	0.14	0.31	0.49	0.84	1.55	ns	2.94	ns/pF
t_f	Output Fall Time, X	0.08	0.19	0.30	0.52	0.97	ns	1.86	ns/pF
	NAN2H								
t_{PLH}	Propagation Delay, A to X	0.16	0.21	0.25	0.33	0.50	ns	0.69	ns/pF
t_{PHL}		0.12	0.15	0.18	0.23	0.35	ns	0.47	ns/pF
t_{PLH}	Propagation Delay, B to X	0.20	0.24	0.29	0.37	0.54	ns	0.69	ns/pF
t_{PHL}		0.11	0.14	0.16	0.22	0.33	ns	0.47	ns/pF
t_r	Output Rise Time, X	0.16	0.24	0.33	0.51	0.86	ns	1.46	ns/pF
t_f	Output Fall Time, X	0.10	0.16	0.21	0.32	0.54	ns	0.90	ns/pF
	NAN2B								
t_{PLH}	Propagation Delay, A to X	0.15	0.19	0.23	0.32	0.48	ns	0.69	ns/pF
t_{PHL}		0.17	0.22	0.28	0.39	0.62	ns	0.94	ns/pF
t_{PLH}	Propagation Delay, B to X	0.17	0.21	0.25	0.33	0.50	ns	0.69	ns/pF
t_{PHL}		0.15	0.20	0.26	0.37	0.60	ns	0.94	ns/pF
t_r	Output Rise Time, X	0.12	0.21	0.30	0.47	0.82	ns	1.46	ns/pF
t_f	Output Fall Time, X	0.10	0.21	0.33	0.55	0.99	ns	1.86	ns/pF

FO capacitance does not include estimated metal lengths

INTERNAL MACROCELLS (SEQUENTIAL)

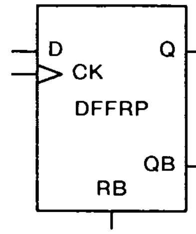
DFFRP – D Flip–Flop with Reset
4 Cells – 8 Equiv Gates
DFFRLP – Scan D Flip–Flop with Reset
5 1/2 Cells – 11 Equiv Gates

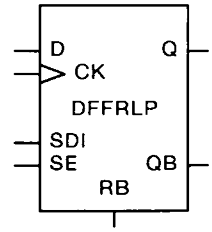
Pin Names:
- D – Data
- CK – Clock
- RB – Reset
- Q – Data Output
- QB – Data Output
- SDI* – Scan Data In
- SE* – Scan Enable

FUNCTION TABLE

D	SDI*	SE*	CK	RB	Q	QB
L	X	L	↑	H	L	H
H	X	L	↑	H	H	L
X	L	H	↑	H	L	H
X	H	H	↑	H	H	L
X	X	X	↓	H	Q	QB
X	X	X	X	L	L	H

* SDI & SE not applicable on DFFRP





CMOS SWITCHING CHARACTERISTICS (Input Edge Rate: t_r,t_f, = 1.0ns) Rev. 1.18

SYM	Parameter	Nom. V_{DD} = 5.0 V, T_J = 25 °C							
		FO=0	FO=1	FO=2	FO=4	FO=8	Unit	K	Unit
	DFFRP								
t_{PLH}	Propagation Delay, CK to Q	0.87	0.95	1.03	1.20	1.53	ns	1.38	ns/pF
t_{PHL}		0.96	1.00	1.03	1.10	1.24	ns	0.58	ns/pF
t_{PLH}	Propagation Delay, CK to QB	1.09	1.17	1.26	1.42	1.75	ns	1.38	ns/pF
t_{PHL}		1.08	1.12	1.15	1.22	1.35	ns	0.56	ns/pF
t_{PHL}	Propagation Delay, RB to Q	0.48	0.51	0.55	0.62	0.76	ns	0.58	ns/pF
t_{PLH}	Propagation Delay, RB to QB	0.62	0.70	0.79	0.95	1.28	ns	1.38	ns/pF
t_r	Output Rise Time, Q	0.11	0.29	0.46	0.81	1.52	ns	2.93	ns/pF
t_f	Output Fall Time, Q	0.16	0.22	0.28	0.40	0.64	ns	1.00	ns/pF
t_r	Output Rise Time, QB	0.07	0.25	0.43	0.78	1.49	ns	2.94	ns/pF
t_f	Output Fall Time, QB	0.12	0.18	0.24	0.36	0.60	ns	1.01	ns/pF
	DFFRLP								
t_{PLH}	Propagation Delay, CK to Q	0.85	0.94	1.02	1.18	1.52	ns	1.38	ns/pF
t_{PHL}		1.05	1.09	1.12	1.19	1.33	ns	0.58	ns/pF
t_{PLH}	Propagation Delay, CK to QB	1.19	1.27	1.35	1.52	1.85	ns	1.38	ns/pF
t_{PHL}		1.03	1.06	1.10	1.17	1.30	ns	0.56	ns/pF
t_{PHL}	Propagation Delay, RB to Q	0.43	0.47	0.50	0.57	0.71	ns	0.58	ns/pF
t_{PLH}	Propagation Delay, RB to QB	0.57	0.65	0.74	0.90	1.23	ns	1.38	ns/pF
t_r	Output Rise Time, Q	0.11	0.29	0.46	0.81	1.52	ns	2.93	ns/pF
t_f	Output Fall Time, Q	0.15	0.21	0.27	0.39	0.63	ns	1.01	ns/pF
t_r	Output Rise Time, QB	0.07	0.25	0.43	0.78	1.49	ns	2.94	ns/pF
t_f	Output Fall Time, QB	0.10	0.16	0.22	0.34	0.59	ns	1.02	ns/pF

FO capacitance does not include estimated metal lengths

Timing Requirements (input Edge Rate: t_r,t_f = 1.0ns)

SYM	Parameter	Minimum Requirement	
		Nom. 5 V, 25°C	Unit
	DFFRP		
t_{su}	Set Up Time, D to CK	0.48	ns
t_h	Hold Time, CK to D	0.11	ns
t_{rec}	Recovery Time, RB to CK	–0.12	ns
t_w	Pulse Width, CK (L)	0.90	ns
	CK (H)	0.67	ns
	RB (L)	0.64	ns

SYM	Parameter	Minimum Requirement	
		Nom. 5 V, 25°C	Unit
	DFFRLP		
t_{su}	Set Up Time, D,SDI,SE to CK	0.79	ns
t_h	Hold Time, CK to D,SDI,SE	–0.13	ns
t_h	Hold Time, CK to SE	–0.05	ns
t_{rec}	Recovery Time, RB to CK	–0.14	ns
t_w	Pulse Width, CK (L)	1.00	ns
	CK (H)	0.71	ns
	RB (L)	0.61	ns

MACROCELL EXAMPLES (continued)

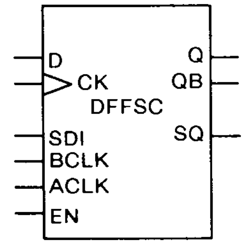
INTERNAL MACROCELLS (SEQUENTIAL)

DFFSC – D Flip–Flop W/Scan Latch
8 Cells – 16 Equiv Gates

Pin Names:
- D - Data
- CK - Clock
- EN - Enable
- BCLK - B Clock
- ACLK - A Clock
- QB - Data Output
- QB - Data Output
- SDI - Scan Data In

D	EN	CK	SDI	BCLK	ACLK	Q	QB	SQ	Notes
X	X	L	X	L	L	Q	QB	SQ	1
X	L	↑	X	L	L	Q	QB	SQ	2
L	H	↑	X	L	L	L	H	SQ	3
H	H	↑	X	L	L	H	L	SQ	3
X	X	L	X	L	H	Q	QB	QB	4
X	X	L	L	H	L	H	L	SQ	5
X	X	L	H	H	L	L	H	SQ	5
X	X	L	L	H	H	H	L	L	6
X	X	L	H	H	H	L	H	H	6

1. No Clock 2. Active Clock, disabled
3. Active Clock, enabled 4. Scan-out Clock applied
5. Scan-in Clock applied 6. Flush or Ring-oscillate



CMOS SWITCHING CHARACTERISTICS (Input Edge Rate: t_r, t_f, = 1.0ns) Rev. 1.18

SYM	Parameter	Nom. V_{DD} = 5.0 V, T_J = 25 °C							
		FO=0	FO=1	FO=2	FO=4	FO=8	Unit	K	Unit
		DFFSC							
t_{PLH}	Propagation Delay, ACLK to SQ	0.60	0.68	0.77	0.93	1.27	ns	1.38	ns/pF
t_{PHL}		0.55	0.59	0.62	0.69	0.83	ns	0.57	ns/pF
t_{PLH}	Propagation Delay, BCLK to Q	0.47	0.52	0.56	0.64	0.81	ns	0.71	ns/pF
t_{PHL}		0.75	0.79	0.83	0.91	1.07	ns	0.68	ns/pF
t_{PLH}	Propagation Delay, BCLK to QB	0.98	1.02	1.06	1.14	1.31	ns	0.69	ns/pF
t_{PHL}		0.96	1.00	1.04	1.11	1.25	ns	0.59	ns/pF
t_{PLH}	Propagation Delay, BCLK to SQ	1.61	1.70	1.78	1.94	2.27	ns	1.37	ns/pF
t_{PHL}		1.49	1.52	1.56	1.63	1.76	ns	0.57	ns/pF
t_{PLH}	Propagation Delay, CK to Q	0.96	1.00	1.04	1.13	1.30	ns	0.71	ns/pF
t_{PHL}		0.95	0.99	1.03	1.12	1.28	ns	0.68	ns/pF
t_{PLH}	Propagation Delay, CK to QB	1.19	1.23	1.28	1.36	1.53	ns	0.70	ns/pF
t_{PHL}		1.46	1.50	1.54	1.61	1.75	ns	0.59	ns/pF
t_{PLH}	Propagation Delay, CK to SQ	1.95	2.03	2.11	2.28	2.61	ns	1.37	ns/pF
t_{PHL}		2.06	2.09	2.13	2.20	2.34	ns	0.57	ns/pF
t_{PLH}	Propagation Delay, SDI to Q	0.46	0.51	0.55	0.63	0.80	ns	0.71	ns/pF
t_{PHL}		0.63	0.67	0.71	0.79	0.95	ns	0.68	ns/pF
t_{PLH}	Propagation Delay, SDI to QB	0.84	0.88	0.92	1.01	1.18	ns	0.70	ns/pF
t_{PHL}		0.96	0.99	1.03	1.10	1.24	ns	0.59	ns/pF
t_{PLH}	Propagation Delay, SDI to SQ	1.47	1.55	1.64	1.80	2.13	ns	1.38	ns/pF
t_{PHL}		1.48	1.51	1.55	1.62	1.75	ns	0.57	ns/pF
t_r	Output Rise Time, Q	0.18	0.26	0.35	0.52	0.86	ns	1.43	ns/pF
t_f	Output Fall Time, Q	0.35	0.41	0.47	0.59	0.83	ns	1.01	ns/pF
t_r	Output Rise Time, QB	0.14	0.23	0.32	0.49	0.83	ns	1.43	ns/pF
t_f	Output Fall Time, QB	0.20	0.26	0.32	0.44	0.68	ns	0.99	ns/pF
t_r	Output Rise Time, SQ	0.11	0.29	0.47	0.82	1.52	ns	2.93	ns/pF
t_f	Output Fall Time, SQ	0.15	0.21	0.27	0.39	0.63	ns	1.01	ns/pF

FO capacitance does not include estimated metal lengths

CMOS TIMING REQUIREMENTS (Input Edge Rate: t_r, t_f, = 1.0ns) Rev. 1.18

SYM	Parameter	Minimum Requirement		SYM	Parameter	Minimum Requirement	
		Nom. 5.0 V, 25 °C	Unit			Nom. 5.0 V, 25 °C	Unit
		DFFSC					
t_{su}	Set Up Time: BCLK to ACLK	1.44	ns	t_h	Hold Time: CK to BCLK	–0.91	ns
t_{su}	Set Up Time: CK to ACLK	1.77	ns	t_h	Hold Time: CK to D	0.41	ns
t_{su}	Set Up Time: SDI to ACLK	1.47	ns	t_h	Hold Time: CK to EN	0.18	ns
t_{su}	Set Up Time: SDI to BCLK	1.13	ns	t_{rec}	Recovery Time: CK to ACLK	–1.48	ns
t_{su}	Set Up Time: D to CK	0.26	ns	t_{rec}	Recovery Time: ACLK to CK	1.97	ns
t_{su}	Set Up Time: EN to CK	0.55	ns	t_w	Pulse Width: ACLK(L)	0.31	ns
t_h	Hold Time: ACLK to BCLK	–0.99	ns	t_w	Pulse Width: ACLK(H)	0.31	ns
t_h	Hold Time: ACLK to CK	–1.07	ns	t_w	Pulse Width: BCLK(L)	0.99	ns
t_h	Hold Time: ACLK to SDI	–0.93	ns	t_w	Pulse Width: BCLK(H)	0.99	ns
t_h	Hold Time: BCLK to CK	–0.97	ns	t_w	Pulse Width: CK(L)	0.84	ns
t_h	Hold Time: BCLK to SDI	0.17	ns	t_w	Pulse Width: CK(H)	1.16	ns

MACROCELL EXAMPLES (continued)

INTERNAL MACROCELLS (METALLIZED SRAM BLOCKS)

Random Access Memories

Motorola offers 26 different building blocks that can be used to construct Single, Dual and Four Port memories. A comprehensive guide to using these blocks and their performance is shown in the H4C Series Reference Guide.

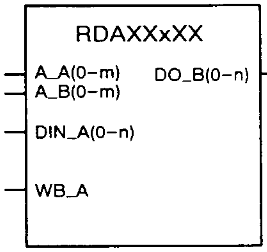
Multiple Memory Blocks

It is possible to combine two or more memory blocks to create larger memory blocks. When multiple blocks are used, the user is responsible for creating the external decoder logic needed. The maximum number of SRAM blocks on an array is restricted to 16, depending on array/SRAM sizes.

Array Sizing

To choose an array into which a design with SRAM will fit, two considerations must be evaluated: the physical size/layout of the SRAM or SRAMs and the gate utilization.

RDAXXxXX – High Speed Dual Port SRAM
Equivalent Gates: see below



Pin Names:
- A_A(0–m) – address bus for Port A
- A_B(0–m) – address bus for Port B
- DIN_A (0–n) – input data
- WB_B – Write enable bus for Port A
- DO_B (0–n) – data output

Size, Address Line Input Capacitance, and Array Availability Information for Dual Port RAMs

Size (Words X Bits)	Name	Available Arrays	Size (Columns X Rows)	Total Gate Count	Port A Input Capacitance Per Address Line	Port A Input Capacitance WB_A Line	Port B Input Capacitance Per Address Line
8–WORD BLOCK							
8X9	RDA8X9	27K – 318K	13X14	356	0.15 pF	0.18 pF	0.15 pF
8X18	RDA8X18	27K – 318K	22X14	608			
8X36	RDA8X36	27K – 318K	40X14	1112			
8X72	RDA8X72	27K – 318K	77X14	2156			

SWITCHING CHARACTERISTICS (Input Edge Rate: t_r,t_f = 1.0ns)

SYM	Parameter	Nom. V_{DD}= 5.0 V, T_J=25 °C								
		Abbr.	FO=0	FO=1	FO=2	FO=4	FO=8	Unit	K	Unit
8–WORD BLOCK										
t_{PLH}	Address Access Time, 9 – Bits	t_{AA}	1.97	2.06	2.15	2.32	2.68	ns	1.47	ns/pF
t_{PHL}		t_{AA}	3.46	3.50	3.53	3.60	3.73	ns	0.56	ns/pF
t_{PLH}	Address Access Time, 18 – Bits	t_{AA}	2.93	3.02	3.11	3.28	3.64	ns	1.47	ns/pF
t_{PHL}		t_{AA}	1.98	2.01	2.05	2.11	2.25	ns	0.56	ns/pF
t_{PLH}	Address Access Time, 36 – Bits	t_{AA}	3.46	3.55	3.64	3.81	4.16	ns	1.47	ns/pF
t_{PHL}		t_{AA}	2.22	2.25	2.29	2.35	2.49	ns	0.56	ns/pF
t_{PLH}	Address Access Time, 72 – Bits	t_{AA}	4.08	4.17	4.26	4.43	4.78	ns	1.47	ns/pF
t_{PHL}		t_{AA}	2.70	2.73	2.77	2.83	2.97	ns	0.56	ns/pF
t_{PLH}	Propagation Delay, WB to DO(n) (WL=9)	t_{WDO}	3.94	4.02	4.12	4.30	4.65	ns	1.47	ns/pF
t_{PHL}		t_{WDO}	2.98	3.01	3.05	3.11	3.25	ns	0.56	ns/pF
t_{PLH}	Propagation Delay, WB to DO(n) (WL=18)	t_{WDO}	4.34	4.43	4.52	4.70	5.05	ns	1.47	ns/pF
t_{PHL}		t_{WDO}	3.18	3.21	3.24	3.31	3.45	ns	0.56	ns/pF
t_{PLH}	Propagation Delay, WB to DO(n) (WL=36)	t_{WDO}	5.00	5.09	5.18	5.35	5.70	ns	1.47	ns/pF
t_{PHL}		t_{WDO}	3.72	3.76	3.79	3.86	3.99	ns	0.56	ns/pF
t_{PLH}	Propagation Delay, WB to DO(n) (WL=72)	t_{WDO}	5.64	5.72	5.81	5.99	6.34	ns	1.47	ns/pF
t_{PHL}		t_{WDO}	4.22	4.26	4.29	4.36	4.49	ns	0.56	ns/pF
t_{PLH}	Propagation Delay, DIN(n) to DO(n)	t_{DDO}	2.37	2.46	2.55	2.72	3.08	ns	1.47	ns/pF
t_{PHL}		t_{DDO}	2.01	2.04	2.08	2.14	2.28	ns	0.56	ns/pF
t_r	Output Rise Time DO(n)	N/A	1.22	1.41	1.61	2.01	2.80	ns	3.29	ns/pF
t_f	Output Fall Time DO(n)	N/A	0.58	0.66	0.74	0.90	1.23	ns	1.36	ns/pF

FO capacitance does not include estimated metal lengths

INTERNAL MACROCELLS (METALLIZED SRAM BLOCKS) continued

RDAXXxXX – High Speed Dual Port SRAM

TIMING REQUIREMENTS (Input Edge Rate: t_r, t_f = 1.0ns)

Sym	Parameter	Minimum Requirement	
		Nom. 5.0V, 25 °C	Unit
8 –WORD BLOCK			
t_{DSU}	Set Up Time, DIN_A(n) to WB_A (WL = 9)	2.01	ns
	DIN_A(n) to WB_A (WL = 18)	2.19	ns
	DIN_A(n) to WB_A (WL = 36)	2.40	ns
	DIN_A(n) to WB_A (WL = 72)	3.09	ns
t_{AWB}	Set Up Time, A_A(n) to WB_A	0.25	ns
t_{DH}	Hold Time, DIN_A(n) to WB_A (WL = 9)	0.96	ns
	DIN_A(n) to WB_A (WL = 18)	1.10	ns
	DIN_A(n) to WB_A (WL = 36)	1.22	ns
	DIN_A(n) to WB_A (WL = 72)	1.70	ns
	A_A(n) to WB_A	0.00	ns
t_{PW}	Pulse Width WB_A (L) (WL = 9)	2.85	ns
	WB_A (L) (WL = 18)	3.17	ns
	WB_A (L) (WL = 36)	3.84	ns
	WB_A (L) (WL = 72)	5.11	ns
	WB_A (H) (WL = 9)	1.41	ns
	WB_A (H) (WL = 18)	1.56	ns
	WB_A (H) (WL = 36)	2.02	ns
	WB_A (H) (WL = 72)	2.60	ns

INTERNAL MACROCELLS (DIFFUSED SRAM BLOCKS)

Memorist ™ Compiler

The Memorist SRAM Compiler is a module available in OACS 2.0 that is used before or during the Design Capture phase of the OACS design process. Motorola's Memorist SRAM Compiler tool automates the creation of fully diffused single and dual port synchronous SRAM blocks. The SRAM is immediately available to the user, on the workstation with necessary symbols, files and entries to enable it to be embedded in the gate array environment as if it were an element in the standard library. The word length and word configuration limits are:

Available word lengths: 1 – 256 bits/word
Available word blocks: 16 – 16,384 words/block

Why Diffused SRAMs?

Why use Memorist diffused SRAMs rather than selecting a metallized SRAM from the standard H4C Library?

- Memorist diffused SRAM's are more efficient then metallized SRAMs (above 2K bits): Metallized SRAMs have > 2.2 gates/bits density, while Memorist SRAMs have > 0.5 gates/bits density
- The performance is better than conventional gate array metallized SRAM implementation.
- Memorist allows flexible implementation of fully diffused SRAMs with hundreds of thousands of different configurations.

Features of Memorist:

- Memorist seeks to be completely "turnkey" by automating all necessary functions for producing a SRAM; from front–end design and characterization to layout generation through automatic place–and–route to back–end verification.
- Memorist allows the user to select accuracy levels versus CPU time tradeoffs in timing charactization for rapid design evaluation.
- Memorist operates completely on the customer's workstation, eliminating the need for direct engineering support from the ASIC Factory or a Regional Design Center.

Access Time VS. Number of Words/Word Lengths

Given a SRAM configuration, such as 1Kx8, there can be up to 40 different implementations. These reflect the different aspect ratios and multi–block configurations. Thus, for each configuration, there can be a range of possible performance and area values. In general, as the performance increases, power and area also increases, and vice versa. Due to the large number of SRAMs available, specific information of performance and layout parameters are available only by using the Memorist SRAM Compiler. The following graphs (Figures 9 – 11) show estimated minimum cycle time, read access time, and equivalent gate count for various number of words and word lengths of the single port memories at typical conditions (typical process, V_{DD} = 5.0V, T_J = 25 °C). These graphs do not show the upper limit of the performance range and physical size.

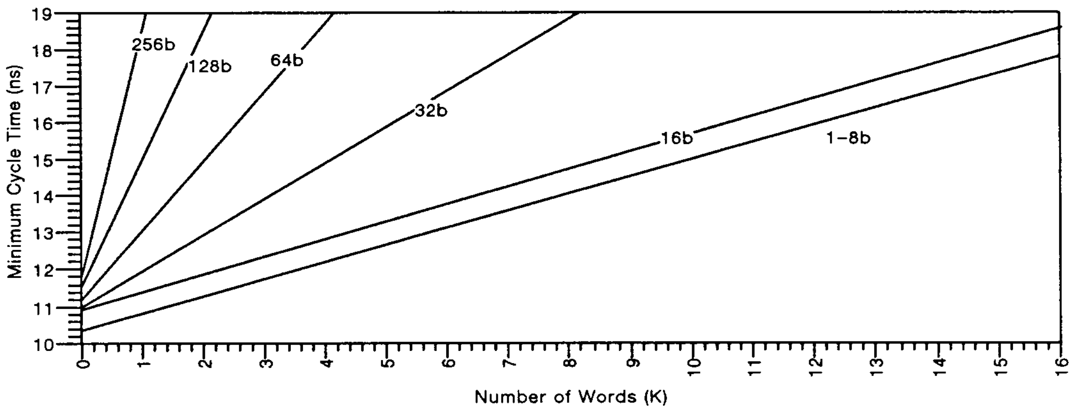


FIGURE 9 – Single Port Minimum Cycle Time vs. Number of Words for Various Word Lengths

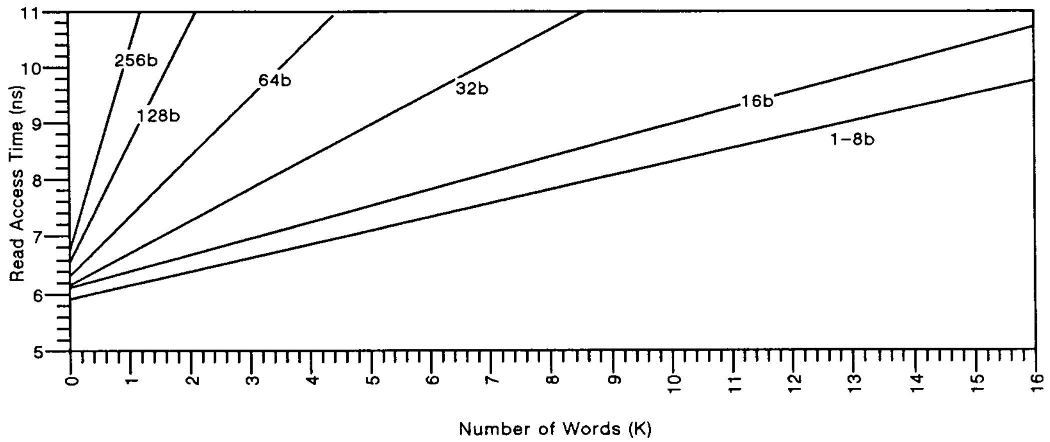


FIGURE 10 – Single Port Minimum Read Access Time vs. Number of Words for Various Word Lengths

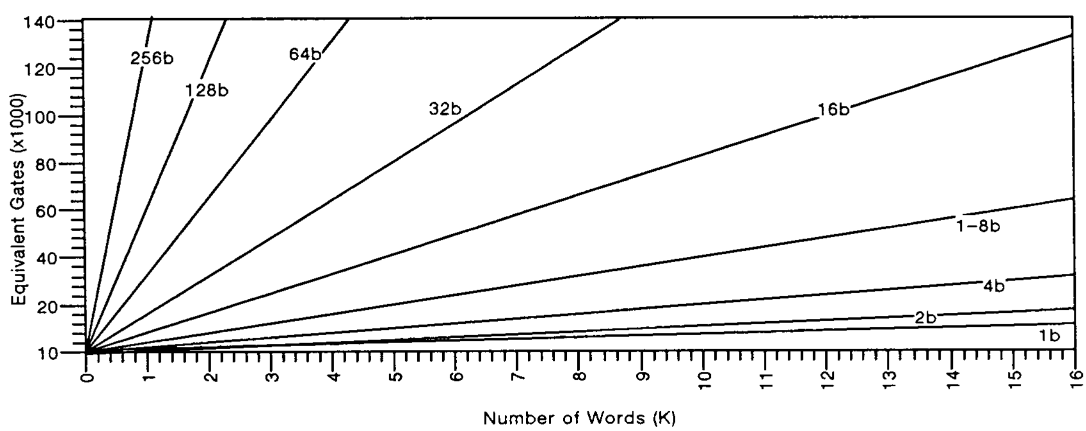


FIGURE 11 – Single Port Minimum Equivalent Gatecount vs. Number of Words for Various Word Lengths

Note: In all the above graphs b = bits

PRELIMINARY ELECTRICAL CONSIDERATIONS FOR H4C SERIES ARRAYS

4/28/91

TABLE 2 – ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	–0.5 to 7.0	V
V_{in}	DC Input Voltage	–1.5 to V_{DD}+1.5	V
V_{out}	DC Output Voltage	–0.5 to V_{DD}+0.5	V
I	DC Current Drain per Pin, Any Single Input or Output	25	mA
I	DC Current Drain per Pin, Any Paralleled Outputs	50	mA
I	DC Current Drain V_{DD} and V_{SS} Pins	75	mA
T_{stg}	Storage Temperature	–65 to +150	°C
T_L	Lead Temperature (10 second soldering)	300	°C

Note: Maximum ratings are those values beyond which damage to the device may occur.

TABLE 3 – RECOMMENDED OPERATING CONDITIONS (to guarantee functionality)

Symbol	Parameter	Min	Max	Unit
V_{DD}	DC Supply Voltage	3.0	6.0	V
V_{in}, V_{out}	Input Voltage, Output Voltage	0.0	V_{DD}	V
T_J	Commercial Operating Temperature	0	+70	°C
T_J	Industrial Operating Temperature	–40	+85	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

PRELIMINARY

TABLE 4 – DC ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0V ± 10%)

Sym	Parameter	Test Conditions	V_{DD}	25°C, 5.0 V Typical	0 to 70°C Guaranteed Limit		–40 to 85°C Guaranteed Limit		Unit
					MIN	MAX	MIN	MAX	
V_{IH}	Minimum High–Level Input Voltage, CMOS Input	V_{out} = 0.1 V or V_{DD} –0.1 V; $\|I_{out}\|$ =20 µA	5.0	2.4					V
				–	0.7 V_{DD}		0.7 V_{DD}		
	Minimum High–Level Input Voltage, TTL Input	V_{out} = 0.1 V or V_{DD} – 0.1 V; $\|I_{out}\|$ = 20 µA	4.5	–	2.0		2.0		
			5.0	1.6					
			5.5	–	2.2		2.2		
V_{IL}	Maximum Low–Level Input Voltage, CMOS Input	V_{out} = 0.1 V or V_{DD} – 0.1 V; $\|I_{out}\|$ = 20 µA	5.0	2.4					V
			5.5	–		0.3 V_{DD}		0.3 V_{DD}	
	Maximum Low–Level Input Voltage, TTL Input	V_{out} = 0.1 V or V_{DD} – 0.1 V; $\|I_{out}\|$ = 20 µA	5.0	1.5					
			5.5	–		0.8		0.8	
I_{OH}	Minimum High–Level Current	V_{OH} = 3.5 V							mA
		8 mA Output Type	4.5	>|20.0|	–12.0		–10.0		
		4 mA Output Type	4.5	>|10.0|	–6.0		–6.0		
		2 mA Output Type	4.5	>|5.0|	–2.0		–2.0		
I_{OL}	Minimum Low–Level Current	V_{OL} = 0.4 V							mA
		8 mA Output Type	4.5	>20.0	12.0		10.0		
		4 mA Output Type	4.5	>10.0	6.0		6.0		
		2 mA Output Type	4.5	>5.0	2.0		2.0		

PRELIMINARY

TABLE 4 – DC ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0V ± 10%)

Sym	Parameter	Test Conditions	V_{DD}	25°C, 5.0 V Typical	0 to 70°C Guaranteed Limit		–40 to 85°C Guaranteed Limit		Unit
					MIN	MAX	MIN	MAX	
V_{T+}	CMOS Schmitt Trigger	**Positive**							V
	Min Threshold Voltage	V_{out} = 0.1V or V_{DD} –0.1 V	–	C	C		C		
	Max Threshold Voltage	$\|I_{out}\|$ = 20 μA	–	C	C		C		
	TTL Schmitt Trigger								
	Min Threshold Voltage	V_{out} = 0.1V or V_{DD} –0.1 V	–	C	C		C		
	Max Threshold Voltage	$\|I_{out}\|$ = 20 μA	–	C	C		C		
V_{T-}	CMOS Schmitt Trigger	**Negative**							V
	Min Threshold Voltage	V_{out} = 0.1V or V_{DD} –0.1 V	–	C	C		C		
	Max Threshold Voltage	$\|I_{out}\|$ = 20 μA	–	C	C		C		
	TTL Schmitt Trigger								
	Min Threshold Voltage	V_{out} = 0.1V or V_{DD} –0.1 V	–	C	C		C		
	Max Threshold Voltage	$\|I_{out}\|$ = 20 μA	–	C	C		C		
⎍	Hysteresis –Schmitt CMOS	V_{T+} to V_{T-}							V
	Min		–	C	C		C		
	Max		–	C	C		C		
	Hysteresis –Schmitt TTL	V_{T+} to V_{T-}							
	Min		–	C	C		C		
	Max		–	C	C		C		
I_{in}	Maximum Input Leakage Current, No Pull Resistor	V_{in} = V_{DD} or V_{SS}	–	±0.15	–5.0	+5.0	–5.0	+5.0	μA
I_{in}	Maximum Input Leakage Current, PU macros for all input types	PUH;V_{in} = V_{SS}	–	–100	–50	–180	–50	180	μA
		PUL;V_{in} = V_{SS}	–	–60	–30	–140	–30	–140	
I_{in}	Maximum Input Leakage Current, PD macros for all input types	PDH;V_{in} = V_{DD}	–	185	100	300	100	300	μA
		PDL;V_{in} = V_{DD}	–	110	50	200	50	200	
I_{OZ}*	Maximum Output Leakage Current, 3-State Output	Output = High Impedance; V_{out} = V_{DD} or V_{SS}	–	± 1	–10	10	–10	10	μA
	Maximum Output Leakage Current, Open Drain Output (With Device Off)	Output = High Impedance; V_{out} = V_{DD}	–	± 1	–10	10	–10	10	
I_{DD}	Maximum Quiescent Supply Current, No Pullup or Pulldown Device ALL VALID INPUT COMBINATIONS	I_{out} = 0mA V_{in} = V_{DD} or V_{SS}	–		DESIGN DEPENDENT				

* Single Drive Output
C = consult factory

PACKAGING

Motorola offers four high performance, surface and through–hole mounted packages to complement the H4C Series arrays.

TAPE AUTOMATED BONDING

Tape Automated Bonding (TAB) represents the state–of–the–art in packaging technology. It provides high performance with ultra high pin density at low cost. In TAB technology the die pads are fabricated with gold bumps which are used to bond the die to an etched leadframe encased in polyimide tape. The assembled die and TAB tape are supplied ready to be placed in carrier (35 or 70 mm).

QFP in the MOLDED CARRIER RING

Motorola currently offers the popular EIAJ standard Plastic Quad Flat Package (QFP) in the Molded Carrier Ring (MCR). The MCR is a coplanarity and lead protection device for QFP packages, developed as an extension of the TAPEPAK™ license and registered as a JEDEC standard. The MCR provides lead protection during manufacturing/testing and shipping (optional) for the fragile fine pitch QFP leads; e.g.: the 28mm square 208 QFP has a 0.50mm pitch with lead thickness of 0.15mm.

Two MCR ring sizes are available. AA: 36mm^2 (supports the 64–100 pin packages with a 14mm X 20mm body) and AB: 46mm^2 (supports the 120–208 pin packages with a 28mm X 28mm body). Another advantage of the MCR is that it allows the use of thermally superior copper, and provides up to 1.5 Watts of power to be dissipated (dependent on temperature and ambient conditions). The MCR enables common manufacturing across the range of packages and a single test socket per ring size because of standardized ring sizes.

After the manufacturing and testing processes the customer may elect to do trim and form by receiving the QFP in the molded carrier ring. If the customer chooses to receive the parts excised, Motorola will trim and form the parts and ship in an industry standard QFP packing tray for lead protection.

All QFP's (with or without an MCR) will be shipped by Motorola baked and drypacked. The trend towards Surface Mount Technology (SMT) with high density, thinner packages (which are more sensitive to thermal stress failure during board mounting) has led Motorola to conduct numerous studies. The resultant action is a slow bake of moisture from the SMT package and shipping in drypack bags to shield the unit from moisture absorption. Units are baked at 125 °C for 24 hours, cooled and placed in the vacuum sealed drypack with desiccant bags, humidity indicator card, and lot identification stickers.

MicroCool™ QUAD FLAT PACK

The MicroCool QFP is a new QFP compatible plastic package with higher heat dissipation capacity. It has a heat slug attached to a printed circuit board which supports a copper lead frame. The package is supported within an MCR to maintain pin coplanarity. The MicroCool is a cost effective and high pin density package that is capable of meeting the higher power dissipation (up to 3 W, depending on temperature and ambient conditions) and higher performance requirements of the H4C Series.

PGA

Motorola will continue to support PGA (Pin Grid Array) packages for thru–hole mounting. Multiple power plane construction is especially important for high pin count and high performance applications.

Table 5 – Package Selection

ARRAY		H4C027	H4C035	H4C057	H4C086	H4C123	H4C161	H4C195	H4C318
# of I/O Cells		196	224	284	334	416	476	524	648
# of Programmable Signal or Power & Ground Pads*	Wire	144	154	188	216	256	284	308	384
	TAB	172	184	220	256	304	336	372	456
# of Dedicated Power & Ground Pads*	Wire	16	22	28	40	48	60	68	84
	TAB	16	24	36	48	56	72	72	100
128 QFP (MCR)		P	P						
160 QFP (MCR)			P	X	P	P			
208 QFP (MCR)				X	P	P			
160 MicroCool™ QFP				P	P	P	P	P	
208 MicroCool™ QFP				P	P	P	P	P	
188 TAB				D					
296 TAB				D		D		D	
376 TAB								P	
299 PGA(CD)						X			
375 PGA(CD)								X	
4XX PGA(CD)									TBD

*Numbers indicate Wire Bond and TAB pads availability

Package Availability:

X – Available
P – Planned
D – In Development (consult factory)

Package Types:

MCR– Molded Carrier Ring
MicroCool™– QFP–type package with heat slug.
PGA(CD)– Ceramic Pin Grid Array – (Cavity Down)
QFP– Plastic Quad Flat Pack
TAB– Tape Automated Bonding

AN INTEGRATED DESIGN SYSTEM SOLUTION

THE OPEN ARCHITECTURE CAD SYSTEM

Motorola's Open Architecture CAD System (OACS) offers a highly versatile and powerful design environment for the H4C Series, including logic synthesis, memory compilation, event-driven simulation, ATPG/fault simulation, static timing analysis and other sophisticated design tools. The OACS integrates several of the industry's most powerful design tools and Motorola's high-performance tools in an industry standard EDIF based CAD environment.

OACS™ Features:

- Supported on HP-Apollo® and SUN® 4 workstations
- Supports multiple technologies
- Industry standard EDIF 2.0.0 based netlist
- Motorola's Memorist™ SRAM Compiler (SP/DP)*
- Synopsys' Design Compiler™ and HDL Compiler™ logic synthesis tools
- Mentor Graphics' NetEd™ (Apollo) and Valid Logic's GED™ (SUN) schematic capture packages
- Design-For-Test support: ESSD/LSSD SCAN, JTAG*
- Sophisticated propagation delay and timing limits calculations for accurate simulations
  - Estimated and actual (back-annotated) wire capacitances
  - Includes intrinsic as well as slew rate, output pin loading and distributed RC delays
  - Continuous process, temperature, and voltage variation
- Functional, pre- and post-layout (back annotated) delay simulations through:
  - Cadence's Verilog XL® (HP-Apollo and SUN)
  - Mentor Graphics' QuickSim™ (HP-Apollo)
- Comprehensive Electrical Rules Checking (ERC)
- Cadence's Veritime™ Static Timing Analysis*
- Motorola's Mustang™ automatic test pattern generation
- Motorola's TestPAS™ test vector validation and extraction*
- Cadence's Gate Ensemble™ physical layout system
- Clock-tree synthesis, clock skew management, timing driven layout*

* available in OACS 2.0

FROM CONCEPT TO PRODUCT

From the conception of the design to fabrication of the product Motorola's design process flow is efficient, flexible and accurate. The design flow has three basic phases, Figure 12: pre-layout, layout, and post-layout design.

Pre-Layout

Pre-layout design is performed by the customer using the OACS to develop and simulate the ASIC product. In addition to schematic capture, designs can be synthesized using a hardware description language (HDL), equations, or truth tables. After the design has been described, an EDIF netlist is generated from the design database. At this point in the design phase, delay and timing calculations, netlist verification, automatic test pattern generation, or static timing analysis and fault grading can be performed. Pre-layout simulations use estimated best/typical/worst-case delays based on gate, load, slew rate, and estimated RC delays. Prior to the release of the design to layout, the test vectors created by the customer must pass specific rules to take full advantage of Motorola's production test equipment.

Layout

Layout design is performed by Motorola's Option Development Engineers (ODE). An ODE is dedicated to each option and works directly with the customer to satisfy their layout requirements. Options such as timing driven layout and clock tree synthesis are available to optimize silicon performance. Upon completion of the physical design, back-annotation data of actual wire routing lengths and RC parasitics is provided to the customer for post-layout verification.

Post-Layout

The post-layout design is performed by the customer to assure that the physical layout of the design satisfies all performance and timing requirements. Post-layout simulations use the actual wire lengths and RC parasitics obtained from the physical layout to provide simulations that represent the circuit's behavior in silicon. Following a successful post-layout design verification and customer sign off Motorola will start the manufacturing of the ASIC design.

AN INTEGRATED DESIGN SYSTEM SOLUTION

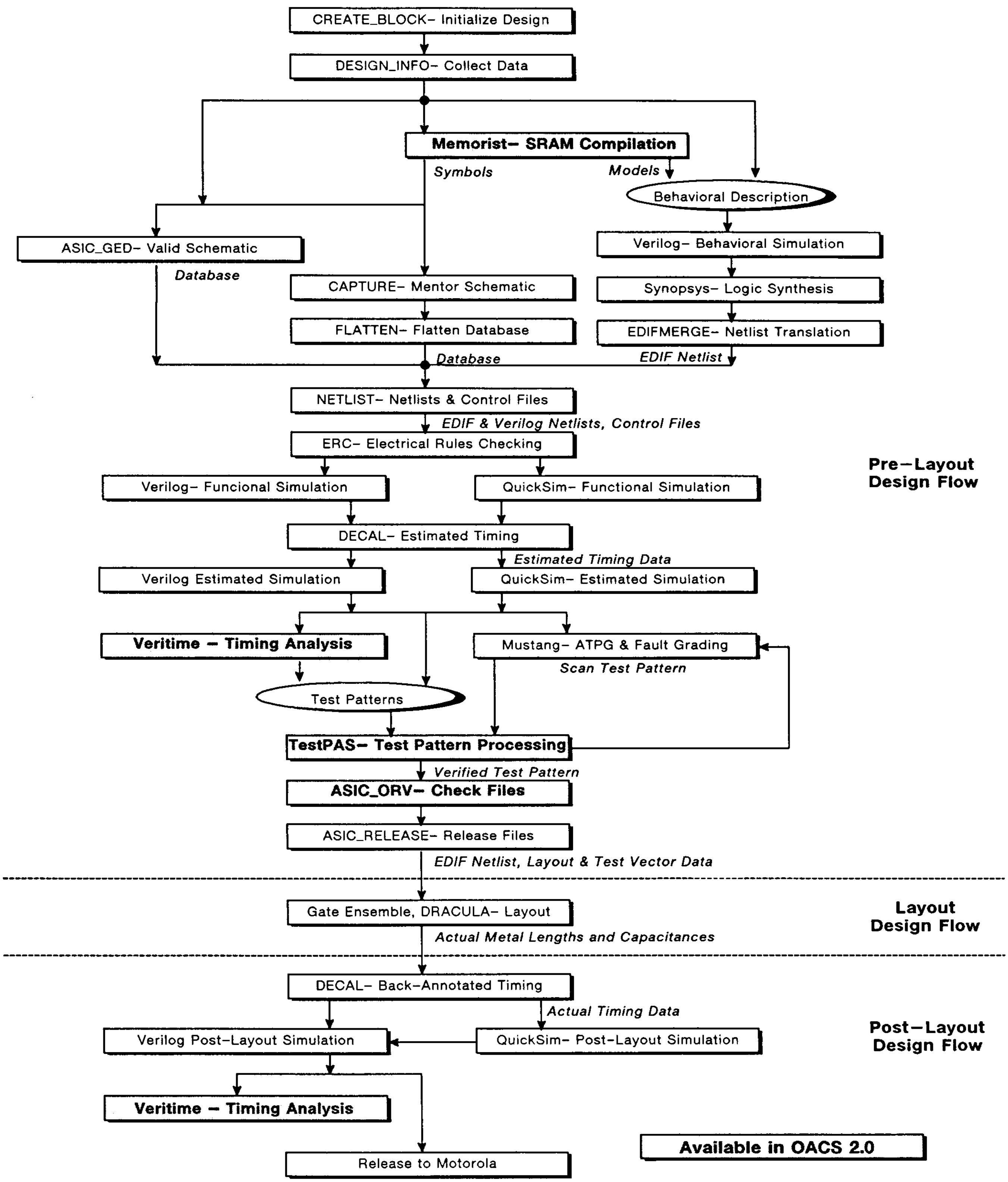


FIGURE 12 — OACS Design Flow