Integrated Device Technology, Inc.

3.3V 128K (8Kx16-BIT) CACHE-TAG SRAM For 3.3V Processors

PRELIMINARY
IDT71V218

FEATURES:

- 8K x 16 Configuration
  - 14 Common I/O TAG Bits
  - 2 Separate I/O Status Bits (VLD and DTY)
- Optimized for 256KB cache and 4GB cacheable space
- High-Speed Address-to-Match comparison times
  - 10/12/15ns
- Optional inclusion of Valid bit in Match output
- Asynchronous Read, Match, and Reset operations
- Synchronous Write operation
- $\overline{\text{RESET}}$ pin invalidates all Tag entries
- Dual Chip selects for easy depth expansion with no performance degredation
- 3.3V power supply
- ZZ pin available to place device in low-power mode
- 48-pin Shrink Small Outline Package (SSOP)

DESCRIPTION:

The IDT71V218 is a 131,072-bit Cache Tag Static RAM, organized 8K x 16. There are fourteen common I/O TAG bits, with the remaining two bits used as status bits. A 14-bit comparator is on-chip to allow fast comparison of the fourteen stored TAG bits and the current Tag input data. An active HIGH MATCH output is generated when these two groups of data are the same for a given address. This high-speed MATCH signal is available as soon as 10ns after the address is presented to the TAG bit inputs.

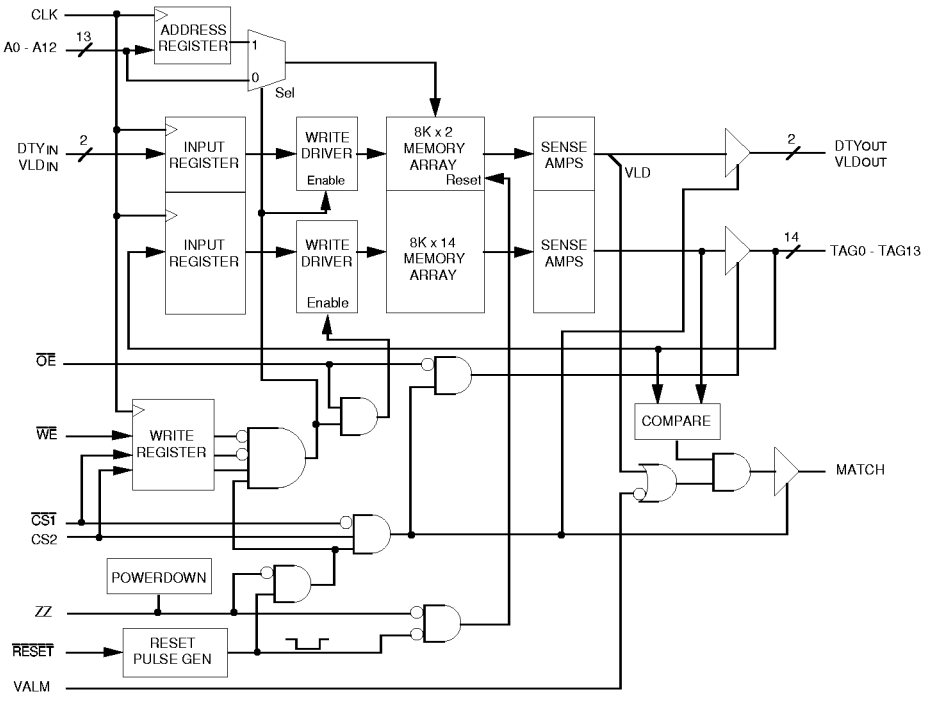
There are two separate I/O status bits, VLD and DTY. When the input pin VALM is HIGH, the VLD bit is used to internally qualify the MATCH output. If VALM is LOW, the VLD bit is not internally involved in the MATCH decision , but is available for use by outside system logic. The DTY bit is not used for internal decision making in the IDT71V218.

Match and Read operations are both asynchronous in order to provide the fastest access times possible, while Write operations are synchronous for ease of system timing. The asynchronous $\overline{\text{RESET}}$ pin, when held LOW, will reset all status bits in the array for easy invalidation of all Tag addresses.

The IDT71V218 is a full 3.3V device which uses a single 3.3V power supply to offer compliance with 3.3V LVTTL Logic levels. The ZZ pin offers a low-power Sleep mode to reduce power consumption and provide system power savings.

The IDT71V218 is fabricated using IDT's high-performance, high-reliability 3.3V CMOS technology and is offered in a space-saving 48-pin Shrink Small Outline Package (SSOP) package.

FUNCTIONAL BLOCK DIAGRAM



3196 drw 01

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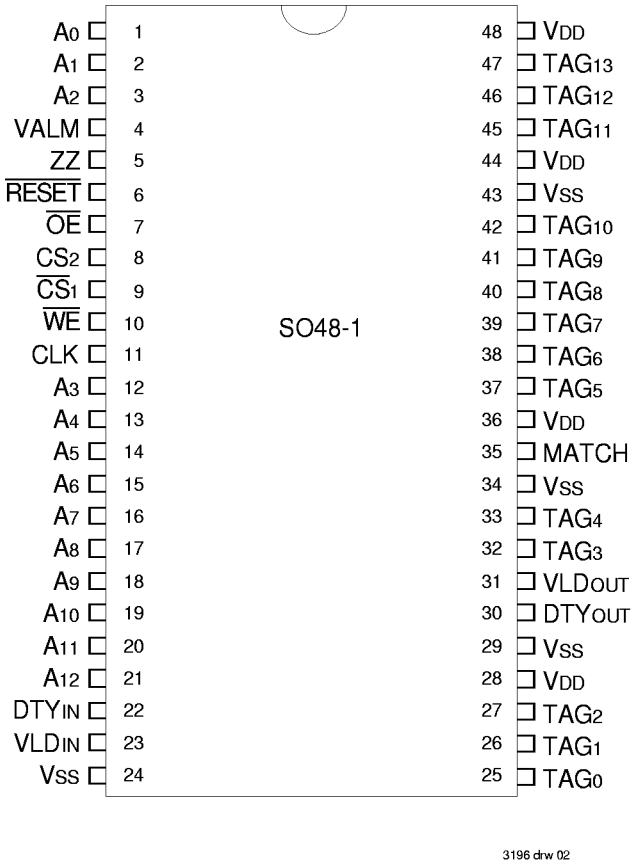
PIN DESCRIPTIONS

$A_0 - A_{12}$	Address Inputs	Input
$\overline{CS}_1$, CS_2	Chip Selects	Input
$\overline{WE}$	Write Enable	Input
$\overline{OE}$	Output Enable	Input
$\overline{RESET}$	Status Bit Reset	Input
ZZ	Sleep Mode Control Pin	Input
VLD_{IN}	Status Input Bit (Valid)	Input
DTY_{IN}	Status Input Bit (Dirty)	Input
VALM	Valid-included-with-Match	Input
CLK	System Clock	Input
$TAG_0 - TAG_{13}$	Tag Data Input/Outputs	I/O
VLD_{OUT}	Status Output Bit (Valid)	Output
DTY_{OUT}	Status Output Bit (Dirty)	Output
MATCH	Match	Output
V_{DD}	+3.3V Power (4 pins)	Pwr
V_{SS}	Ground (4 pins)	Gnd

3196 tbl 01

PIN CONFIGURATION



3196 drw 02

SSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{DD}+0.5	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTES: 3196 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{DD} and Input terminals only.
3. I/O terminals.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	3.135	3.3	3.465	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage - Inputs	2.0	—	5.0	V
V_{IH}	Input High Voltage - I/O	2.0	—	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	–0.3(1)	—	0.8	V

NOTE: 3196 tbl 03

1. V_{IL} (min.) = –1.5V for pulse width less than $t_{CYC}/2$, once per cycle.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	V_{DD}
Commercial	0°C to +70°C	0V	3.3V ± 5%

3196 tbl 04

CAPACITANCE

(T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 3dV	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	7	pF

NOTE: 3196 tbl 05

1. This parameter is determined by device characterization but is not production tested.

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3V ± 5%, T_A = 0 to 70°C)

Symbol	Parameter	Test Condition	IDT71V218 Min.	IDT71V218 Typ.	IDT71V218 Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{DD} = Max., V_{IN} = GND to V_{DD}	—	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{DD} = Max., $\overline{CS}_1$ = V_{IH}, V_{OUT} = GND to V_{DD}	—	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{DD} = Min.	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –8mA, V_{DD} = Min.	2.4	—	—	V

3196 tbl 06

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(1, 2) (V_{DD} = 3.3V ± 5%, T_A = 0 to 70°C)

Symbol	Parameter	Test Condition	71V218S10	71V218S12	71V218S15	Unit
I_{DD}	Operating Power Supply Current	ZZ ≤ V_{IL}, $\overline{CS}_1$ ≤ V_{IL}, CS_2 ≥ V_{IH}, $\overline{RESET}$ ≥ V_{IH} Outputs Open, V_{DD} = Max., f = f_{MAX}(3)	175	165	155	mA
I_{SB}	Standby Power Supply Current	ZZ ≥ V_{IH}, V_{IN} ≥ V_{IH} or ≤ V_{IL} V_{DD} = Max., f = f_{MAX}(3)	15	15	15	mA
I_{ZZ}	Full Sleep Mode Power Supply Current	ZZ ≥ V_{HD}, V_{IN} ≥ V_{HD} or ≤ V_{LD} V_{DD} = Max., f = 0(3)	5	5	5	mA

NOTES:

3196 tbl 07

1. All values are maximum guaranteed values.
2. V_{HD} = V_{DD} - 0.2V, V_{LD} = 0.2V
3. f_{MAX} =1/t_{CYC} (CLK cycling at f_{MAX}, address inputs cycling at 1/3 f_{MAX}). f = 0 means no input or I/O signals are switching.

FUNCTIONAL TRUTH TABLE(1)

MODE	TAG	VLD_{IN}	DTY_{IN}	VLD_{OUT}	DTY_{OUT}	$\overline{OE}$	$\overline{WE}$	$\overline{CS1}$	CS2	ZZ	$\overline{RESET}$	VALM	MATCH
Sleep	Hi-Z	X	X	Hi-Z	Hi-Z	X	X	X	X	H	X	X	Hi-Z
Reset	Hi-Z	X	X	Hi-Z	Hi-Z	X	H	X	X	L	L	X	Hi-Z
Deselect	Hi-Z	X	X	Hi-Z	Hi-Z	X	X	H	X	L	H	X	Hi-Z
Deselect	Hi-Z	X	X	Hi-Z	Hi-Z	X	X	X	L	L	H	X	Hi-Z
Read	OUT	X	X	OUT	OUT	L	H	L	H	L	H	X	U
Write	IN	IN	IN	VLD_{IN}	DTY_{IN}	H	L	L	H	L	H	X	U
Write Status Only	OUT	IN	IN	VLD_{IN}	DTY_{IN}	L	L	L	H	L	H	X	U
Match (see below)	IN	X	X	OUT	OUT	H	H	L	H	L	H	-	-

NOTES:

3196 tbl 09

1. "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care, Hi-Z = High Impedance, U = Output is driven, but level is undefined.

MATCH TRUTH TABLE(1, 2)

MODE	TAG (IN)	VALM	VLD_{OUT}	MATCH
Simple Match	= ADDRESSED DATA	L	X	H
Simple Mismatch	≠ ADDRESSED DATA	L	X	L
Invalid Entry	X	H	L	L
Match on Valid Entry	= ADDRESSED DATA	H	H	H
Mismatch on Valid Entry	≠ ADDRESSED DATA	H	H	L

NOTES:

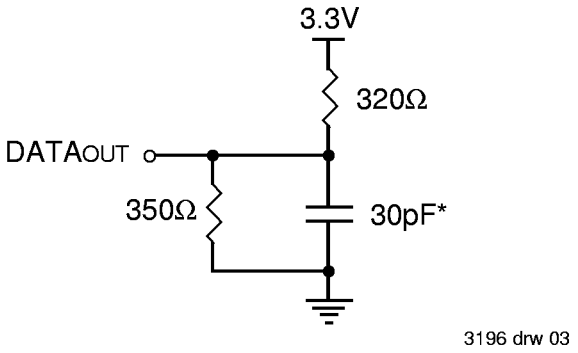
3196 tbl 10

1. $\overline{OE}$ = $\overline{WE}$ = CS2 = $\overline{RESET}$ = High. $\overline{CS1}$ = ZZ = Low
2. "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.

AC TEST CONDITIONS

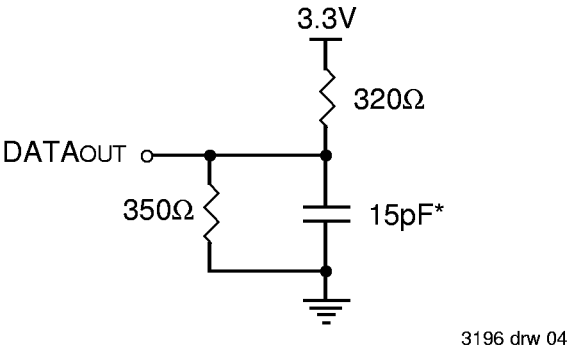
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1, 2, 3, and 4

3196 tbl 08



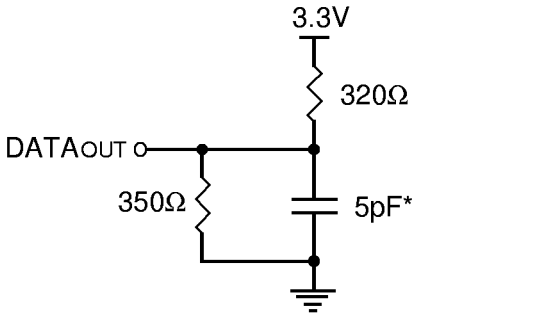
3196 drw 03

Figure 1. AC Test Load
TAG Outputs



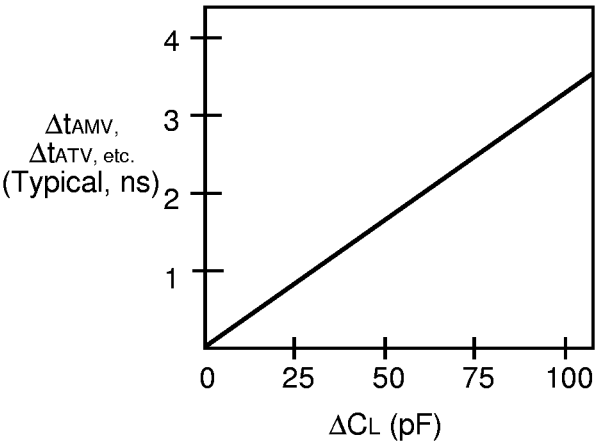
3196 drw 04

Figure 2. AC Test Load
MATCH, VLD and DTY Outputs



3196 drw 05

Figure 3. AC Test Load
(for t_{LZ} and t_{HZ} parameters)



3196 drw 06

Figure 4. Capactive Derating

*Includes scope and jig capacitances

AC ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3V ± 5%, T_A = 0 to 70°C)

Symbol	Parameter	IDT71V218S10		IDT71V218S12		IDT71V218S15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
MATCH Cycle								
t_{AMV}	Address to MATCH Valid	—	10	—	12	—	15	ns
t_{TMV}	Tag Input to MATCH Valid	—	10	—	12	—	15	ns
t_{CMV}	Chip Enable to MATCH Valid	—	10	—	12	—	15	ns
t_{CMLZ}(1)	Chip Enable to MATCH in Low-Z	2	—	2	—	2	—	ns
t_{CMHZ}(1)	Chip Enable to MATCH in High-Z	0	6	0	6	0	7	ns
t_{AMH}	MATCH Valid Hold from Address Change	2	—	2	—	2	—	ns
t_{TMH}	MATCH Valid Hold from Tag Input Change	2	—	2	—	2	—	ns

NOTE:
1. This parameter is guaranteed with the AC Load (Figure 3) by device characterization, but is not production tested.

3196 tbl 11

AC ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3V ± 5%, T_A = 0 to 70°C)

Symbol	Parameter	IDT71V218S10		IDT71V218S12		IDT71V218S15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{ATV}	Address to Tag Valid	—	13	—	15	—	17	ns
t_{CTV}	Chip Enable to Tag Valid	—	11	—	13	—	15	ns
t_{CLZ}(1)	Chip Enable to Tag and Status Bits in Low-Z	2	—	2	—	2	—	ns
t_{CHZ}(1)	Chip Enable to Tag and Status Bits in High-Z	0	6	0	6	0	7	ns
t_{OE}	Output Enable to Tag Bits Valid	—	6	—	7	—	7	ns
t_{OLZ}(1)	Output Enable to Tag Bits in Low-Z	0	—	0	—	0	—	ns
t_{OHZ}(1)	Output Enable to Tag Bits in High-Z	0	6	0	6	0	7	ns
t_{ATH}	Tag Bit Hold from Address Change	2	—	2	—	2	—	ns
t_{ASV}	Address to Status Valid	—	10	—	12	—	15	ns
t_{CSV}	Chip Enable to Status Valid	—	10	—	12	—	15	ns
t_{ASH}	Status Bit Hold from Address Change	2	—	2	—	2	—	ns

NOTE:
1. This parameter is guaranteed with the AC Load (Figure 3) by device characterization, but is not production tested.

3196 tbl 12

AC ELECTRICAL CHARACTERISTICS (1)

(V_{DD} = 3.3V ± 5%, T_A = 0 to 70°C)

Symbol	Parameter	IDT71V218S10		IDT71V218S12		IDT71V218S15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle and Clock Parameters								
t_S	$\overline{WE}$, Chip Enable, and Input Data Set-up Time	3	—	3	—	3	—	ns
t_H	$\overline{WE}$, Chip Enable, and Input Data Hold Time	1	—	1	—	1	—	ns
t_{SA}	Address Set-up Time (Write Cycle Only)	3	—	3	—	3	—	ns
t_{HA}	Address Hold Time (Write Cycle Only)	1	—	1	—	1	—	ns
t_{KMH}	CLK HIGH Write to MATCH Invalid	0	—	0	—	0	—	ns
t_{KRTV}(3)	CLK HIGH Read to Tag Bits Valid	—	12	—	14	—	16	ns
t_{KWSV}(3)	CLK HIGH Write to Status Outputs Valid	—	12	—	14	—	16	ns
t_{KRSV}(3)	CLK HIGH Read to Status Outputs Valid	—	12	—	14	—	16	ns
t_{KSH}(2)	Status Output Hold from CLK HIGH (Write Cycle)	2	—	2	—	2	—	ns
t_{OW}	$\overline{OE}$ HIGH before Write	10	—	10	—	12	—	ns
t_{WO}	End of Write to $\overline{OE}$ Asserted	5	—	5	—	6	—	ns

NOTES:
1. All Write cycles are synchronous and referenced from rising CLK.
2. This parameter is guaranteed by device characterization, but is not production tested.
3. Addresses are stable prior to CLK transition HIGH.

3196 tbl 13

AC ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3V ± 5%, T_A = 0 to 70°C)

Symbol	Parameter	IDT71V218S10 Min.	IDT71V218S10 Max.	IDT71V218S12 Min.	IDT71V218S12 Max.	IDT71V218S15 Min.	IDT71V218S15 Max.	Unit
Reset Cycle								
t_{RP}	$\overline{RESET}$ Pulse Width	20	—	25	—	30	—	ns
t_{RTV}	$\overline{RESET}$ HIGH to Tag Valid	—	60	—	60	—	60	ns
t_{RTLZ}[1]	$\overline{RESET}$ HIGH to Tag Low-Z	0	50	0	50	0	50	ns
t_{RTHZ}[1]	$\overline{RESET}$ LOW to Tag High-Z	—	8	—	8	—	9	ns
t_{RSV}	$\overline{RESET}$ HIGH to Status Valid	—	60	—	60	—	60	ns
t_{RSLZ}[1]	$\overline{RESET}$ HIGH to Status Low-Z	0	50	0	50	0	50	ns
t_{RSHZ}[1]	$\overline{RESET}$ LOW to Status High-Z	—	8	—	8	—	8	ns
t_{RMV}[1]	$\overline{RESET}$ HIGH to MATCH Valid	—	60	—	60	—	60	ns
t_{RMLZ}[1]	$\overline{RESET}$ HIGH to MATCH Low-Z	0	50	0	50	0	50	ns
t_{RMHZ}[1]	$\overline{RESET}$ LOW to MATCH High-Z	—	8	—	8	—	8	ns
t_{RW}	$\overline{RESET}$ HIGH before Write	50	—	50	—	50	—	ns
t_{WR}	End of Write to $\overline{RESET}$ LOW	5	—	5	—	5	—	ns

NOTE:
1. This parameter is guaranteed with the AC Load (Figure 3) by device characterization, but is not production tested.

3196 tbl 13

AC ELECTRICAL CHARACTERISTICS [1]

(V_{DD} = 3.3V ± 5%, T_A = 0 to 70°C)

Symbol	Parameter	IDT71V218S10 Min.	IDT71V218S10 Max.	IDT71V218S12 Min.	IDT71V218S12 Max.	IDT71V218S15 Min.	IDT71V218S15 Max.	Unit
Sleep Cycle								
t_{ZTV}	ZZ LOW to Tag Valid	—	30	—	30	—	30	ns
t_{ZTLZ}[2]	ZZ LOW to Tag Low-Z	0	—	0	—	0	—	ns
t_{ZTHZ}[2]	ZZ HIGH to Tag High-Z	—	8	—	9	—	10	ns
t_{ZSV}	ZZ LOW to Status Valid	—	30	—	30	—	30	ns
t_{ZSLZ}[2]	ZZ LOW to Status Low-Z	0	—	0	—	0	—	ns
t_{ZSHZ}[2]	ZZ HIGH to Status High-Z	—	8	—	9	—	10	ns
t_{ZMV}	ZZ LOW to MATCH Valid	—	30	—	30	—	30	ns
t_{ZMLZ}[2]	ZZ LOW to MATCH Low-Z	0	—	0	—	0	—	ns
t_{ZMHZ}[2]	ZZ HIGH to MATCH High-Z	—	8	—	9	—	10	ns
t_{ZW}	ZZ LOW before Write	20	—	20	—	20	—	ns
t_{WZ}	End of Write to ZZ HIGH	5	—	5	—	5	—	ns
t_{ZSR}	ZZ LOW before $\overline{RESET}$ LOW	15	—	15	—	15	—	ns
t_{RZ}	End of Reset to ZZ HIGH	50	—	50	—	50	—	ns
t_{RZH}	$\overline{RESET}$ Hold from ZZ HIGH	10	—	10	—	10	—	ns

NOTES:
1. Sleep mode is intended to be used during extended time periods of device inactivity.
2. This parameter is guaranteed with the AC Load (Figure 3) by device characterization, but is not production tested.

3196 tbl 14

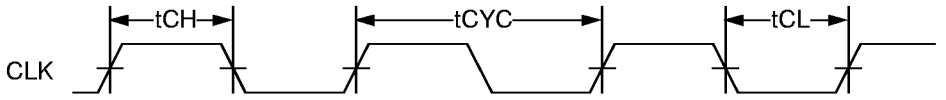
AC ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3V ± 5%, T_A = 0 to 70°C)

Symbol	Parameter	IDT71V218S10 Min.	IDT71V218S10 Max.	IDT71V218S12 Min.	IDT71V218S12 Max.	IDT71V218S15 Min.	IDT71V218S15 Max.	Unit
Clock Timing								
t_{CYC}	Clock Cycle Time	15	—	15	—	16.6	—	ns
t_{CH}	Clock HIGH Time	5	—	5	—	5	—	ns
t_{CL}	Clock LOW Time	5	—	5	—	5	—	ns

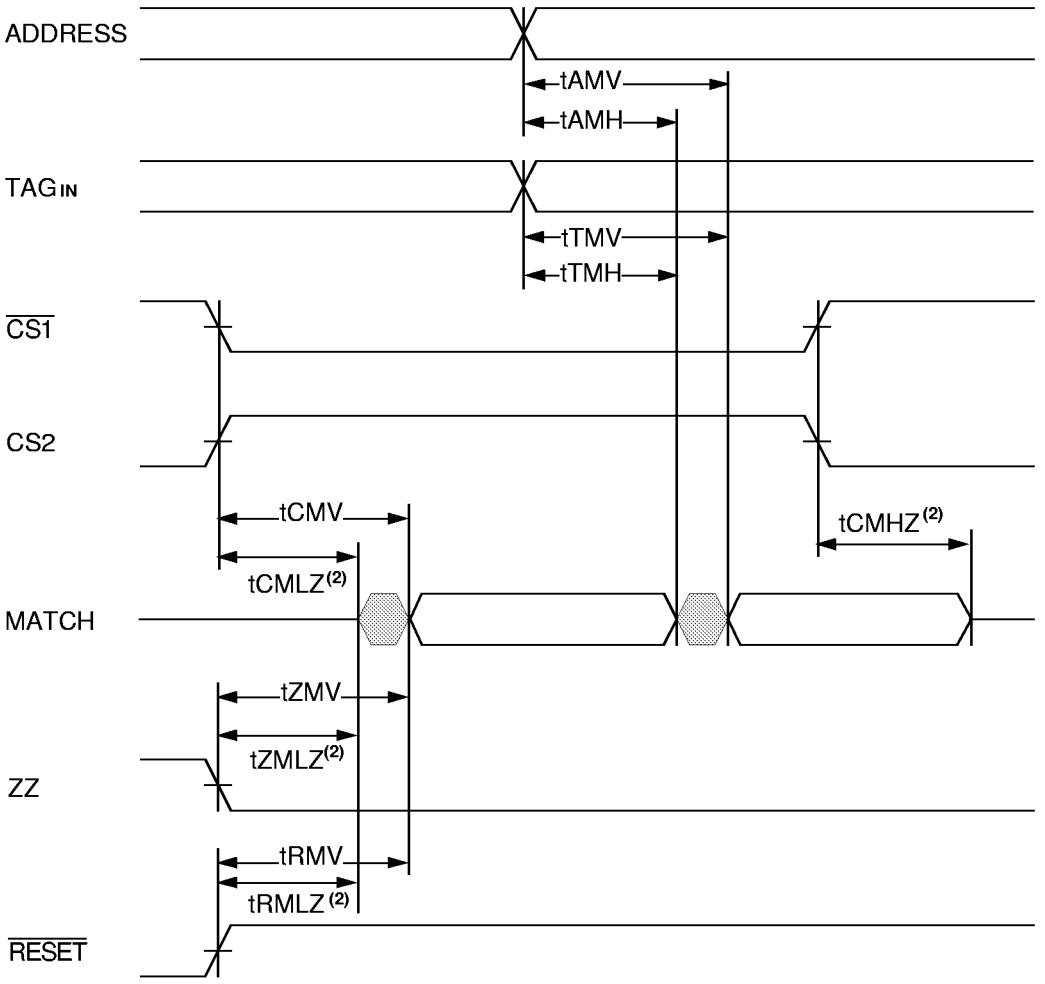
3196 tbl 15

SYSTEM CLOCK TIMING WAVEFORM



3196 drw 07

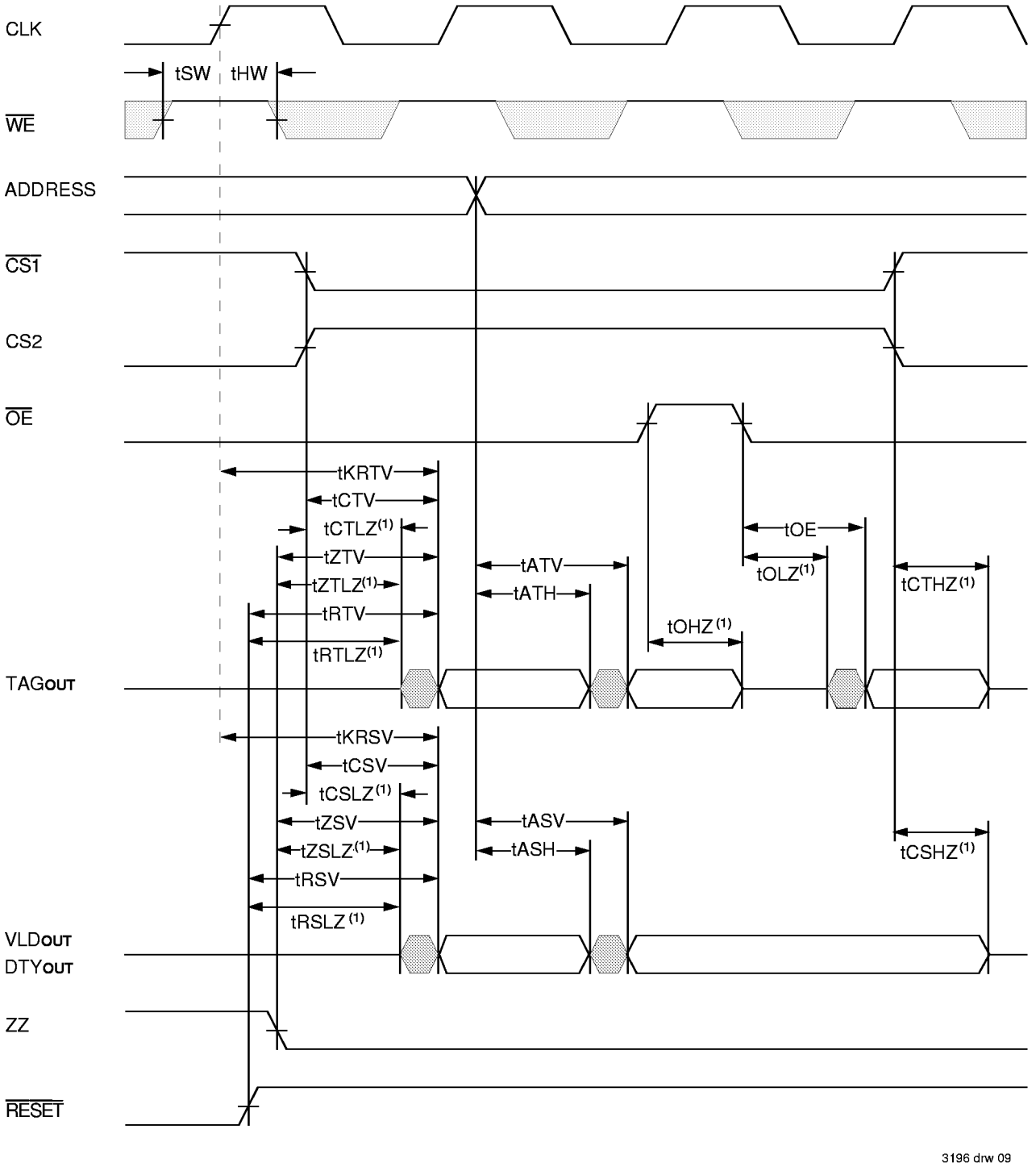
TIMING WAVEFORMS OF MATCH CYCLE(1)



3196 drw 08

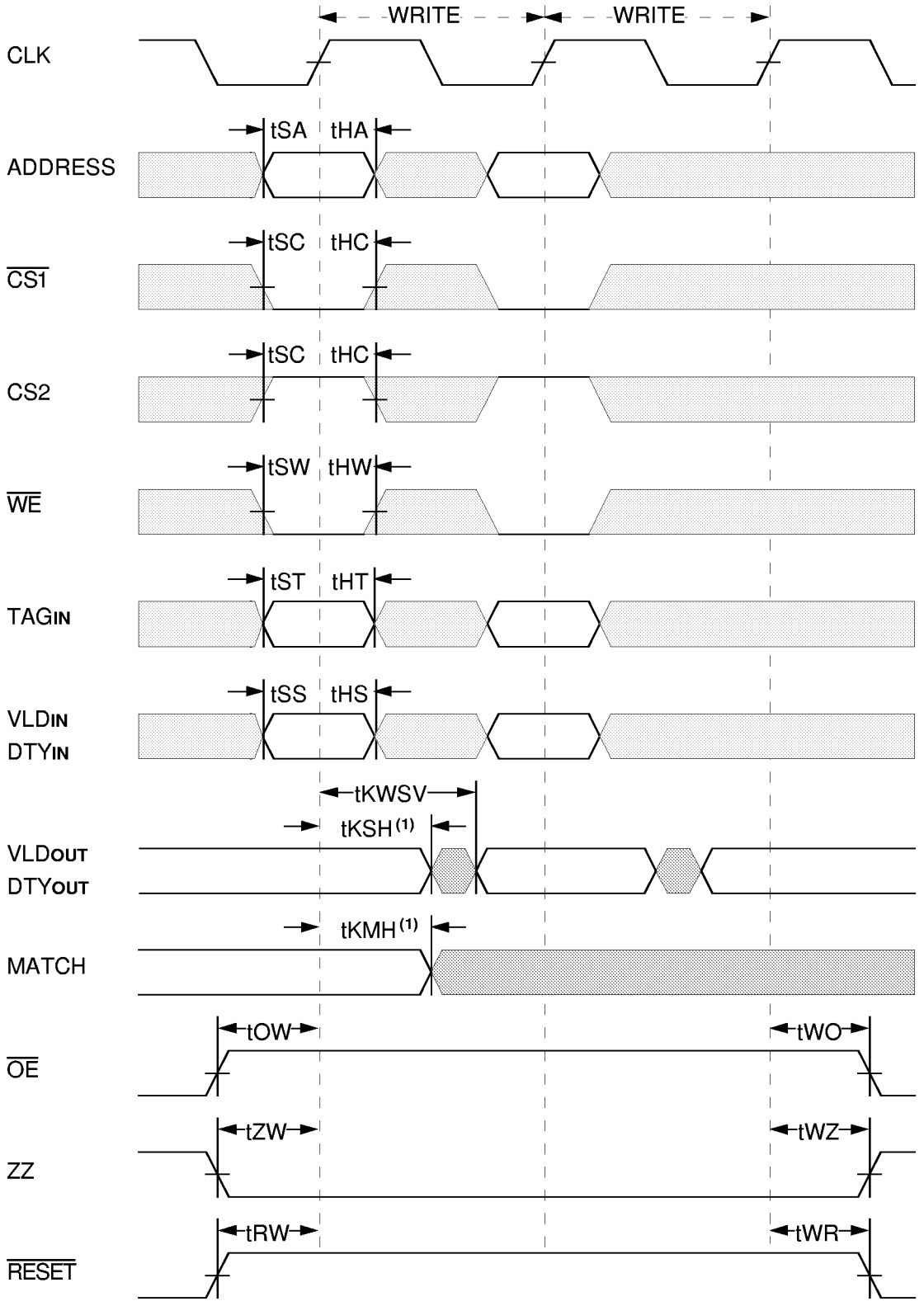
NOTES:
1. $\overline{OE}$ is HIGH.
2. Transition is measured ±200mV from steady state.

TIMING WAVEFORMS OF READ CYCLE



NOTE:
1. Transition is measured ±200mV from steady state.

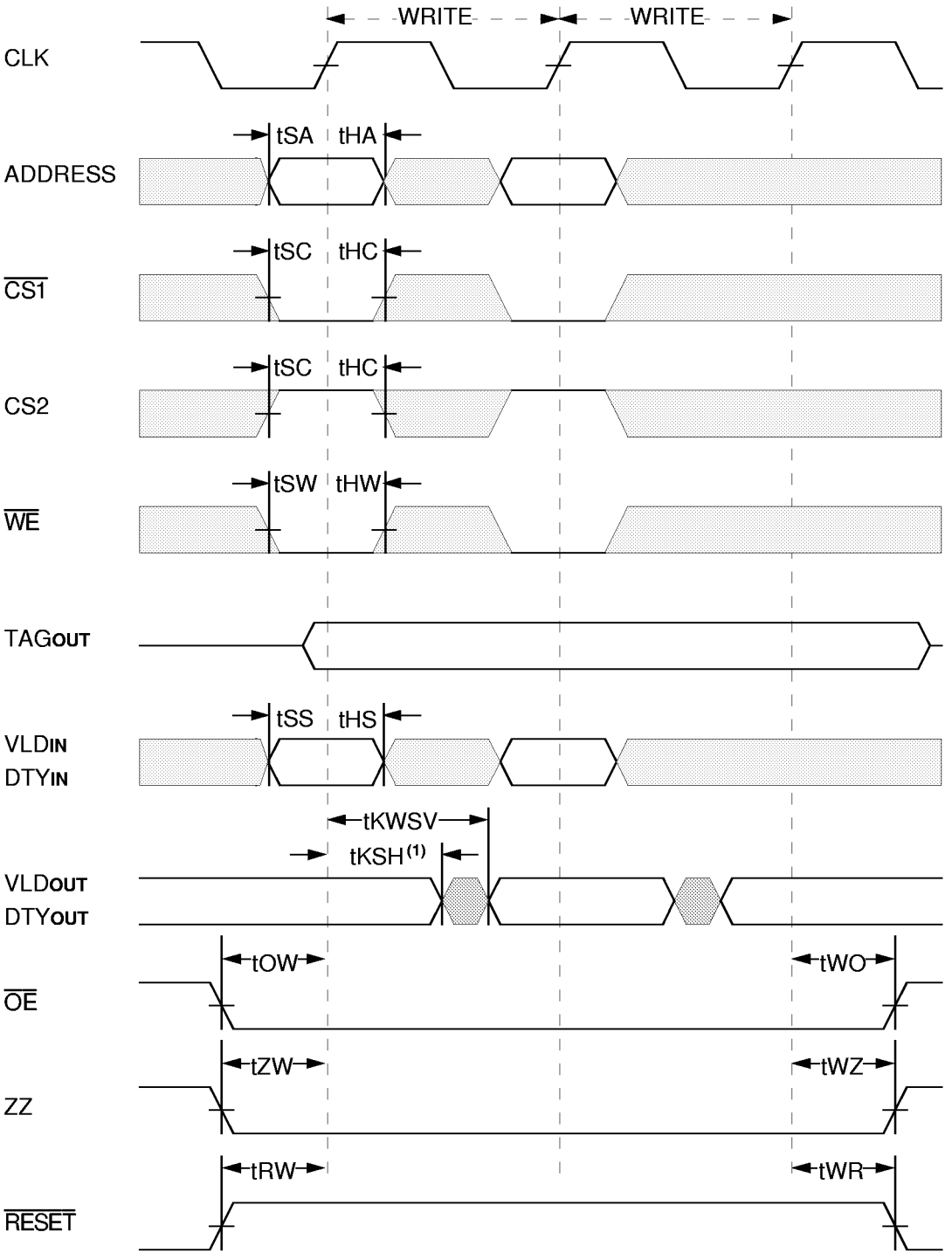
TIMING WAVEFORMS OF WRITE CYCLE ($\overline{OE}$ HIGH)



NOTE:
1. tKSH and tKMH apply only if these outputs are already valid prior to the referenced CLK.

3196 drw 10

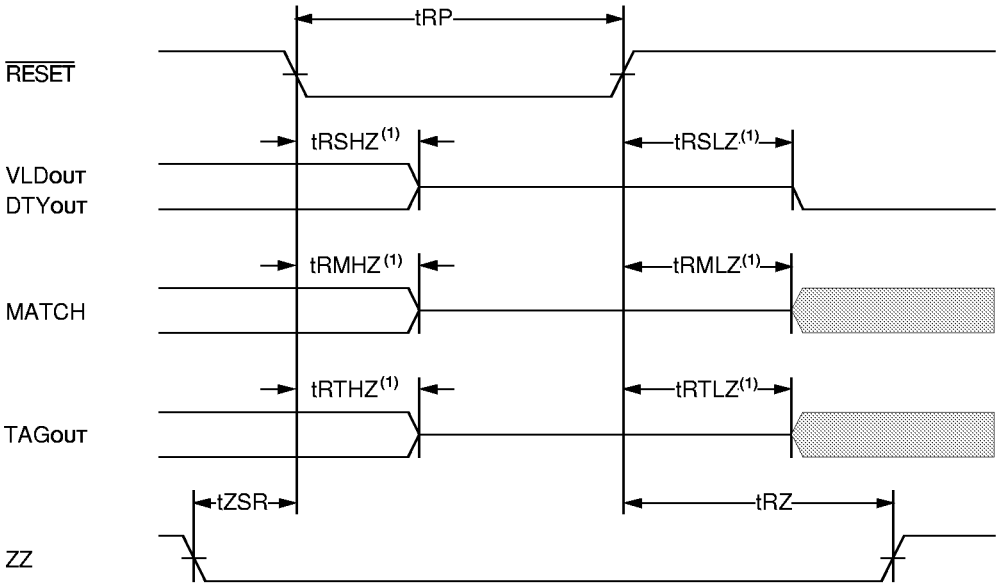
TIMING WAVEFORMS OF WRITE CYCLE ($\overline{OE}$ LOW)



3196 drw 11

NOTE:
1. tKSH apply only if these outputs are already valid prior to the referenced CLK.

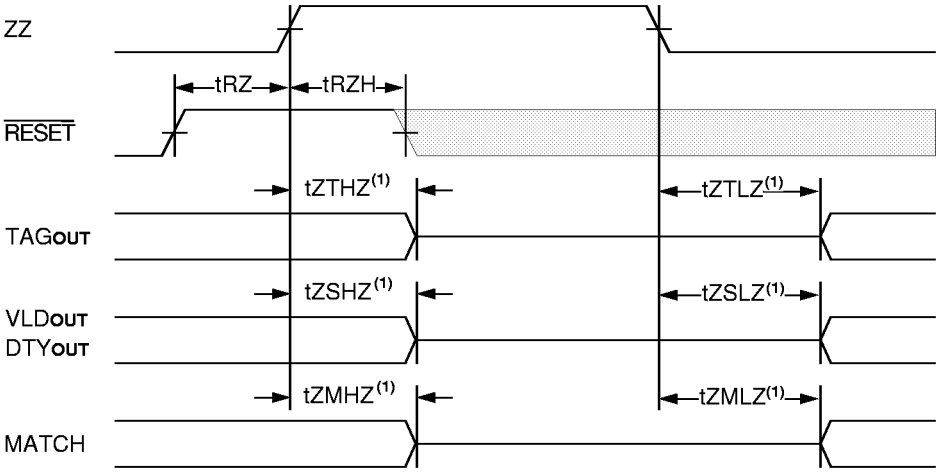
TIMING WAVEFORMS OF RESET FUNCTION



NOTE:
1. Transition is measured ±200mV from steady state.

3196 drw 12

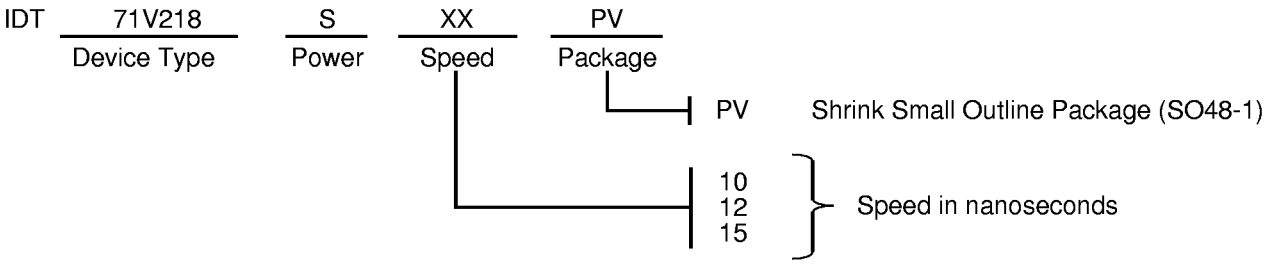
TIMING WAVEFORMS OF SLEEP MODE FUNCTIONALITY



NOTE:
1. Transition is measured ±200mV from steady state.

3196 drw 13

ORDERING INFORMATION



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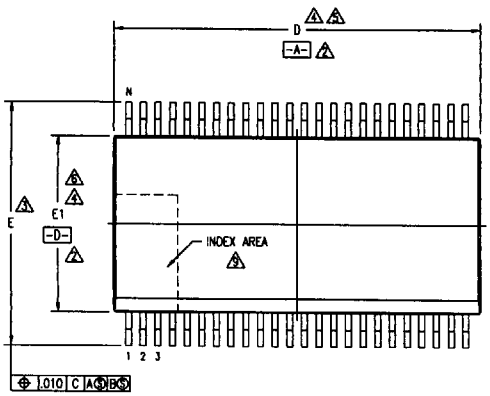
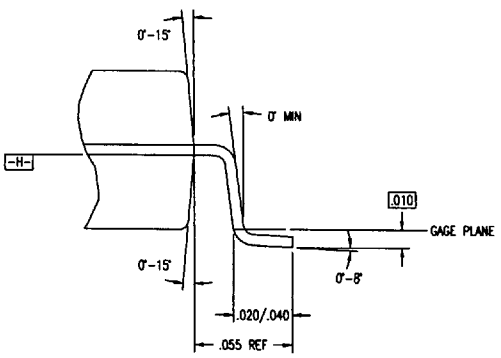
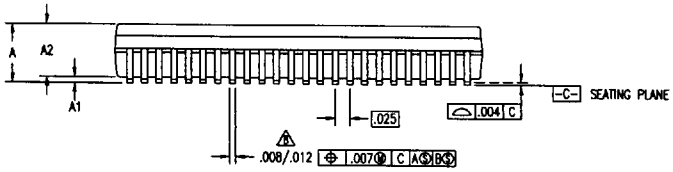
SSOP

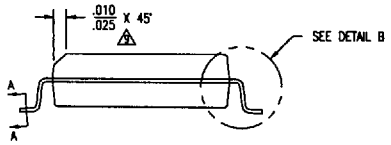
REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
17893	00	INITIAL RELEASE	07/15/90	A. FUNCELL
22377	01	REMOVE CHAMFER FROM PACKAGE	04/15/92	T. VU
27492	02	REDRAW TO JEDEC FORMAT	02/01/95	

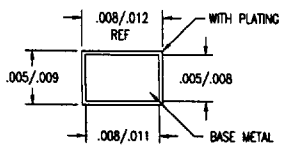




DETAIL B







SECTION A-A

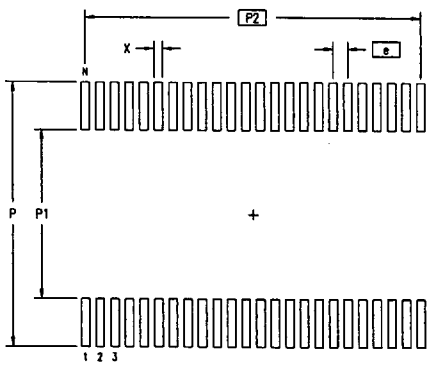
TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070	
DECIMAL XX± XXX± XXXX±	ANGULAR ±		
APPROVALS	DATE	TITLE PV PACKAGE OUTLINE .300" BODY WIDTH SSOP .025" PITCH	
DRAWN AA	08/15/90		
CHECKED		SIZE C	DRAWING No. PSC-4029 REV 02
		DO NOT SCALE DRAWING	

SSOP (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
17893	00	INITIAL RELEASE	07/15/90	A. FUNCELL
22377	01	REMOVE CHAMFER FROM PACKAGE	04/15/92	T. VU
27492	02	REDRAW TO JEDEC FORMAT	02/01/95	

DWG #		S048-1			DWG #		S056-1		
SYMBOL	JEDEC VARIATION AA			NOTE	JEDEC VARIATION AB			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX	
A	.095	.102	.110		.095	.102	.110	
A1	.008	.012	.016		.008	.012	.016	
A2	.088	.090	.092		.088	.090	.092	
D	.620	.625	.630	4,5	.720	.725	.730	4,5
E	.395	.405	.420	3	.395	.405	.420	3
E1	.291	.295	.299	4,6	.291	.295	.299	4,6
N	48				56			

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX
P	.450	.458	.450	.458
P1	.282	.290	.282	.290
P2	.575 BSC		.675 BSC	
X	.010	.018	.010	.018
e	.025 BSC		.025 BSC	
N	48		56	

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982

2 DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-

3 DIMENSION E TO BE DETERMINED AT SEATING PLANE -C-

4 DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-

5 DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE

6 DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .015 PER SIDE

7 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND .010 FROM LEAD TIP

8 LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .004 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT

9 THE CHAMFER ON THE PACKAGE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE ZONE INDICATED

10 ALL DIMENSIONS ARE IN INCHES

11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-118, VARATION AA & AB

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc.
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APPROVALS	DATE	TITLE PV PACKAGE OUTLINE .300" BODY WIDTH SSOP .025" PITCH
DRAWN AA	05/15/90	
CHECKED		SIZE C DRAWING No. PSC-4029 REV 02
		DO NOT SCALE DRAWING