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PRODUCT OVERVIEW

KS88-SERIES MICROCONTROLLERS

Samsung's KS88 series of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU, a wide range of integrated peripherals, and various mask-programmable ROM sizes. Important CPU features include:

- Efficient register-oriented architecture
- Selectable CPU clock sources
- Idle and Stop power-down mode release by interrupt
- Built-in basic timer with watchdog function

A sophisticated interrupt structure recognizes up to eight interrupt levels. Each level can have one or more interrupt sources and vectors. Fast interrupt processing (within a minimum six CPU clocks) can be assigned to specific interrupt levels.

KS88C2064 MICROCONTROLLER

The KS88C2064 single-chip CMOS microcontroller is fabricated using a highly advanced CMOS process and is based on Samsung's newest CPU architecture.

The KS88C2064 is the microcontroller which has 64-Kbyte mask-programmable ROM and 192-Kbyte mask ROM for font data.

Using a proven modular design approach, Samsung engineers developed the KS88C2064 by integrating the following peripheral modules with the powerful SAM87 core:

- Four programmable I/O ports, excluding one BUZ pin, for a total of 32 pins.
- Eight bit-programmable pins for external interrupts.
- One 8-bit basic timer for oscillation stabilization and watchdog functions (system reset).
- One 8-bit timer/counter and one 16-bit timer/counter with selectable operating modes.
- Watch timer for real time.

The KS88C2064 is a versatile microcontroller for data bank or dictionary. It is currently available in a 128-pin QFP package.

FEATURES

CPU

- SAM87 CPU core

Memory

- 64-Kbyte internal program memory (ROM)
- 192-Kbyte internal memory (ROM) for font data
- 272-byte internal register file (Excluding LCD RAM)
- 6144-byte data RAM

Instruction Set

- 78 instructions
- IDLE and STOP instructions added for power-down modes

Instruction Execution Time

- 1.5 μ s at 4 MHz fx (minimum)
- 183 μ s at 32,768 Hz fxt

Interrupts

- Five interrupt levels and 15 interrupt sources
- 15 vectors (15 sources have a dedicated vector address)
- Fast interrupt processing feature (for one selected interrupt level)

I/O Ports

- Four 8-bit I/O ports (P0–P3) for a total of 32-bit programmable pins
- Eight input pins for external interrupts
- One output only pin for BUZ

Watch Timer

- Interval time: 3.91 ms, 1s at 32,768 Hz
- Four frequency outputs to BUZ pin and BUZ pin
- Clock source generation for LCD

LCD Controller/Driver

- 65 segments and 18 common terminals
- Internal resistor circuit for LCD bias
- Voltage doubler
- All dot can be switched on/off

Timers and Timer/Counters

- One programmable 8-bit basic timer (BT) for oscillation stabilization control or watchdog timer (software reset) function
- One 8-bit timer/counter (Timer 0) with three operating modes; Interval, Capture and PWM
- One 16-bit timer/counter (Timer 1) with two 8-bit timer/counter modes; Interval

Power-Down Modes

- Idle mode (CPU clock stops)
- Stop mode (main oscillation and CPU clock stops)

Operating Temperature Range

- – 40 °C to + 85 °C

Operating Voltage Range

- 2.2 V to 4.5 V at 1 MHz fx
- 2.7 V to 4.5 V at 4 MHz fx

Package Type

- 128-pin QFP

BLOCK DIAGRAM

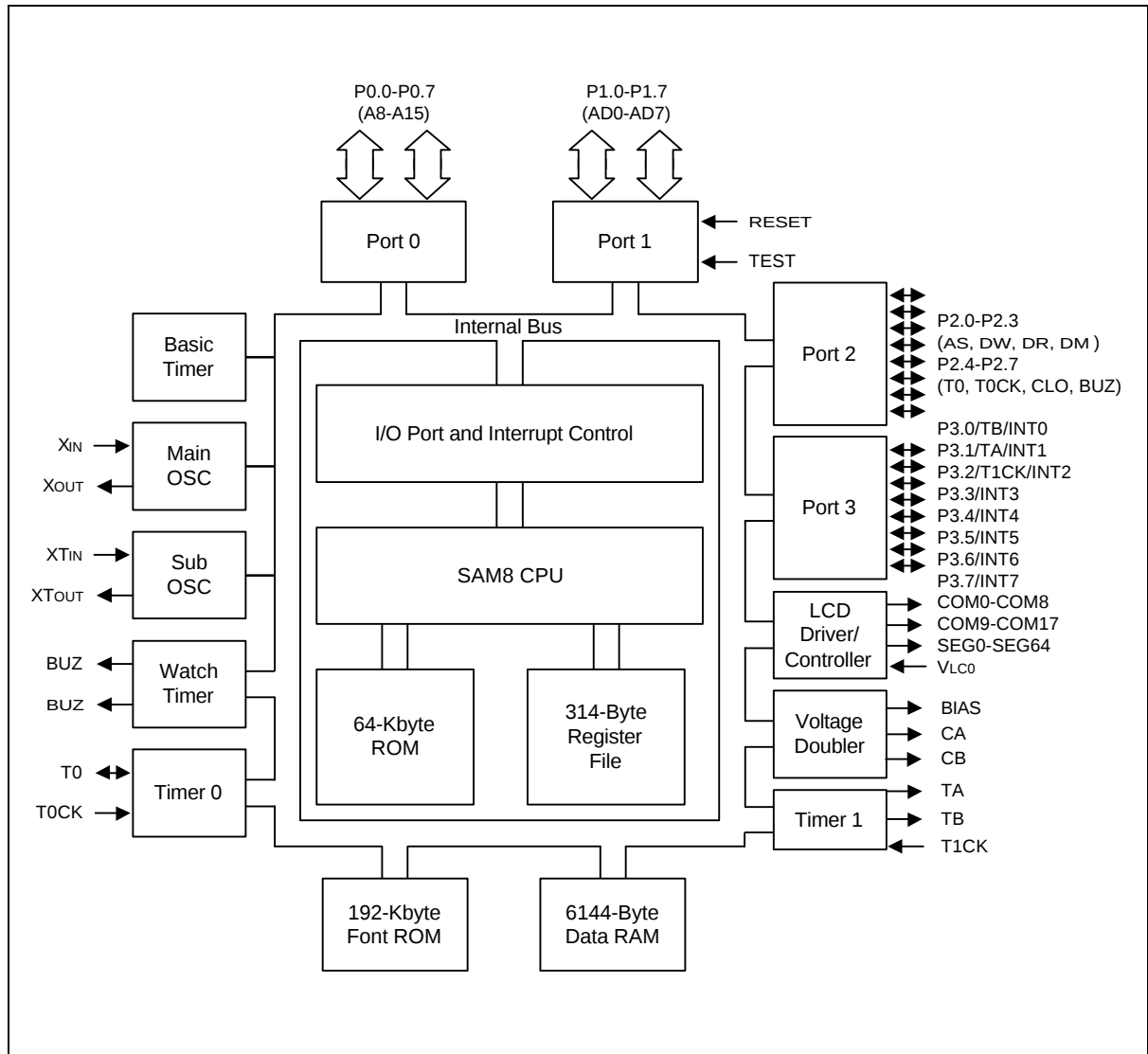


Figure 1-1. Block Diagram

PIN ASSIGNMENTS

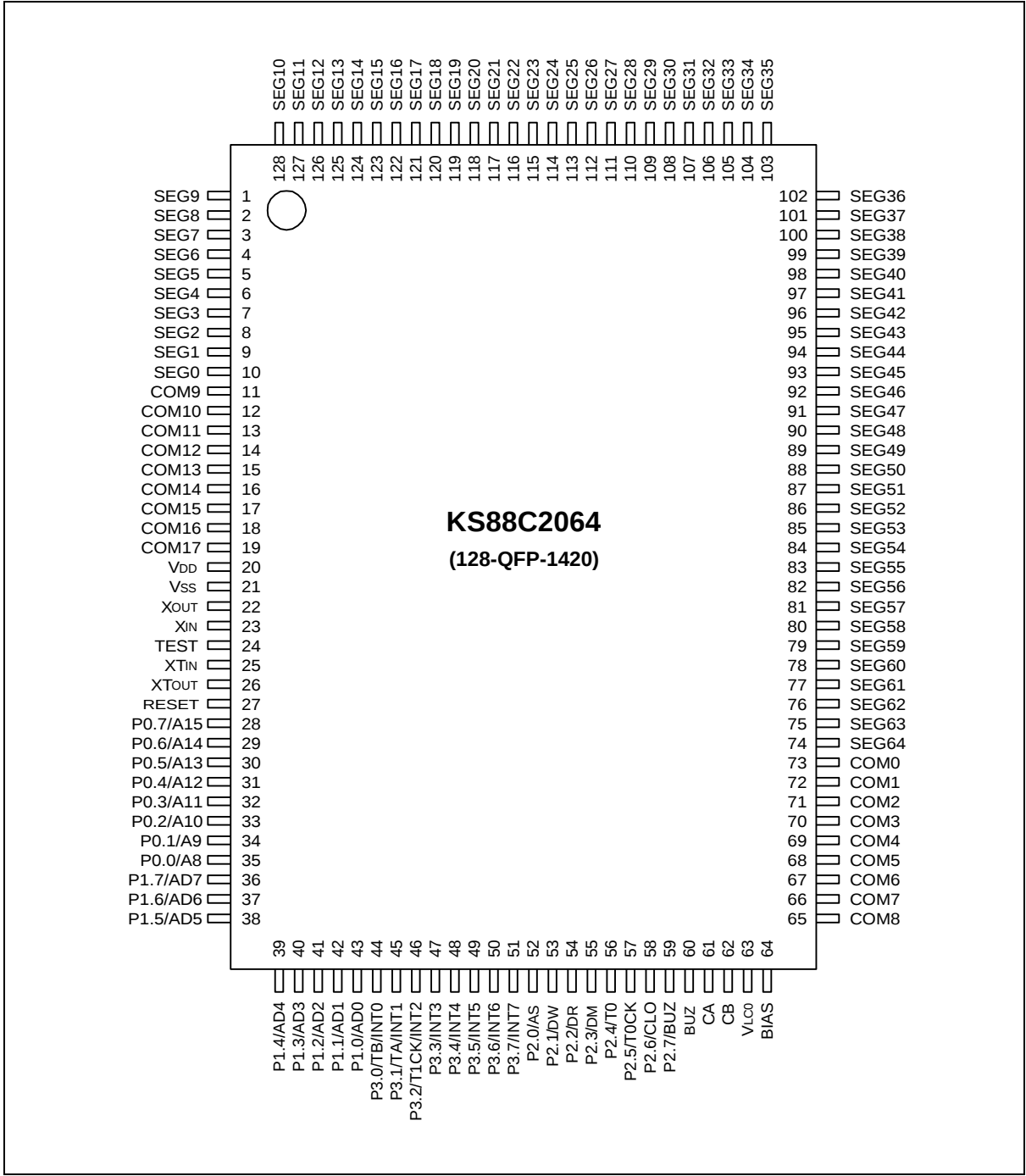


Figure 1-2. Pin Assignment (128-Pin QFP Package)

PIN DESCRIPTIONS

Table 1-1. Pin Descriptions

Pin Names	Pin Type	Pin Description	Circuit Type	Pin No.	Shared Functions
P0.0–P0.7	I/O	I/O port with nibble-programmable pins; schmitt trigger input or push-pull, open-drain output and software assignable pull-up; also configurable as external interface address lines A8–A15.	3	35–38	A8–A15
P1.0–P1.7	I/O	Same general characteristics as port 0; also configurable as external interface address/data lines AD0–AD7.	3	43–50	AD0–AD7
P2.0–P2.3	I/O	I/O port with bit-programmable pins; schmitt trigger input or push-pull output and software assignable pull-ups. Lower nibble pins 0–3 are configurable for external interface signals.	5	52–55	AS, DW, DR, DM
P2.4–P2.7	I/O	P2.4/capture input, interval/PWM output (T0) P2.5/timer 0 clock input (T0CK) P2.6/system clock output (CLO) P2.7/buzzer signal output (BUZ)	6	56–59	T0, T0CK, CLO, BUZ
P3.0–P3.7	I/O	I/O port with bit-programmable pins; schmitt trigger input or push-pull output and software assignable pull-up; P3.0–P3.7 are alternately used for external interrupt input (noise filters, interrupt enable and pending control); P3.0/timer B clock output (TB)/INT0 P3.1/timer 1/A clock output (TA)/INT1 P3.2/timer 1/A clock input (T1CK)/INT2	4	44–51	TB/INT0, TA/INT1, T1CK/INT2, INT3–INT7
T1CK	I/O	Timer A external clock input pins.	4	46	P3.2/INT2
TB TA	I/O	Timer B and 1/A clock output pins.	4	44 45	P3.0/INT0 P3.1/INT1
AS, DW, DR, DM	I/O	Output pins for external interface control signals. AS: address strobe DW: data memory write DR: data memory read DM: data memory select	5	52–55	P2.0–P2.3
T0	I/O	Capture input or interval/PWM output.	6	56	P2.4
T0CK	I/O	Timer 0 clock input.	6	57	P2.5

Table 1-1. Pin Descriptions (Continued)

Pin Names	Pin Type	Pin Description	Circuit Type	Pin No.	Shared Functions
CLO	I/O	Clock output	6	58	P2.6
BUZ	I/O	Output pin for buzzer signal.	6	59	P2.7
BUZ	O	Inverted buzzer signal output.	—	60	—
INT0–INT7	I/O	External interrupt input pins.	4	44–51	P3.0/TB, P3.1/TA, P3.2/T1CK, P3.3–P3.7
AD0–AD7	I/O	Address low and data ports.	3	43–36	P1.0–P1.7
A8–A15	I/O	Address high output ports.	3	35–28	P0.0–P0.7
COM0–COM8	O	LCD common signal output.	7	73–65	—
COM9–COM17	O	LCD common signal output.	7	11–19	—
SEG0–SEG64	O	LCD seg signal output.	8	10–1 128–74	—
CA, CB	—	Capacitor terminal for voltage doubling.	—	61, 62	—
V _{LC0}	—	LCD power supply.	—	63	—
BIAS	O	Bias voltage level for LCD driving.	—	64	—
RESET	I	System reset pin	2	27	—
XT _{IN} , XT _{OUT}	—	Crystal oscillator pins for sub clock.	—	25, 26	—
TEST	I	Test signal input (must be connected to V _{DD}).	—	24	—
X _{IN} , X _{OUT}	—	Main oscillator pins	—	23, 22	—
V _{DD} , V _{SS}	—	Power input pins	—	20, 21	—

PIN CIRCUIT DIAGRAMS

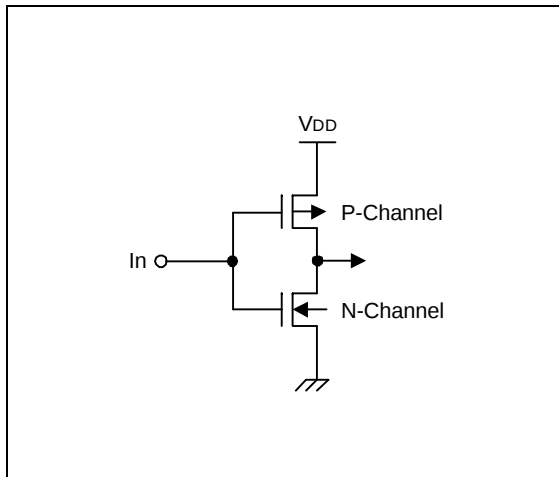


Figure 1-3. Pin Circuit Type 1

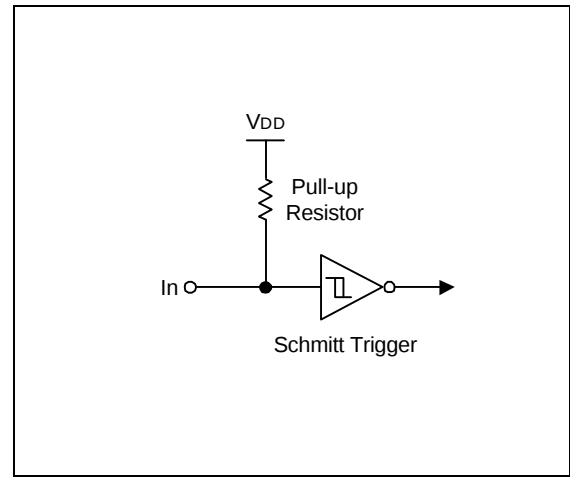


Figure 1-4. Pin Circuit Type 2 (RESET)

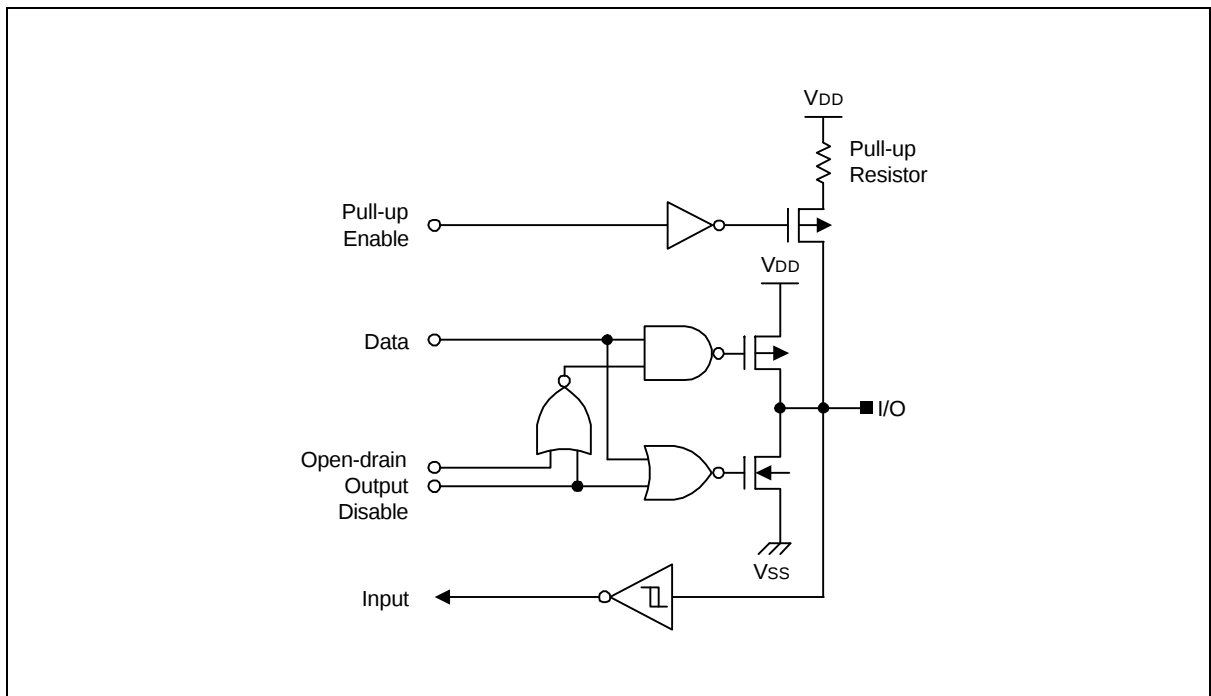


Figure 1-5. Pin Circuit Type 3 (Ports 0, 1)

PIN CIRCUIT DIAGRAMS (Continued)

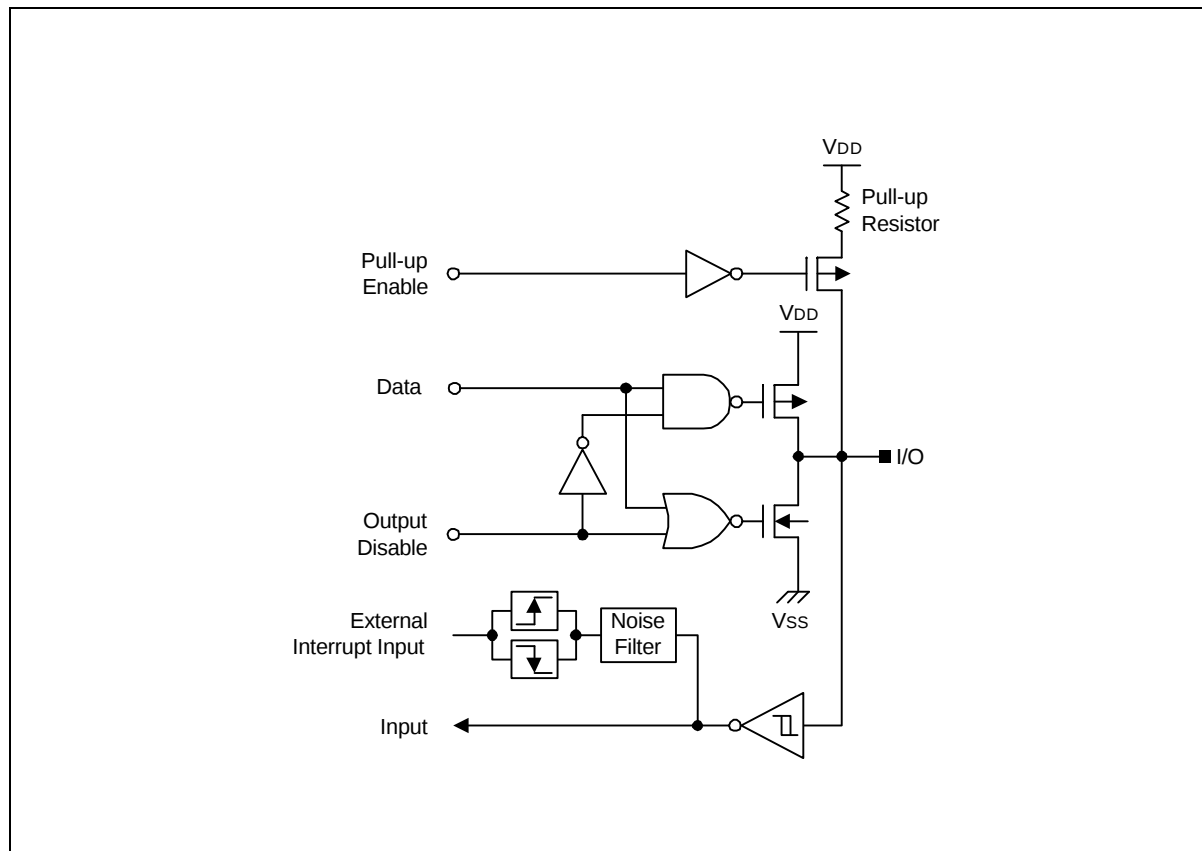


Figure 1-6. Pin Circuit Type 4 (Port 3)

PIN CIRCUIT DIAGRAMS (Continued)

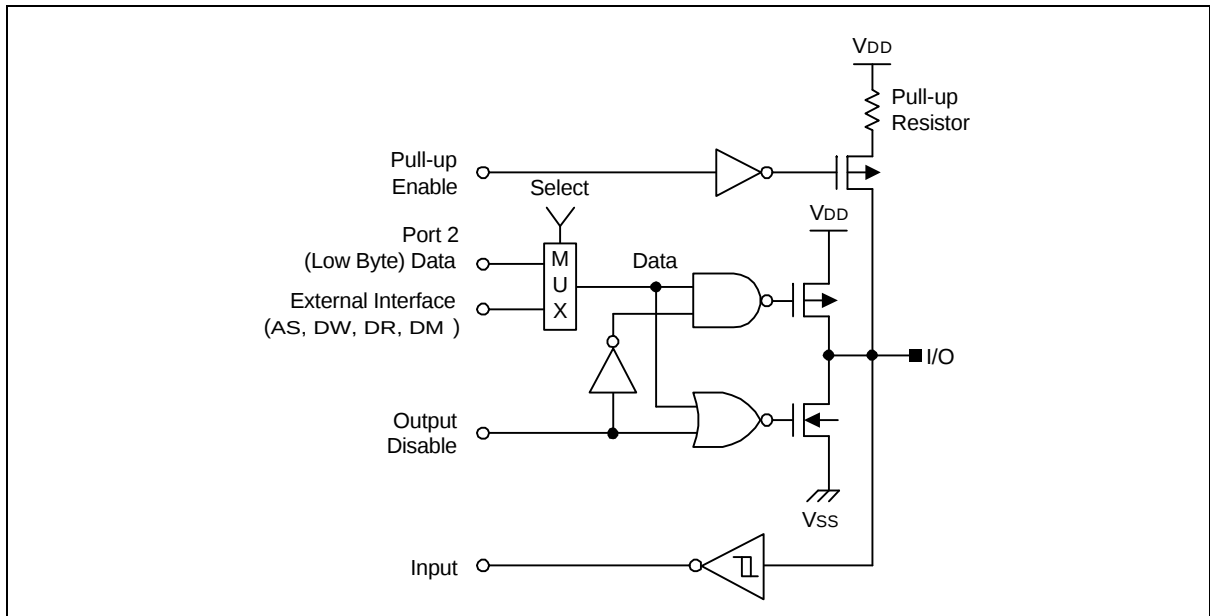


Figure 1-7. Pin Circuit Type 5 (Ports 2.0-2.3)

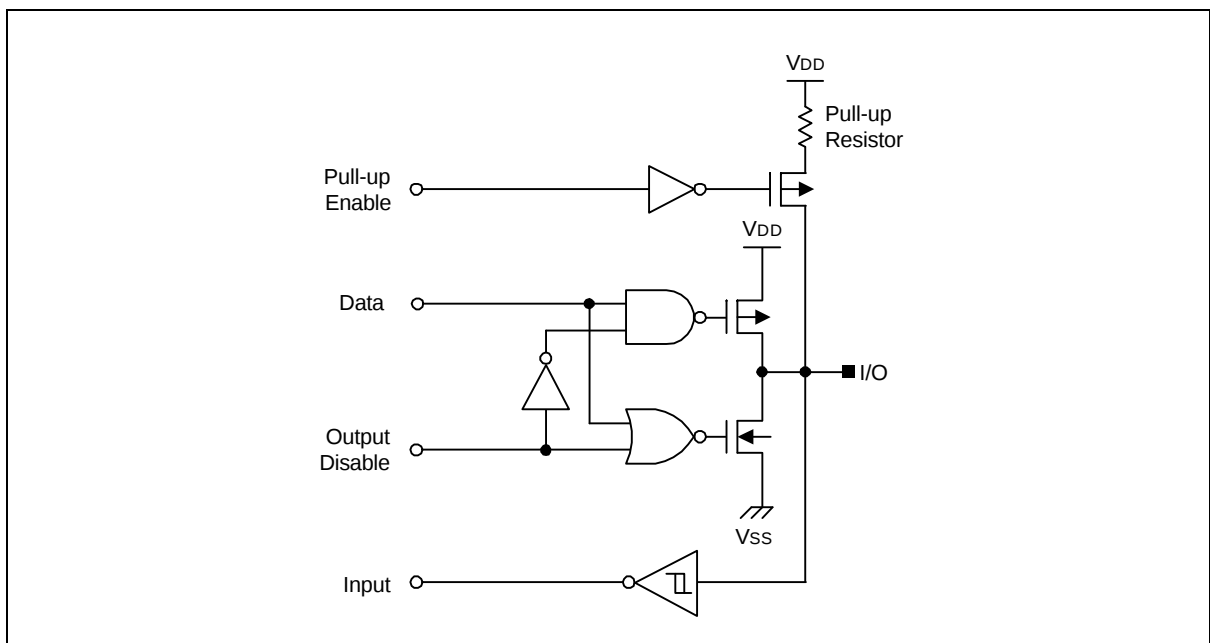


Figure 1-8. Pin Circuit Type 6 (Ports 2.4-2.7)

PIN CIRCUIT DIAGRAMS (Continued)

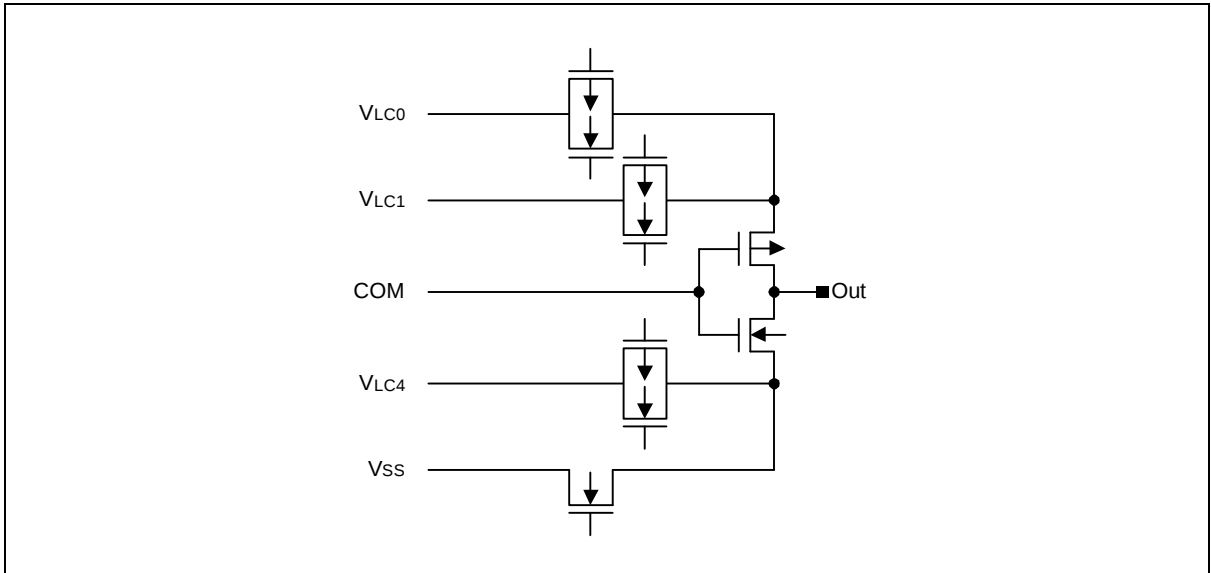


Figure 1-9. Pin Circuit Type 7 (COM0-COM17)

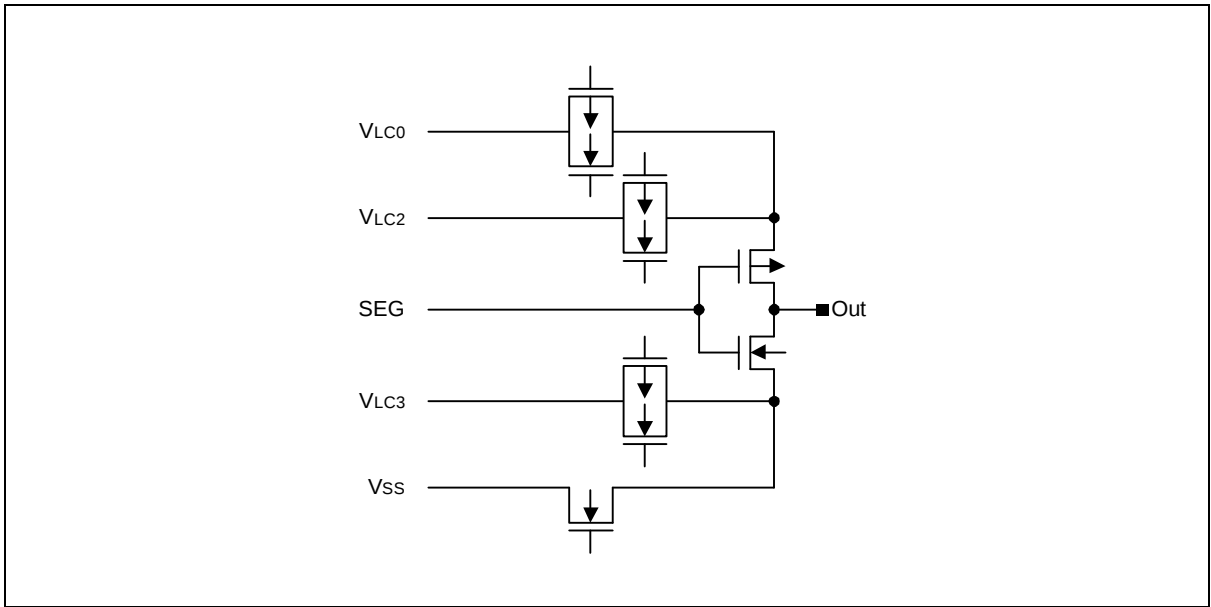


Figure 1-10. Pin Circuit Type 8 (SEG0-SEG64)

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ELECTRICAL DATA

OVERVIEW

In this chapter, KS88C2064 electrical characteristics are presented in tables and graphs. The information is arranged in the following order:

- Absolute maximum ratings
- D.C. electrical characteristics
- Data retention supply voltage in Stop mode
- Stop mode release timing when initiated by an external interrupt
- Stop mode release timing when initiated by a Reset
- I/O capacitance
- A.C. electrical characteristics
- Input timing for external interrupts (port 0, P2.3–P2.0)
- Input timing for RESET
- Oscillation characteristics
- Oscillation stabilization time

Table 15-1. Absolute Maximum Ratings

(T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V _{DD}	–	– 0.3 to + 5.5	V
Input voltage	V _{IN}	Ports 0, 1, 2, and 3	– 0.3 to V _{DD} + 0.3	V
Output voltage	V _O	All output pins	– 0.3 to V _{DD} + 0.3	V
Output current High	I _{OH}	One I/O pin active	– 18	mA
		All I/O pins active	– 60	
Output current Low	I _{OL}	One I/O pin active	+ 30	mA
		Total pin current for ports 0–3	+ 100	
Operating temperature	T _A	–	– 40 to + 85	°C
Storage temperature	T _{STG}	–	– 65 to + 150	°C

Table 15-2. D.C. Electrical Characteristics

(T_A = -40 °C to +85 °C, V_{DD} = 2.2 V to 4.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input High voltage	V _{IH1}	All input pins except V _{IH2} and V _{IH3}	0.8 V _{DD}	—	V _{DD}	V
	V _{IH2}	RESET	0.8 V _{DD}		V _{DD}	
	V _{IH3}	X _{IN} , XT _{IN}	V _{DD} - 0.5		V _{DD}	
Input Low voltage	V _{IL1}	All input pins except V _{IL2} and V _{IL3}	0	—	0.2 V _{DD}	
	V _{IL2}	RESET			0.2 V _{DD}	
	V _{IL3}	X _{OUT} , XT _{OUT}			0.5	
Output High voltage	V _{OH}	V _{DD} = 3.0 V; I _{OH} = -1 mA All output pins	V _{DD} - 1.0	—	—	μA
Output Low voltage	V _{OL}	V _{DD} = 3.0 V; I _{OL} = 2 mA All output pins	—	—	1.0	
Input High leakage current	I _{LIH1}	V _{IN} = V _{DD} ; all input pins except X _{IN} , X _{OUT} , XT _{IN} , and XT _{OUT}	—	—	1	
	I _{LIH2}	V _{IN} = V _{DD} ; X _{IN} , X _{OUT} , XT _{IN} , and XT _{OUT}			20	
Input Low leakage current	I _{LIL1}	V _{IN} = 0 V; all input pins except X _{IN} , X _{OUT} , XT _{IN} , and XT _{OUT}	—	—	-1	
	I _{LIL2}	V _{IN} = 0 V; X _{IN} , X _{OUT} , XT _{IN} , and XT _{OUT}			-20	
Output High leakage current	I _{LOH}	V _{OUT} = V _{DD} All output pins	—	—	1	
Output Low leakage current	I _{LOL}	V _{OUT} = 0 V All output pins	—	—	-1	

Table 15-2. D.C. Electrical Characteristics (Continued)

(T_A = -40°C to +85°C, V_{DD} = 2.2 V to 4.5 V)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Middle output voltage	V _{OM1}	V _{MN} = V _{LCD} − (N/5)	COM0–17	V _{M1} − 0.2	V _{M1}	V _{M1} + 0.2	V
	V _{OM2}	× V _{LCD}	SEG0–64	V _{M2} − 0.2	V _{M2}	V _{M2} + 0.2	
	V _{OM3}	N = 1, 2, 3, and 4	SEG0–64	V _{M3} − 0.2	V _{M3}	V _{M3} + 0.2	
	V _{OM4}		COM0–17	V _{M4} − 0.2	V _{M4}	V _{M4} + 0.2	
V _{LCD} −V _{COMi} voltage drop (i = 0–17)	V _{DC}	V _{LCD} = 3.0 V to 6.0 V − 15 μA per common pin		−	−	120	mV
V _{LCD} −V _{SEGx} voltage drop (x = 0–64)	V _{DS}	V _{LCD} = 3.0 V to 6.0 V − 15 μA per common pin		−	−	120	mV
LCD driving voltage	V _{LCD}	−		3.0	−	6.0	V
Pull-up resistors	R _{L1}	V _{IN} = 0 V; T _A = 25 °C; V _{DD} = 3.0 V Ports 0, 1, 2, and 3		30	80	200	kΩ
	R _{L2}	V _{IN} = 0 V; T _A = 25 °C; V _{DD} = 3.0 V RESET only		300	500	800	
LCD voltage dividing resistor	R _{LCD}	V _{LCD} = 3.0 V to 6.0 V T _A = 25 °C		40	60	80	kΩ
Supply current (note)	I _{DD1}	V _{DD} = 3.0 V ± 10% 2 MHz crystal		−	1.5	3.5	mA
	I _{DD2}	Idle mode; V _{DD} = 3.0 V ± 10% 2 MHz crystal			0.5	1.5	
	I _{DD3}	V _{DD} = 3.0 V ± 10% 32 kHz crystal			30	70	μA
	I _{DD4}	Idle mode; V _{DD} = 3.0 V ± 10% 32 kHz crystal			6	12	
	I _{DD5}	Stop mode; V _{DD} = 3.0 V ± 10% XT _{IN} = 0 V			0.5	1	

NOTES:

- Supply current does not include current drawn through internal pull-up resistors, LCD voltage dividing resistors, voltage doubler, or external output current loads.
- I_{DD1} and I_{DD2} include power consumption for subsystem clock oscillation.
- I_{DD3} and I_{DD4} are current when main system clock oscillation stops and the subsystem clock is used.

Table 15-3. Data Retention Supply Voltage in Stop Mode

(T_A = - 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V _{DDDR}	—	2.2	—	4.5	V
Data retention supply current	I _{DDDR}	V _{DDDR} = 2.2 V	—	—	5	μA
Release signal set time	t _{SREL}	—	0	—	—	μs
Oscillator stabilization wait time	t _{WAIT}	Released by RESET	—	2 ¹⁶ /f _X (1)	—	ms
		Released by interrupt	—	(2)	—	

NOTES:

1. f_X is the main oscillator frequency.
2. The duration of the oscillation stabilization time (t_{WAIT}) when it is released by an interrupt is determined by the setting in the basic timer control register, BTCON.

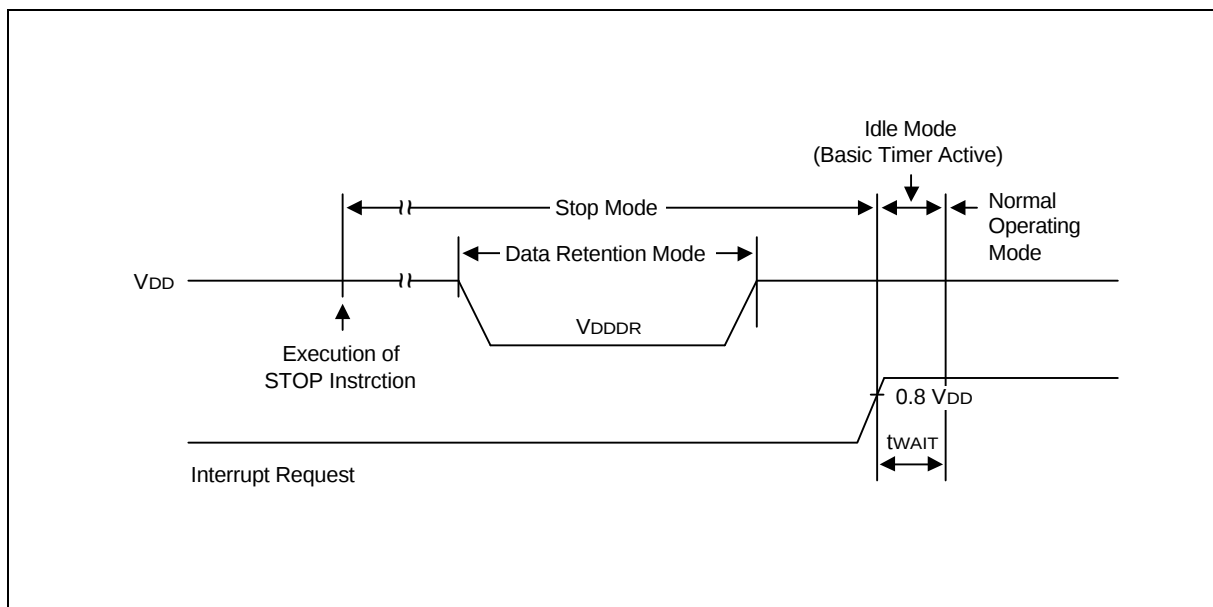


Figure 15-1. Stop Mode Release Timing When Initiated by an External Interrupt

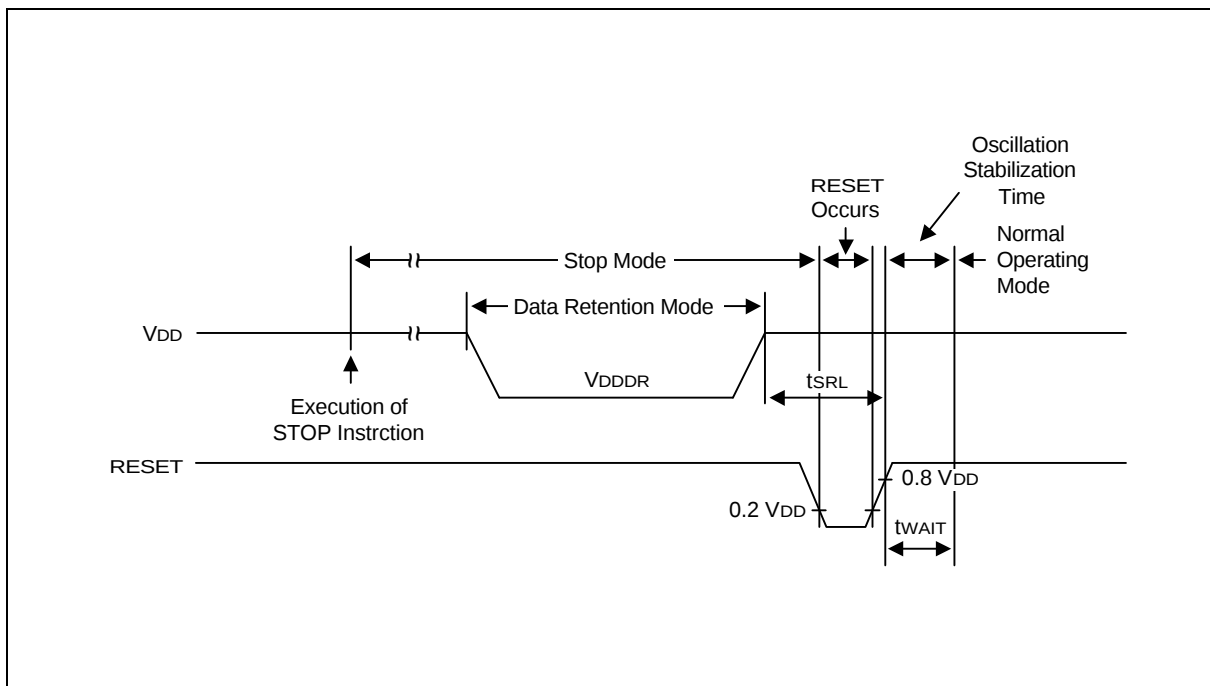


Figure 15-2. Stop Mode Release Timing When Initiated by a RESET

Table 15-4. Input/Output Capacitance

(T_A = -40 °C to +85 °C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C _{IN}	f = 1 MHz; unmeasured pins are connected to V _{SS}	—	—	10	pF
Output capacitance	C _{OUT}					
I/O capacitance	C _{IO}					

Table 15-5. A.C. Electrical Characteristics

(T_A = -40 °C to +85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Interrupt input, High, Low width	t _{INTH} , t _{INTL}	P3.0–P3.7 V _{DD} = 3 V	500	700	—	ns
RESET input Low width	t _{RSL}	Input V _{DD} = 3 V	2000	—	—	

Table 15-6. Voltage Doubler Output

(T_A = -40 °C to +85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Voltage Doubler Output	V _{BIAS}	V _{DD} = 3 V ± 10 % only	2 V _{DD} - 0.5	2 V _{DD}	2 V _{DD} + 0.5	V

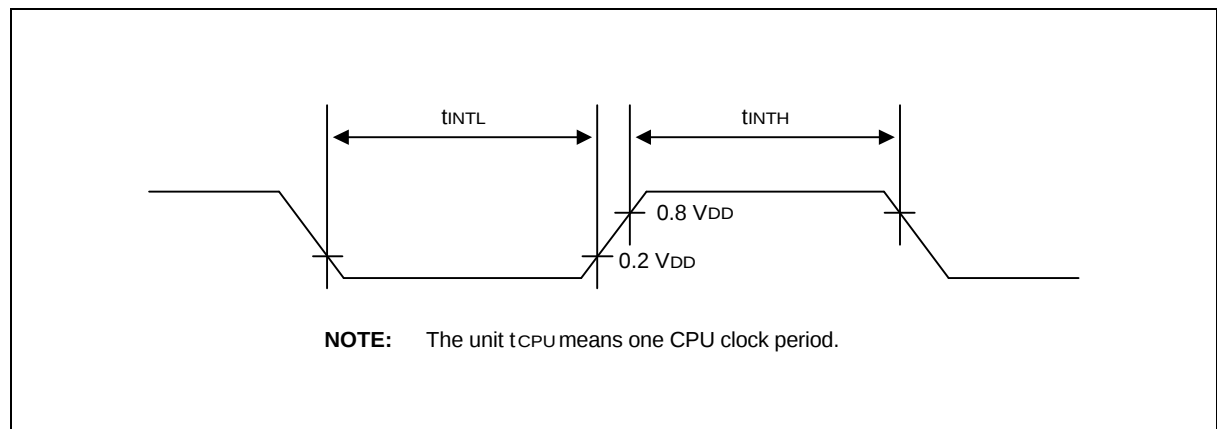


Figure 15-3. Input Timing for External Interrupts (P3.0–P3.7)

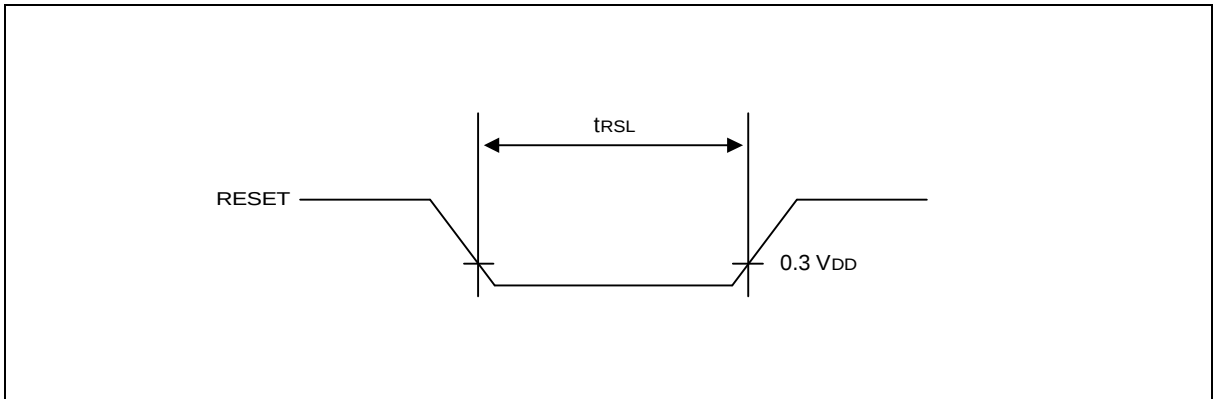


Figure 15-4. Input Timing for RESET

Table 15-7. Main Oscillation Characteristics

(T_A = - 40 °C + 85 °C, V_{DD} = 2.2 V to 4.5 V)

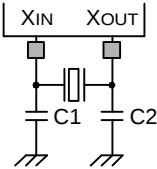
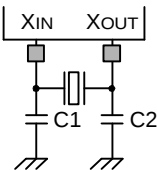
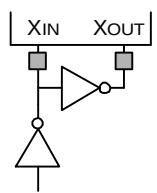
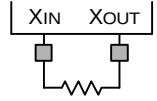
Oscillator	Clock Circuit	Conditions	Min	Typ	Max	Unit
Crystal		CPU clock oscillation frequency	0.4	—	4	MHz
Ceramic		CPU clock oscillation frequency	0.4	—	4	MHz
External clock		X _{IN} input frequency	0.4	—	4	MHz
RC		Frequency, V _{DD} = 3 V	0.4	—	2	MHz

Table 15-8. Sub Oscillation Characteristics

($T_A = -40\text{ }^{\circ}\text{C} + 85\text{ }^{\circ}\text{C}$, $V_{DD} = 2.2\text{ V}$ to 4.5 V)

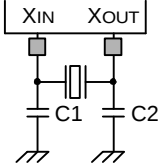
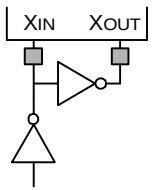
Oscillator	Clock Circuit	Conditions	Min	Typ	Max	Unit
Crystal		CPU clock oscillation frequency	32	32.768	35	kHz
External clock		XT_{IN} input frequency	32	—	500	kHz

Table 15-9. Main Oscillation Stabilization Time

($T_A = -40\text{ }^{\circ}\text{C} + 85\text{ }^{\circ}\text{C}$, $V_{DD} = 3.0\text{ V} \pm 10\%$)

Oscillator	Test Condition	Min	Typ	Max	Unit
Crystal	$f_x > 400\text{ kHz}$	—	—	80	ms
Ceramic	Oscillation stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	—	—	50	ms
External clock	X_{IN} input High and Low width (t_{XH} , t_{XL})	25	—	700	ns

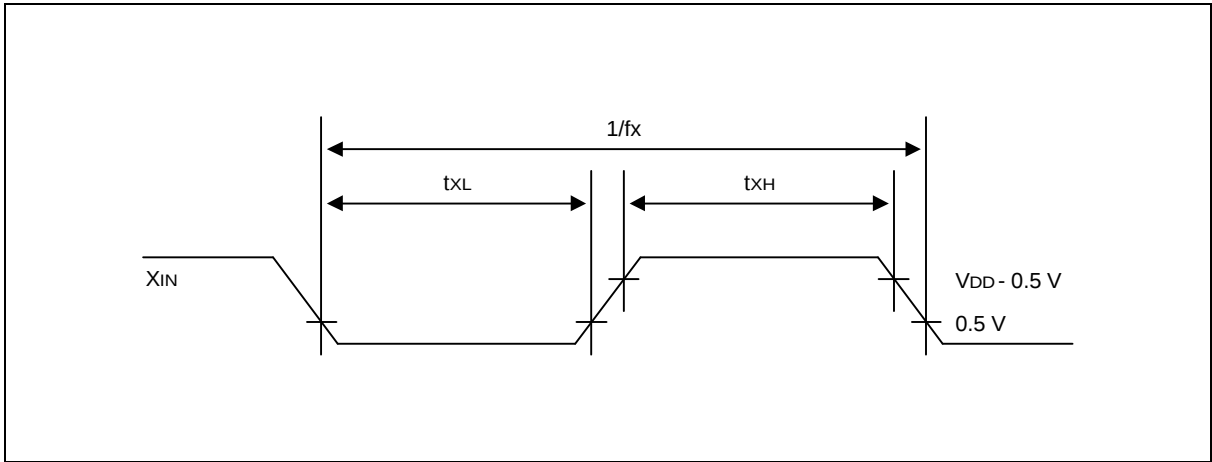


Figure 15-5. Clock Timing Measurement at X_{IN}

Table 15-10. Sub Oscillation Stabilization Time

($T_A = -40\text{ }^{\circ}\text{C} + 85\text{ }^{\circ}\text{C}$, $V_{DD} = 3.0\text{ V} \pm 10\%$)

Oscillator	Test Condition	Min	Typ	Max	Unit
Crystal	–	–	1.0	2	s
External clock	X_{IN} input High and Low width (t_{XH} , t_{XL})	1	–	18	μs

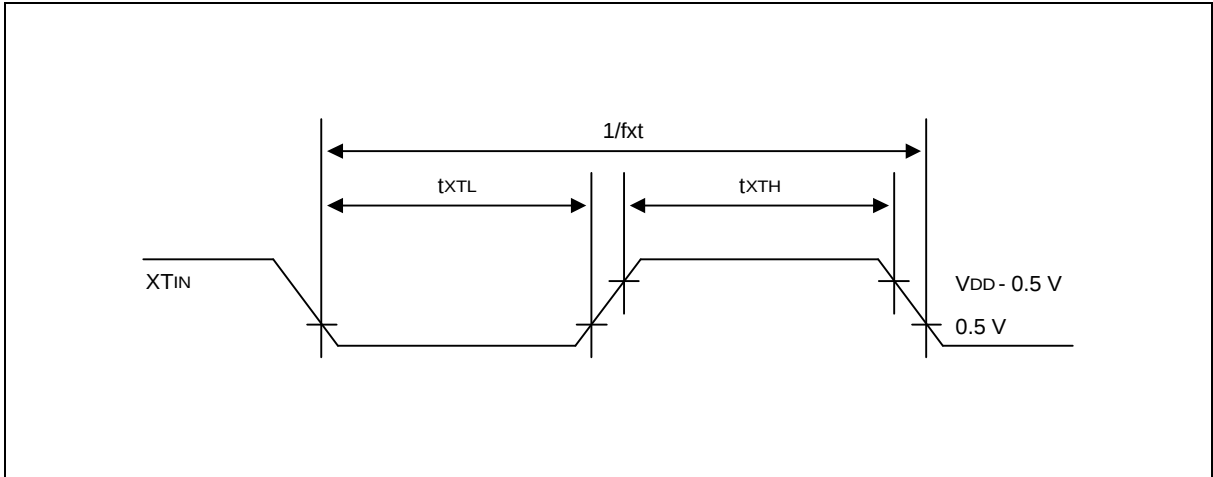


Figure 15-6. Clock Timing Measurement at X_{TIN}

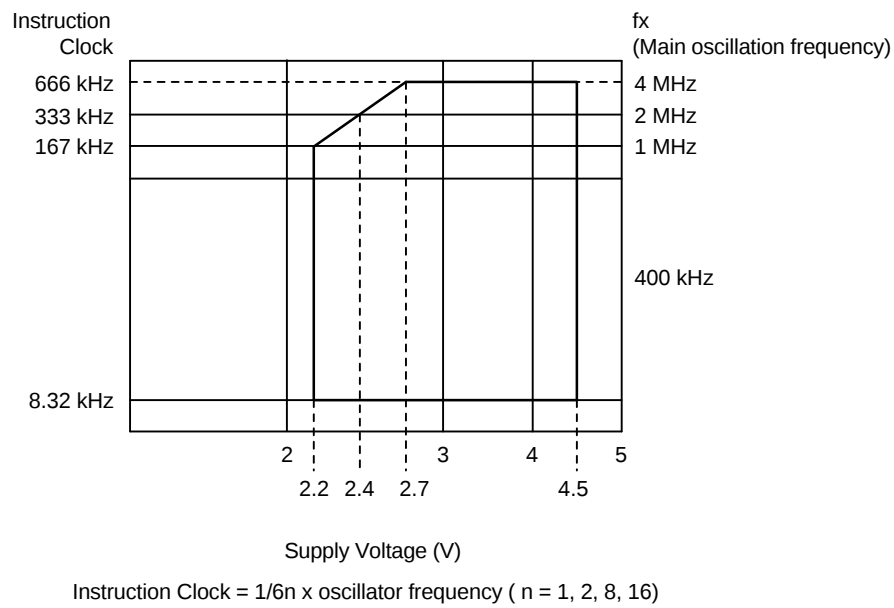


Figure 15-7. Operating Voltage Range

16 MECHANICAL DATA

OVERVIEW

The KS88C2064 microcontroller is currently available in a 128-pin TQFP package.

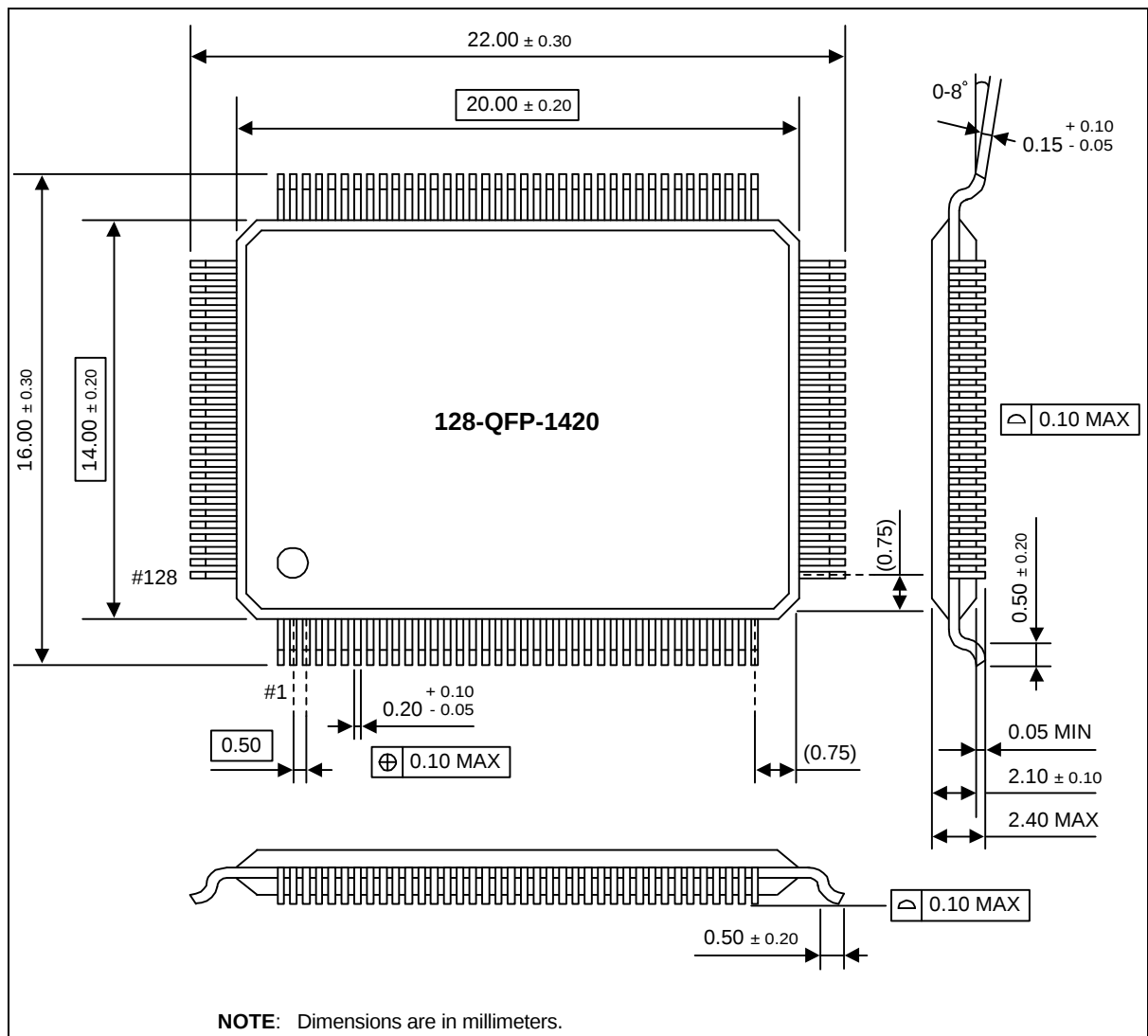


Figure 16-1. 128-Pin TQFP Package Mechanical Data