DS3124-1.0

MV4320

KEYPAD PULSE DIALLER

The MV4320 is fabricated using ISO-CMOS high density technology. The device is a pin-for-pin replacement for the DF320 Loop Disconnect Dialler and offers wider operating supply voltage range and lower power dissipation. The MV4320 accepts up to 20 digits from a standard 2 of 7 keypad and has a REDIAL option which is activated by the # key. The device provides dial pulsing and muting outputs and has a HOLD pin for interrupting a dialling sequence. Outpulsing, mark/space ratio and dialling speed are pin selectable.

The MV4320 is available in Ceramic DIL (DG, −40°C to +85°C).

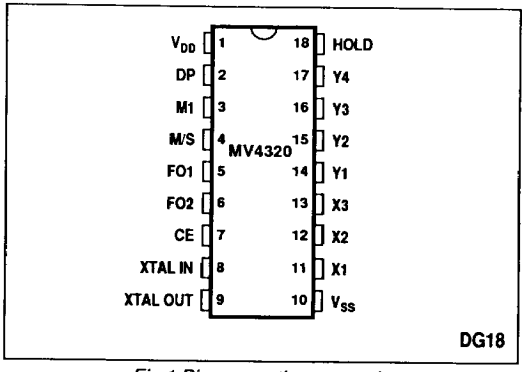

Fig.1 Pin connections - top view

FEATURES

- Pin for Pin Replacement for the DF320
- 2.5V to 5.5V Supply Voltage Operating Range
- 375μW Dynamic Power Dissipation at 3V
- Uses Inexpensive 3.58 MHz Ceramic Resonator or Crystal
- Stores up to 20 Digits
- Selectable Outpulsing Mark/Space Ratio
- Selectable Dialling Speeds of 10, 16, 20 and 932 Hz
- Low Cost

APPLICATIONS

- Pushbutton Telephones
- Tone to Pulse Converters
- Mobile Telephone
- Repertory Dialers

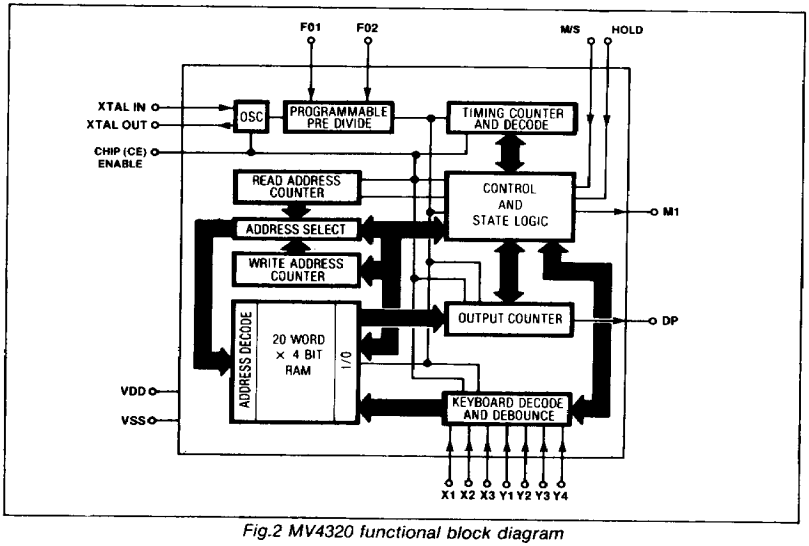

Fig.2 MV4320 functional block diagram

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD} = 3.0V; T_{amb} = +25°C; f_{CLK} = 3.579545MHz
All voltages wrt V_{SS}

		CHARACTERISTICS		SYMBOL	MIN	TYP*	MAX	UNITS	TEST CONDITIONS	
1	SUPPLY	Supply Voltage Operating Range		V_{DD}	2.5		5.5	V		
2		Standby Supply Current		I_{DDS}		1.0	10.0	μA	CE = V_{SS}	
3		Operating Supply Current		I_{DD}		125	200	μA	3.579545 MHz Crystal, $C_{XTALOUT}$ = 12pF	
4	INPUT	Pull-Up Transistor Source Current		I_{IL}	-0.5	-3.0	-12.0	μA	$V_{IN} = V_{SS}$	X_1, X_2, X_3
5		Input Leakage Current		I_{IH}		0.1		nA	$V_{IN} = V_{DD}$	Y_1, Y_2, Y_3, Y_4
6		Input Leakage Current		I_{IL}		-0.1		nA	$V_{IN} = V_{SS}$	M/S, IDP, F01,
7		Pull-Down Transistor Sink Current		I_{IH}	0.5	3.0	12.0	μA	$V_{IN} = V_{DD}$	F02, FD, HOLD
8		Logic '0' Level		V_{IL}			0.9	V	All inputs	
9		Logic '1' Level		V_{IH}	2.1			V		
10	OUTPUT	Voltage Levels	Low-Level	V_{OL}		0	0.01	V	No Load	DP, M1/M2
11			High-level	V_{OH}	2.99	3		V		
12		Drive Current	N-Channel Sink	I_{OL}	0.8	2.0		mA	V_{OUT} = 2.3V	
13			P-Channel Source	I_{OH}	-0.8	-2.0		mA	V_{OUT} = 0.7V	

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD} = 3.0V; T_{amb} = +25°C; f_{CLK} = 3.579545MHz
All voltages wrt V_{SS}

		CHARACTERISTICS	SYMBOL	MIN	TYP*	MAX	UNITS	TEST CONDITIONS
14	DYNAMIC	Output Rise Time	t_R		1.0		us	DP, M_1.
15		Output Fall Time	t_F		1.0		us	C_L = 50pF
16		Maximum Clock Frequency	t_{CLK}	3.58			MHz	3.579545 MHz Crystal
17		Mark to Space Ratio	M/S		2:1			Note 1
18					3:2			
19		Impulsing Rate = $\frac{1}{T}$			10		Hz	Note 1
20					16			
21					20			
22					932			
23		Clock Start Up Time	t_{on}		1.5	4	ms	Timed from CE '1'
24		Input Capacitance	C_{in}		5.0		pF	Any Input

* Typical parametric values are for Design Aid Only, not guaranteed and not subject to production testing. Timing waveforms are subject to production functional test.

NOTES:
1. See Pin Function, Table 1.

OPERATING NOTES

The first key entered in any dialling sequence initiates the oscillator by internally taking CE high. Digits may be entered asynchronously from the keypad. Dialling and mute functions are output as shown in figures 3 and 4. Figure 3 shows use of the circuits with external control of CE. This mode is useful if a bistable latching relay is used to mute and switch the complete pulse dialler circuit. In this mode, the pulse occurring on M1 when CE is taken high, with no keypad input, can be used to initiate the bistable latching relay. Figure 4 shows the timing diagram for the CE internal control mode. Initially CE is low and goes high on recognition of the first valid key input. Keypad data is entered asynchronously.

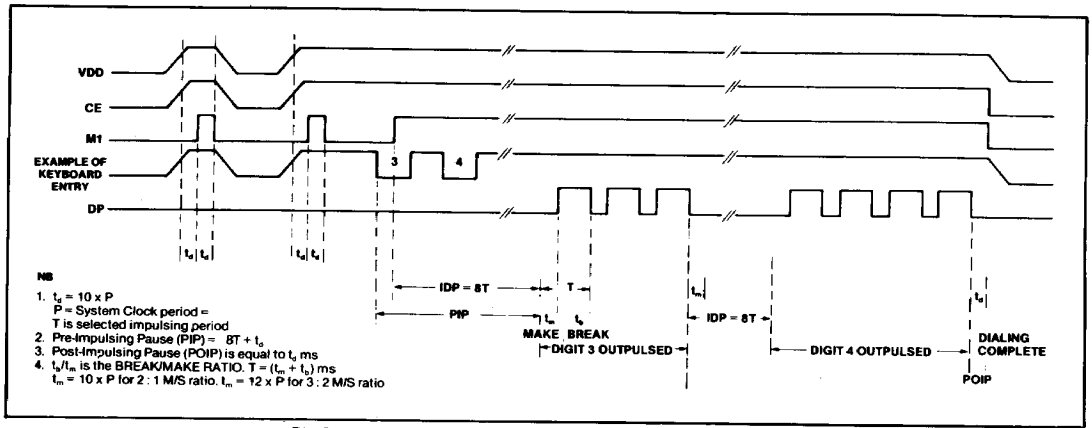

Fig.3 Keypad pulse dialer timing diagram, CE-External control

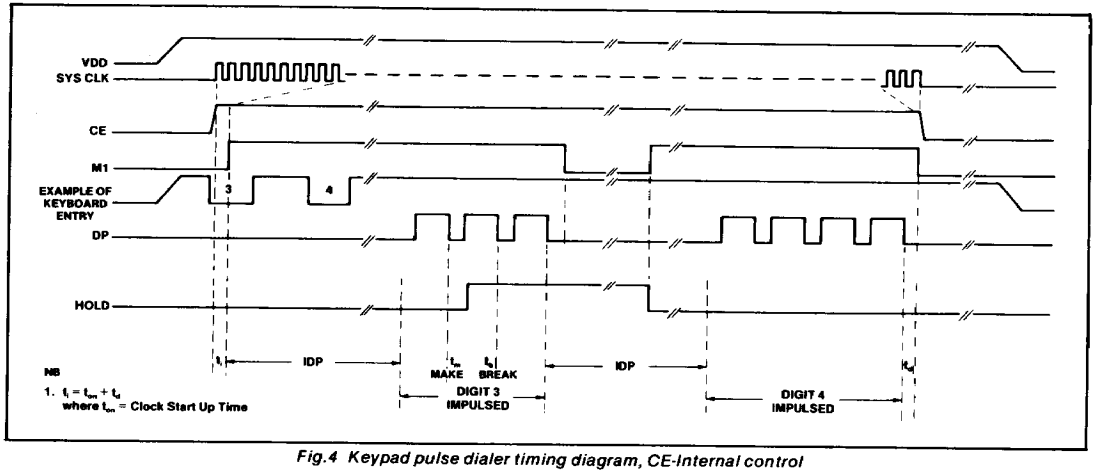

Fig.4 Keypad pulse dialer timing diagram, CE-Internal control

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

	MIN.	MAX.
V_{DD}-V_{SS}	-0.3V	10V
Voltage on any pin	V_{SS} - 0.3V	V_{DD} + 0.3V
Current at any pin		10mA
Operating Temperature	-40°C	+85°C
Storage Temperature	-65°C	+150°C
Power Dissipation		1000mW

Derate 16mW/°C above 75°C. All leads soldered to PC board.

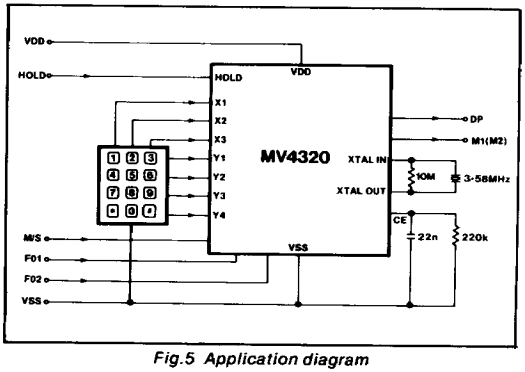

Fig.5 Application diagram

PIN FUNCTIONS

<table>
<tr><td>V_{DD}</td><td colspan="5">Positive voltage supply</td></tr>
<tr><td>DP</td><td colspan="5">Dial Pulsing Output Buffer</td></tr>
<tr><td>M1</td><td colspan="5">Mute Output (Off Normal) Buffer</td></tr>
<tr><td>M/S</td><td colspan="4">Mark/Space (Break/Make) Ratio select. On-chip pull-down transistor to V_{SS}.
Note: O/C = Open Circuit</td><td>O/C
V_{DD}</td><td>2:1
3:2</td></tr>
<tr><td>F01,F02</td><td colspan="2">Impulsing Rate Selection.
On-chip pull-down transistor to V_{SS}.
* Assumes f_{CLK} = 3.579545MHz.</td><td>F01
O/C
O/C
V_{DD}
V_{DD}</td><td>F02
O/C
V_{DD}
O/C
V_{DD}</td><td>Nominal Impulsing Rate
10Hz
20Hz
932Hz
16Hz</td><td>Actual* Impulsing Rate
10.13Hz
19.42Hz
932.17Hz
15.54Hz</td><td>System Clock frequency
303.9Hz
582.6Hz
27,965.1Hz
466.1Hz</td></tr>
<tr><td>CE</td><td colspan="5">Chip Enable. An active input. Control is internal via static keyboard decode, or by external forcing.</td></tr>
<tr><td>XTAL IN</td><td colspan="5">Crystal Input. Active, clamped low if CE = '0', high impedance if CE = '1'.</td></tr>
<tr><td>XTAL OUT</td><td colspan="5">Crystal Output Buffer to drive crystal.</td></tr>
<tr><td>V_{SS}</td><td colspan="5">System ground</td></tr>
<tr><td>X_1,X_2,X_3</td><td colspan="5">Column keyboard Inputs. On-chip pull-up transistors to V_{DD}.
Active LOW.</td></tr>
<tr><td>Y_1,Y_2,Y_3,Y_4</td><td colspan="5">Row keyboard Inputs. On-chip pull-up transistors to V_{DD}.
Active LOW.</td></tr>
<tr><td>HOLD</td><td colspan="5">O/C — Normal Operation
V_{DD} — No impulsing. If activated during impulsing, hold occurs when the current digit is complete
Prevents further impulsing. On-chip pull-down transistor to V_{SS}.</td></tr>
</table>