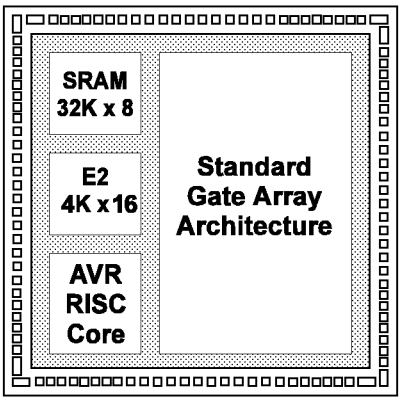
Features

- 0.5 µm Drawn Gate Length (0.45 µm L_{eff}) Sea-of-Gates Architecture with Triple-level Metal
- Embedded E^2 Memory up to 256 Kb
- 3.3V Operation with 5.0V Tolerant Input and Output Buffers
- High-speed, 200 ps Gate Delay, 2-input NAND, FO = 2 Nominal
- Up to 1.6 Million Used Gates - 684 pins
- System Level Integration Technology
  - Cores: ARM7TDMI™ and AV*R*® (8-bit RISC) Microcontrollers, USB and PCI Cores, 10T/100 Ethernet MAC
  - Memory: SRAM, ROM and FIFO; Gate Level or Embedded
  - I/O Interfaces: CMOS, LVTTL, LVDS, PCI, USB - 5V Tolerant I/O

Description

The ATL50/E^2 Series Embedded Array from Atmel offers the capability to incorporate E^2 memory in System Level Integration ASIC designs. The ATL50/E^2 is fabricated on 0.5 µm (drawn) process which combines logic and nonvolatile memory without significant penalties in memory speed or logic density. The E^2 blocks are identical to the blocks in Atmel's AT28 Series standard products. In addition to nonvolatile memory blocks, the ATL50/E^2 also offers system building blocks such as microcontrollers, USB function, PCI cores and a large number of other cores (UART, USART, SCC, etc.). Customers can specify their own unique embedded array, combining nonvolatile memory, logic, system blocks, cores, SRAM and ROM, resulting in a true system on a chip.

ATL50/E^2 Embedded Array (example)



Embedded Arrays

ATL50/E^2 Series

E^2
4K x 16
8K x 16
12K x 16
16K x 16

E^2 ASIC

Rev. 1173D–11/99

Absolute Maximum Ratings*

Operating Ambient Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Maximum Input Voltage:	
Inputs	V_{DD} + 0.5V
5V tolerant/compliant	V_{DD5} + 0.5V
Maximum Operating Voltage (V_{DD})	3.6V
Maximum Operating Voltage (V_{DD5})	5.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.3 Volt DC Characteristics

Applicable over recommended operating temperature and voltage range unless otherwise noted.

Symbol	Parameter	Buffer	Test Condition	Min	Typ	Max	Units
T_A	Operating Temp	All		-55		125	°C
V_{DD}	Supply Voltage	All		3.0	3.3	3.6	V
I_{IH}	High-level Input Current	CMOS	$V_{IN} = V_{DD}$, $V_{DD} = V_{DD}$ (max)			10	µA
		PCI				10	
I_{IL}	Low-level Input Current	CMOS	$V_{IN} = V_{SS}$, $V_{DD} = V_{DD}$ (max), Pull up = 620KΩ	-10			µA
		PCI		-10			
I_{OZ}	High-impedance State Output Current	All	$V_{IN} = V_{DD}$ or V_{SS}, $V_{DD} = V_{DD}$ (max), No pull up	-10		10	µA
I_{OS}	Output Short-circuit Current	2 mA Buffer	$V_{OUT} = V_{DD}$, $V_{DD} = V_{DD}$ (max)		14		mA
		2 mA Buffer	$V_{OUT} = V_{SS}$, $V_{DD} = V_{DD}$ (max)		-9		
V_{IH}	High-level Input Voltage	CMOS, LVTTL		2.0			V
		PCI		0.475V_{DD}			
		CMOS/TTL-level Schmitt		2.0	1.7		
V_{IL}	Low-level Input Voltage	CMOS				0.8	V
		PCI				0.325V_{DD}	
		CMOS/TTL-level Schmitt			1.1	0.8	
V_{HYS}	Hysteresis	TTL-level Schmitt			0.6		V
V_{OH}	High-level Output Voltage	P011	I_{OH} = 2 mA, $V_{DD} = V_{DD}$ (min)	0.7V_{DD}			V
		PCI	I_{OH} = -500 µA	0.9V_{DD}			
		PO11V	I_{OH} = -500 µA	0.7V_{DD}			
V_{OL}	Low-level Output Voltage	P011	I_{OL} = 2 mA, $V_{DD} = V_{DD}$ (min)			0.4	V
		PCI	I_{OL} = 1.5 mA			0.1V_{DD}	
		PO11V	I_{OL} = 500 µA			0.4	

I/O Buffer DC Characteristics

Symbol	Parameter	Test Condition	Typ	Units
C_{IN}	Capacitance, Input Buffer (die)	3.3V	2.4	pF
C_{OUT}	Capacitance, Output Buffer (die)	3.3V	5.6	pF
$C_{I/O}$	Capacitance, Bidirectional	3.3V	6.6	pF

I/O Buffers

- Programmable output drive (2 mA - 24 mA)
- 2,000 volt ESD protection
- Programmable slew rate control
- Programmable Pullup/Pulldown/Keeper

Design for Testability

Atmel supports a wide range of Design for Testability techniques to improve the percentage of a design that can be fully tested. By achieving a high degree of testability, a designer can reduce design and prototype debug time, minimize production test time, and improve board and system level test and diagnostic capability.

Synopsys Test Compiler software is fully supported by Atmel. By use of this system during design, the computer will create and add a set of scan chains to the design, and test vectors will be generated to provide greater than 95% fault coverage. This method requires only 1 or 2 added pins for Test Enable and Test Mode. This is the easiest and least expensive method of designing testability into a gate array design.

Ad Hoc means of increasing testability of a gate array are also available. Partitioning, memory array isolation, and test point insertion are encouraged and supported by the ATL50/E^2 Series embedded arrays. Atmel also encourages the inclusion of Built In Self-Test (BIST) techniques whenever possible. Each of these methods is discussed in detail in the Atmel CMOS Gate Array Design Manual.

In addition to all of the above, the ATL50/E^2 Series embedded arrays also support the Joint Test Action Group (JTAG) boundary scan architecture and Test Access Port (TAP) requirements. The required soft and hard macros to implement IEEE 1149.1 compliant architecture are available in Atmel's cell library. Use of JTAG architecture requires an additional 4 to 5 pins for test mode, data and clock signals.

Design

Design Systems Supported

Atmel supports several major software systems for design with complete cell libraries, as well as utilities for netlist verification, test vector verification and accurate delay simulations.

The following design systems are supported:

System	Version	Tools
Cadence®	4.4.3 2.1.p2 4.1-s051 2.5 3.4B 2.3	Opus™ - Schematic and Layout NC Verilog™ - Verilog Simulator Pearl™ - Static Path Verilog-XL™ - Verilog Simulator Logic Design Planner™ - Floorplanner BuildGates™ - Synthesis (Ambit)
Mentor/Model Tech™	5.2e B2 and Later	Modelsim Verilog and VHDL (VITAL) Simulator QuickVHDL™
Synopsys™	98.08, 98.05 5.0.1A	VSS™ - VHDL Simulator Design Compiler™ - Synthesis Test Compiler™ - Scan Insertion and ATPG Primetime™ - Static Path VCS™ - Verilog Simulator
Exemplar™	1998.2f	Leonardo Spectrum™ - Synthesis
Syntest	V2.2 V2.2 V1.6	TurboCheck - Gate TurboScan TurboFault

Design Flow

Atmel's Gate Array/Embedded Array design flow is structured to allow the designer to consolidate the greatest number of system components onto the same silicon chip, using widely available third party design tools. Atmel's cell library reflects silicon performance over extremes of temperature, voltage and process, and includes the effects of metal loading, inter-level capacitance and edge rise and fall times. The design flow includes clock tree synthesis to customer-specified skew and latency goals. RC extraction is performed on the final design database and incorporated into the timing analysis.

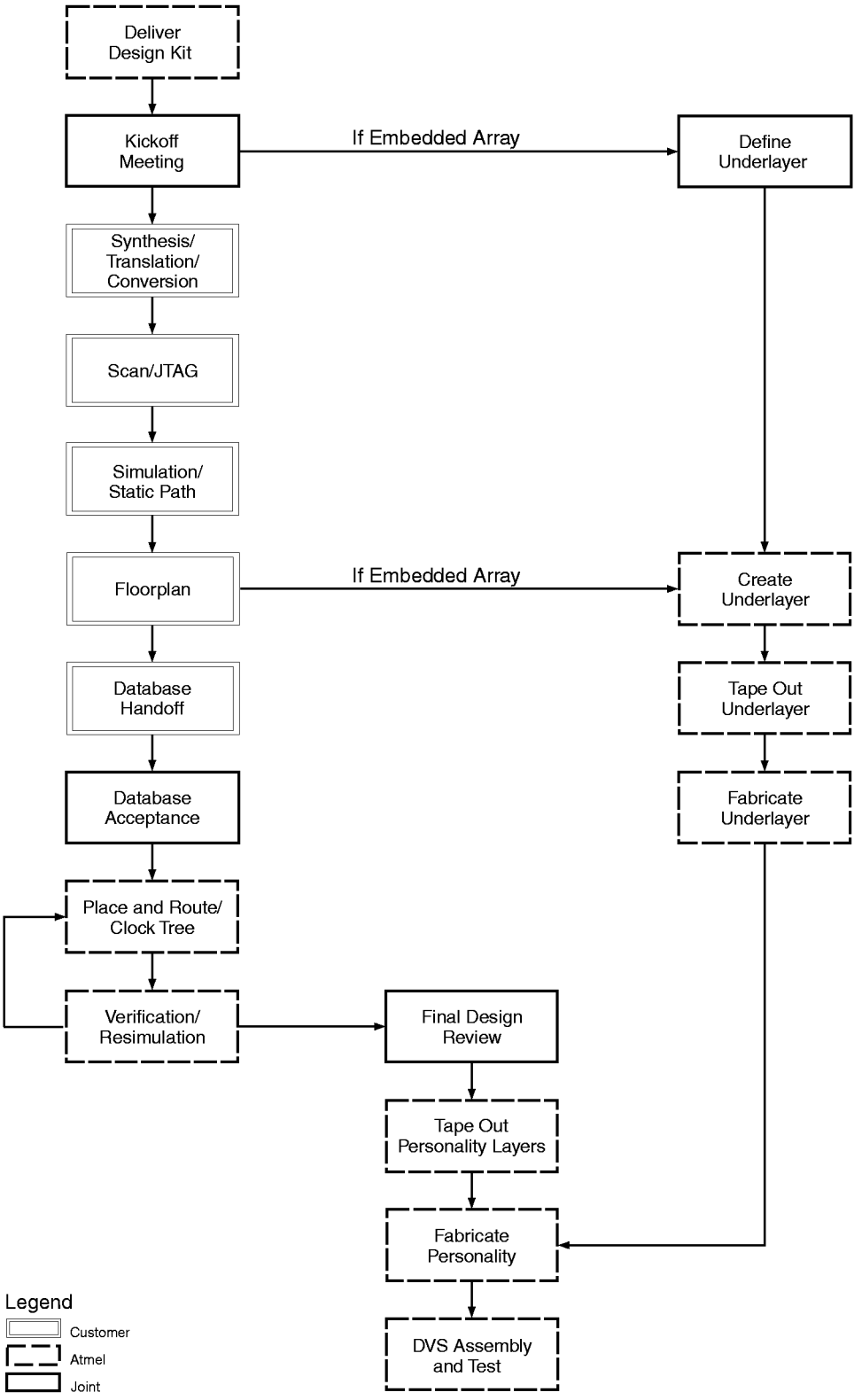
The **Gate Array/Embedded Array Design Flow**, shown on the following page, provides a pictorial description of the typical interaction between Atmel's design staff and the customer. Atmel will deliver design kits to support the customer's synthesis, verification, floorplanning and scan insertion activities. Tools such as Synopsys™, Cadence®, Verilog-HDL™, CTgen™, Exemplar™, PathMILL™ and TimeMILL™ are used, and many others are available. Should a design include embedded memory (SRAM, ROM or CAM) or an embedded core, Atmel will conduct a design review with the customer to understand the partition of the Gate Array/Embedded Array and to define the location of the memory blocks and/or cores so that an underlayer layout model can be created.

Following Database Acceptance, automated test pattern generation (ATPG) is performed, if required, on scan paths using Synopsys™ or Sunrise™ tools, the design is routed, and post-route RC data is extracted. After post-route verification and a Final Design Review, the design is taped out for fabrication.

Pin Definition Requirements

The corner pads are reserved for Power and Ground only. All other pads are fully programmable as Input, Output, Bidirectional, Power or Ground. When implementing a design with 5V compliant buffers, one buffer site must be reserved for the VDD5 pin, which is used to distribute 5V power to the compliant buffers.

Gate Array/Embedded Array Design Flow



Design Options

Logic Synthesis

Atmel can accept netlists in VHDL (MIL-STD-454, IEEE STD 1076) or Verilog-HDL™ format. Atmel fully supports Synopsys for VHDL™ simulation as well as synthesis. VHDL or Verilog-HDL is Atmel's preferred database format for Gate Array/Embedded Array design.

ASIC Design Translation

Atmel has successfully translated existing designs from most major ASIC vendors (LSI Logic®, Motorola®, SMOS™, Oki®, NEC®, Fujitsu®, AMI® and others) into Atmel ASICs. These designs have been optimized for speed and gate count and modified to add logic or memory, or replicated as a pin-for-pin compatible, drop-in replacement.

FPGA and PLD Conversions

Atmel has successfully translated existing FPGA/PLD designs from most major vendors (Xilinx®, Actel®, Altera®, AMD® and Atmel) into Atmel ASICs. There are four primary reasons to convert from an FPGA/PLD to an ASIC. Conversion of high volume devices for a single or combined design is cost effective. Performance can often be optimized for speed or low power consumption. Several FPGA/PLDs can be combined onto a single chip to minimize cost while reducing on-board space requirements. Finally, in situations where an FPGA/PLD was used for fast cycle time prototyping, an ASIC may provide a lower cost answer for long-term volume production.

Macro Cores

AVR (8-bit RISC) Microcontroller (8515)

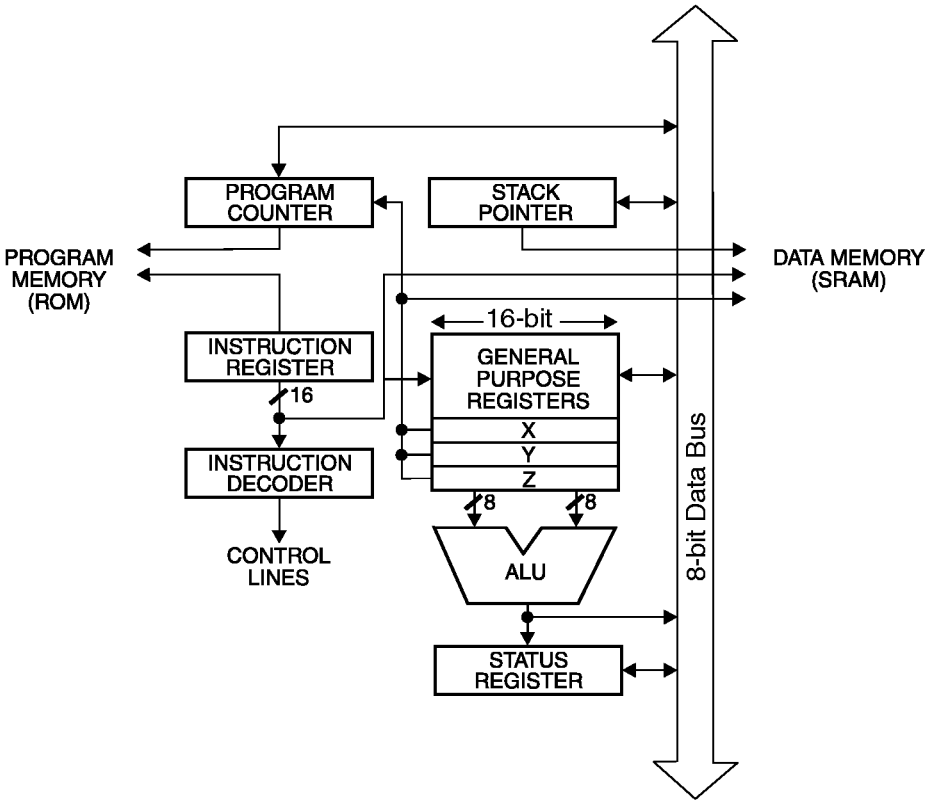
The AVR RISC Microcontroller is a true 8-bit RISC architecture, ideally suited for embedded control applications. The AVR is offered as a gate level, soft macro in the ATL50/E^2 family.

The AVR supports a powerful set of 120 instructions. The AVR pre-fetches an instruction during prior instruction execution, enabling the execution of one instruction per clock cycle.

The Fast Access RISC register file consists of 32 general purpose working registers. These 32 registers eliminate the data transfer delay in the traditional program code intensive accumulator architectures.

The AVR will interface with up to 8K x 8 program memory and 64K x 8 data memory. Included, are several optional peripherals: UART, 8-bit timer/counter, 16-bit timer/counter, external and internal interrupts and programmable watchdog timer.

AVR (8-bit RISC) ASIC Core



ARM7TDMI Embedded Microcontroller Core

The ARM7TDMI (Advanced RISC Machines) is a powerful 32-bit processor offered as an embedded core in the ATL50/E^2 series embedded arrays.

The ARM7TDMI is a member of the Advanced RISC Machines (ARM) family of general purpose 32-bit microprocessors, which offer high performance for very low power consumption.

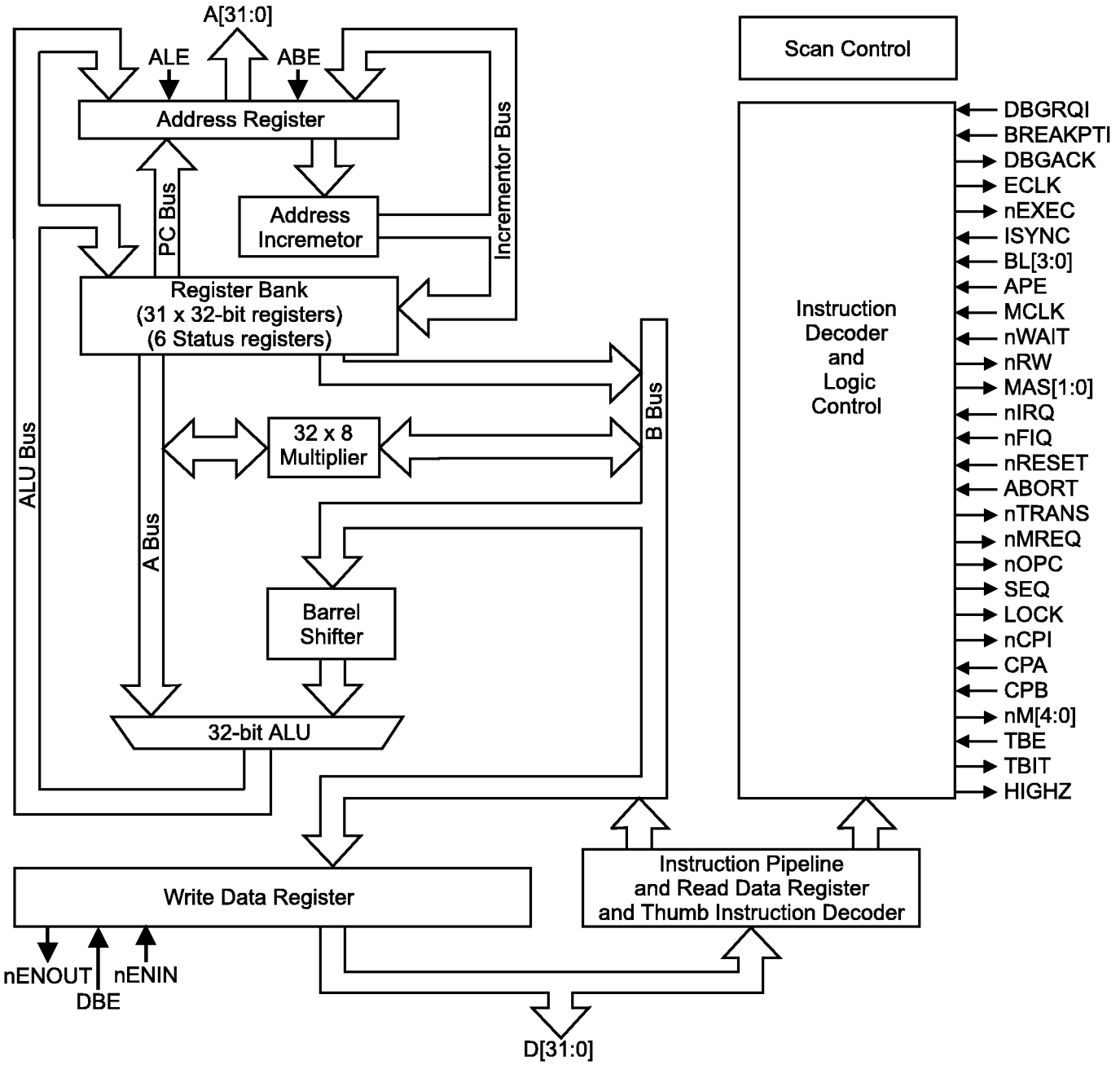
The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed Complex Instruction Set Computers (CISC). This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective chip.

Pipelining is employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM memory interface has been designed to allow the performance potential to be realized without incurring high costs in the memory system. Speed critical control signals are pipelined to allow system control functions to be implemented in standard low-power logic, and these control signals facilitate the exploitation of the fast local access modes offered by industry standard dynamic SRAMs.

The ARM7TDMI core includes several optional peripheral macros. The options offered are Real Time Clock, DMA Controller, USART, External Bus Interface, Interrupt, Timer and Advanced Power Management and Controller.

ARM7TDMI Embedded Microcontroller Core



Cell Index

Signal Name	Description	Site Count[1]
ADD3X	1-bit Full Adder with Buffered Outputs	10
AND2	2-input AND	2
AND2H	2-input AND - High-drive	3
AND3	3-input AND	3
AND3H	3-input AND - High-drive	4
AND4	4-input AND	3
AND4H	4-input AND - High-drive	4
AND5	5-input AND	5
AOI22	2-input AND into 2-input NOR	2
AOI22H	2-input AND into 2-input NOR - High-drive	4
AOI222	Two, 2-input ANDs into 2-input NOR	4
AOI222H	Two, 2-input ANDs into 2-input NOR - High-drive	8
AOI2223	Three, 2-input ANDs into 3-input NOR	4
AOI2223H	Three, 2-input ANDs into 3-input NOR - High-drive	7
AOI23	2-input AND into 3-input NOR	2
BUF1	1x Buffer	2
BUF2	2x Buffer	2
BUF2T	2x Tri-state Bus Driver with Active-high Enable	4
BUF2Z	2x Tri-state Bus Driver with Active-low Enable	4
BUF3	3x Buffer	3
BUF4	4x Buffer	3
BUF4T	4x Tri-state Bus Driver with Active-high Enable	5
BUF8	8x Buffer	5
BUF12	12x Buffer	8
BUF16	16x Buffer	10
CLA7X	7-input Carry Lookahead	5
DEC4	2:4 Decoder	7
DEC4N	2:4 Decoder with Active-low Enable	9
DEC8N	3:8 Decoder with Active-low Enable	24
DFF	D Flip-flop	8
DFFBCPX	D Flip-flop with Asynchronous Clear and Preset with Complementary Outputs	16
DFFBSRX	D Flip-flop with Asynchronous Set and Reset with Complementary Outputs	16
DFFC	D Flip-flop with Asynchronous Clear	9
DFFR	D Flip-flop with Asynchronous Reset	11
DFFS	D Flip-flop with Asynchronous Set	9

Cell Index (Continued)

Signal Name	Description	Site Count[1]
DFFSR	D Flip-flop with Asynchronous Set and Reset	12
DLY1500	Delay Buffer 1.5 ns	6
DLY2000	Delay Buffer 2.1 ns	10
DLY3000	Delay Buffer 3.0 ns	10
DLY6000	Delay Buffer 6.0 ns	24
DSS	Set Scan Flip-flop	11
DSSBCPY	Set Scan Flip-flop with Clear and Preset	16
DSSBR	Set Scan Flip-flop with Reset	13
DSSBS	Set Scan Flip-flop with Set	13
DSSR	Set Scan D Flip-flop with Reset	13
DSSS	Set Scan D Flip-flop with Set	12
DSSSR	Set Scan D Flip-flop with Set and Reset	14
HLD1	Bus Hold Cell	4
INV1	1x Inverter	1
INV1D	Dual 1x Inverters	2
INV1Q	Quad 1x Inverters	4
INV1TQ	Quad Tri-state Inverter	7
INV2	2x Inverter	2
INV2T	2x Tri-state Inverter with Active-high Enable	3
INV3	3x Inverter	2
INV4	4x Inverter	2
INV8	8x Inverter	4
INV10	10x Inverter	8
JKF	JK Flip-flop	10
JKFBCPX	Clear Preset JK Flip-flop with Asynchronous Clear and Preset and Complementary Outputs	16
JKFC	JK Flip-flop with Asynchronous Clear	12
LAT	LATCH	4
LATBG	LATCH with Complementary Outputs and Inverted Gate Signal	6
LATBH	LATCH with High-drive Complementary Outputs	7
LATR	LATCH with Reset	4
LATS	LATCH with Set	6
LATSR	LATCH with Set and Reset	8
MUX2	2:1 MUX	4
MUX2H	2:1 MUX - High-drive	5
MUX2I	2:1 MUX with Inverted Output	3

Cell Index (Continued)

Signal Name	Description	Site Count[1]
MUX2IH	2:1 MUX with Inverted Output - High-drive	4
MUX2N	2:1 MUX with Active-low Enable	4
MUX2NQ	Quad 2:1 MUX with Active-low Enable	18
MUX2Q	Quad 2:1 MUX	14
MUX3I	3:1 MUX with Inverted Output	6
MUX3IH	3:1 MUX with Inverted Output - High-drive	8
MUX4	4:1 MUX	9
MUX4X	4:1 MUX with Transmission Gate Data Inputs	10
MUX4XH	4:1 MUX with Transmission Gate Data Inputs - High-drive	10
MUX5H	5:1 MUX - High-drive	14
MUX8	8:1 MUX	18
MUX8N	8:1 MUX with Active-low Enable	20
MUX8XH	8:1 MUX with Transmission Gate Data Inputs - High-drive	18
NAN2	2-input NAND	2
NAN2D	Dual 2-input NAND	3
NAN2H	2-input NAND - High-drive	2
NAN3	3-input NAND	2
NAN3H	3-input NAND - High-drive	3
NAN4	4-input NAND	3
NAN4H	4-input NAND - High-drive	4
NAN5	5-input NAND	5
NAN5H	5-input NAND - High-drive	6
NAND5S	5-input NAND - Single Stage	3
NAN6	6-input NAND	6
NAN6H	6-input NAND - High-drive	7
NAN8	8-input NAND	7
NAN8H	8-input NAND - High-drive	7
NOR2	2-input NOR	2
NOR2D	Dual 2-input NOR	3
NOR2H	2-input NOR - High-drive	2
NOR3	3-input NOR	2
NOR3H	3-input NOR - High-drive	3
NOR4	4-input NOR	3
NOR4H	4-input NOR - High-drive	4
NOR5	5-input NOR	5
NOR5S	5-input NOR - Single Stage	3

Cell Index (Continued)

Signal Name	Description	Site Count[1]
NOR8	8-input NOR	7
OAI22	2-input OR into 2-input NAND	2
OAI22H	2-input OR into 3-input NAND - High-drive	4
OAI222	Two, 2-input ORs into 2-input NAND	2
OAI222H	Two, 2-input ORs into 2-input NAND - High-drive	4
OAI22224	Four, 2-input ORs into 4-input NAND	6
OAI23	2-input OR into 3-input NAND	3
ORR2	2-input OR	2
ORR2H	2-input OR - High-drive	3
ORR3	3-input OR	3
ORR3H	3-input OR - High-drive	4
ORR4	4-input OR	3
ORR4H	4-input OR - High-drive	4
ORR5	5-input OR	5
XNR2	2-input Exclusive NOR	4
XNR2H	2-input Exclusive NOR - High-drive	4
XOR2	2-input Exclusive OR	4
XOR2H	2-input Exclusive OR - High-drive	4

Note: 1. A single ATL50/E^2 routing site contains four transistors, two N-channels and two P-channels, aligned in columns. The number of sites used per gate varies according to the specific isolation and power requirements. Percent utilization varies from 50% to 70%, with more accurate utilization figures generated by DoubleCheck™, Atmel's netlist checker.

3.3 Volt I/O Buffer Cell Index

Cell Name	Description
PFIPCI	PCI Input
PFPECLL	Positive ECL Output
PFPECLR	Positive ECL Output
PIC	CMOS Input
PICH	CMOS Input - High-drive
PICI	CMOS Inverting Input
PICS	CMOS Input with Schmitt Trigger
PICSI	CMOS Inverting Input with Schmitt Trigger
PID	Differential Input
PO11	2 mA Tri-state Output
PO11F	2 mA Tri-state Output (fast)
PO11S	2 mA Tri-state Output (slow)
PO22	4 mA Tri-state Output
PO22F	4 mA Tri-state Output (fast)
PO22I	4 mA Inverting Tri-state Output
PO22S	4 mA Tri-state Output (slow)
PO33	6 mA Tri-state Output
PO33F	6 mA Tri-state Output (fast)
PO33S	6 mA Tri-state Output (slow)
PO44	8 mA Tri-state Output
PO44F	8 mA Tri-state Output (fast)
PO44S	8 mA Tri-state Output (slow)
PO55	10 mA Tri-state Output
PO55F	10 mA Tri-state Output (fast)
PO55S	10 mA Tri-state Output (slow)

3.3 Volt I/O Buffer Cell Index

Cell Name	Description
PO66	12 mA Tri-state Output
PO66F	12 mA Tri-state Output (fast)
PO66S	12 mA Tri-state Output (slow)
PO77	14 mA Tri-state Output
PO77F	14 mA Tri-state Output (fast)
PO77S	14 mA Tri-state Output (slow)
PO88	16 mA Tri-state Output
PO88F	16 mA Tri-state Output (fast)
PO88S	16 mA Tri-state Output (slow)
PO99	18 mA Tri-state Output
PO99F	18 mA Tri-state Output (fast)
PO99S	18 mA Tri-state Output (slow)
POAA	Tri-state Output
POAAF	Tri-state Output (fast)
POAAS	Tri-state Output (slow)
POBB	Tri-state Output
POBBF	Tri-state Output (fast)
POBBS	Tri-state Output (slow)
POCC	Tri-state Output
POCCF	Tri-state Output (fast)
POCCS	Tri-state Output (slow)
PX1L	XTAL Oscillator
PX2L	XTAL Oscillator
PX3L	XTAL Oscillator
PX4L	XTAL Oscillator

5.0 Volt Tolerant[1]

Cell Name	Description
PFIPCI	PCI Input
PFIPCIV	5V Tolerant PCI Input
PIC	CMOS Input
PICH	CMOS Input - High-drive
PICI	CMOS Inverting Input
PICS	CMOS Input with Schmitt Trigger
PICSI	CMOS Inverting Input with Schmitt Trigger
PICSV	5V Tolerant CMOS Input with Schmitt Trigger
PICV	5V Tolerant CMOS Input
PO11	2 mA Tri-state Output
PO11F	2 mA Tri-state Output (fast)
PO11S	2 mA Tri-state Output (slow)
PO11V	5V Tolerant 2 mA Tri-state Output
PO11VF	5V Tolerant 2 mA Tri-state Output (fast)
PO11VS	5V Tolerant 2 mA Tri-state Output (slow)
PO22	4 mA Tri-state Output
PO22F	4 mA Tri-state Output (fast)
PO22I	4 mA Inverting Tri-state Output
PO22S	4 mA Tri-state Output (slow)
PO22V	5V Tolerant 4 mA Tri-state Output
PO22VF	5V Tolerant 4 mA Tri-state Output (fast)
PO22VS	5V Tolerant 4 mA Tri-state Output (slow)
PO33	6 mA Tri-state Output
PO33F	6 mA Tri-state Output (fast)
PO33S	6 mA Tri-state Output (slow)
PO33V	5V Tolerant 6 mA Tri-state Output
PO33VF	5V Tolerant 6 mA Tri-state Output (fast)
PO33VS	5V Tolerant 6 mA Tri-state Output (slow)
PO44	8 mA Tri-state Output
PO44F	8 mA Tri-state Output (fast)
PO44S	8 mA Tri-state Output (slow)
PO44V	5V Tolerant 8 mA Tri-state Output
PO44VF	5V Tolerant 8 mA Tri-state Output (fast)
PO44VS	5V Tolerant 8 mA Tri-state Output (slow)
PO55	10 mA Tri-state Output
PO55F	10 mA Tri-state Output (fast)

5.0 Volt Tolerant[1]

Cell Name	Description
PO55S	10 mA Tri-state Output (slow)
PO55V	5V Tolerant 10 mA Tri-state Output
PO55VF	5V Tolerant 10 mA Tri-state Output (fast)
PO55VS	5V Tolerant 10 mA Tri-state Output (slow)
PO66	12 mA Tri-state Output
PO66F	12 mA Tri-state Output (fast)
PO66S	12 mA Tri-state Output (slow)
PO66V	5V Tolerant 12 mA Tri-state Output
PO66VF	5V Tolerant 12 mA Tri-state Output (fast)
PO66VS	5V Tolerant 12 mA Tri-state Output (slow)
PO77	14 mA Tri-state Output
PO77F	14 mA Tri-state Output (fast)
PO77S	14 mA Tri-state Output (slow)
PO77V	5V Tolerant 14 mA Tri-state Output
PO77VF	5V Tolerant 14 mA Tri-state Output (fast)
PO77VS	5V Tolerant 14 mA Tri-state Output (slow)
PO88	16 mA Tri-state Output
PO88F	16 mA Tri-state Output (fast)
PO88S	16 mA Tri-state Output (slow)
PO88V	5V Tolerant 16 mA Tri-state Output
PO88VF	5V Tolerant 16 mA Tri-state Output (fast)
PO88VS	5V Tolerant 16 mA Tri-state Output (slow)
PO99	18 mA Tri-state Output
PO99F	18 mA Tri-state Output (fast)
PO99S	18 mA Tri-state Output (slow)
PO99V	5V Tolerant 18 mA Tri-state Output
PO99VF	5V Tolerant 18 mA Tri-state Output (fast)
PO99VS	5V Tolerant 18 mA Tri-state Output (slow)
POAA	Tri-state Output
POAAF	Tri-state Output (fast)
POAAS	Tri-state Output (slow)
POAAV	5V Tolerant mA Tri-state Output
POAAVF	5V Tolerant mA Tri-state Output (fast)
POAAVS	5V Tolerant mA Tri-state Output (slow)
POBB	Tri-state Output
POBBF	Tri-state Output (fast)

5.0 Volt Tolerant[1]

Cell Name	Description
POBBS	Tri-state Output (slow)
POBBV	5V Tolerant mA Tri-state Output
POBBVF	5V Tolerant mA Tri-state Output (fast)
POBBVS	5V Tolerant mA Tri-state Output (slow)
POCC	Tri-state Output
POCCF	Tri-state Output (fast)
POCCS	Tri-state Output (slow)
PX1L	XTAL Oscillator
PX2L	XTAL Oscillator
PX3L	XTAL Oscillator
PX4L	XTAL Oscillator

5.0 Volt Compliant[2]

Cell Name	Description
PICV5	5V Compliant
PO22V5	5V Compliant 4 mA Tri-state Output
PO44V5	5V Compliant 8 mA Tri-state Output

Notes:
1. Tolerant: Can accept a 5.0 volt input but uses 3.3 volt power supply.
2. Compliant: Can accept a 5.0 volt input or output. Requires a 5.0 volt power supply.

Embedded E^2 Memory

Description

The ATL50/E^2 Series Embedded Array E^2 Memory blocks are accessed like a static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64 bytes simultaneously. During a write cycle, the addresses and 1 to 64 bytes of data are internally latched. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by polling of BUSY. Once the end of a write cycle has been detected, a new access for a read or write can begin.

Normal Operation Pins

Pin	Description
CLOCK	During LOAD operation: Rising edge latches address and input data if LOAD is high. If CLOCK is high, then the address and input data is latched as LOAD rises. During READ operation: Rising edge latches address data. Read access time will be based on the rising edge of CLOCK to valid data out.
AIN<12:0>	13 address bits to be read from or to be used for loading data when in the write mode.
DIN<15:0>	16 bits of input data.
DOUT<15:0>	16 bits of output data.
READ	Activates read mode. Active-high.
BYTEMD	When high enables data in byte mode only. When low enables data in 16-bit mode. This is valid for both read and write.
LOAD	While active, data is loaded. On falling edge write operation begins. When LOAD falls the address that is present in the address register is latched in and will represent the page address data will be written to. No address changes (no CLOCK pulses) should take place while BUSY is high.
BUSY	Indicates a write is in progress. This goes high after LOAD falls and stays active throughout the write cycle time.
WRTLOCK	When high will not allow the loading of data and preventing a write to be initiated due to unwanted control signal edges.
RESETB	External, active-low, reset which initializes the E^2 and clears BUSY to low.
POR	Power on reset. High at power on and low afterwards. Not to be confused with the system power on reset. This signal most generally will not be used.
OSC_128 kHz	External 128 kHz clock to control the write cycle timing. This is generated from the 13.56 MHz carrier frequency when in the contactless mode. No specific timing requirements other than a fixed frequency of 128 kHz.
EXT_CLK	In the contactless mode this signal will be high, enabling the use of the 128 kHz external clock (OSC_128 kHz) to the E^2. In the contacted mode this signal will be low and an internal oscillator will control the write cycle timing.

Test Mode Pins

Pin	Description
BLKMD	When high, a block write will be performed.
BLKDAT	Data to be written when in the block mode. If in the BLKMD, then make DIN = BLKDAT.
BLKE	Enables BLKDAT data to be written to the even pages. Active-high.
BLKO	Enables BLKDAT data to be written to the odd pages. Active-high.
TSTMD	Converts the address register to an address counter in the TSTMD.
CLEAR	Clears the address register when high.
INCR	On the rising edge, increments the address when TSTMD is high.
MARGIN	Used in the read mode to read the E^2 cell with a bias condition. If READ and MARGIN are high, the E^2 is in the read margin mode.
VMARGIN	Bias condition used when MARGIN is high.

Embedded E^2 Memory Normal Operations

BYTE MODE SIGNAL BYTEMD: BYTEMD controls if the E^2 will read/write a byte or a word at a time. If BYTEMD is high, then only 1 byte is read or written to. If BYTEMD is low, then a 2-byte word will be read or written to. If BYTEMD is low (word mode) and byte 1 is addressed, then byte 0 will be active as well. The same applies for bytes 2 & 3, 4 & 5 ..... 62 & 63.

READ: Reads may be byte or words (16 bits) according to BYTEMD signal. When LOAD is low and READ is high, rising edge of CLOCK latches address data and data stored at the memory location determined by the address pins is asserted on the DOUT[15:0] pins. Read mode is deactivated when LOAD or BUSY are high.

BYTE WRITE: When WRTLOCK is low and LOAD is high, rising edge of CLOCK latches address and input data. Write cycle starts when LOAD falls. The signal CLOCK may be a free running clock. In that case, LOAD should change synchronously with CLOCK falling to preclude inadvertent cases of CLOCK and LOAD momentarily high together. If CLOCK is static high, then a byte write could also be accomplished by using LOAD signal alone. In that case, the address and data are acquired on LOAD rising.

PAGE WRITE: The page write operation of E^2 allows 1 to 64 bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write. The first byte written can then be followed by 1 to 63 additional bytes clock in by CLOCK while holding LOAD high. Data may be loaded into the data latches in any order within the page boundary of 64 bytes.

Embedded E^2 Memory Test Modes Operations

In test mode (TSTMD = 1)

- The address register is converted into an address counter and a rising edge on INCR increments the address.
- CLEAR presets the address counter to 7FFh.
- CLOCK no longer latches address.
- The first INCR rising edge places the address counter at 000h.

READ: While READ and TSTMD is high, clear the address counter by pulsing CLEAR high. High pulse on INCR increment the address counter and data stored at the memory location determined by the address counter is asserted on the DOUT[15:0] pins.

WRITE: Write Operation in test mode is similar to the normal write except address is now changed by the INCR signal. With LOAD low, clear the address counter with a high pulse of CLEAR. Next, assert LOAD and pulse INCR to increment address. Then rising edge of CLOCK latches DIN[15:0]. Subsequent bytes are written by changing DIN, pulsing INCR and then latching data with CLOCK. Write cycle starts when LOAD falls. To continue writing following pages, do not activate CLEAR.

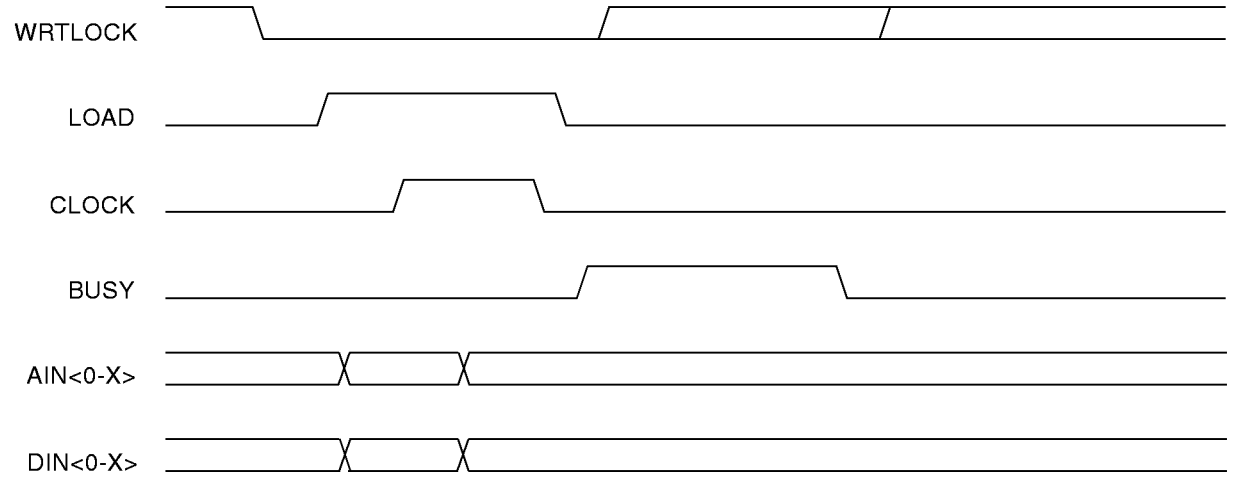
BLOCK WRITE: Block write could be used to set (1's) or clear (0's) the whole E^2. While BLKMD is high and BLKDAT is valid, assert LOAD. BLKDAT is then acquired on the rising edge of CLOCK. Write operation begins after LOAD falls. BLKDAT must be stable while LOAD and CLOCK are high. CLOCK can be left high always and block writing can be accomplished using only the LOAD signal.

EVEN/ODD BLOCK PAGE WRITES: While BLKE/BLKO is high, assert LOAD. While DIN is valid, pulse CLOCK to latch in data and continue for a whole page. Write operation begins after LOAD falls.

Waveforms

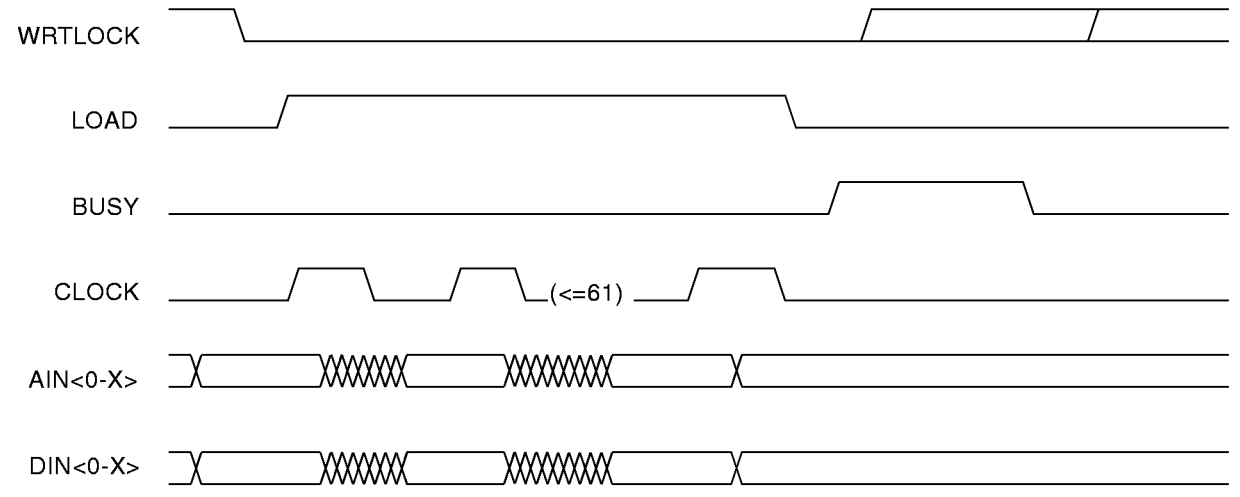
Byte Write

Low: TSTMD BLKMD BLKE BLKO MARGIN
High: RESETB
X: READ CLEAR INCR BLKDAT VMARGIN



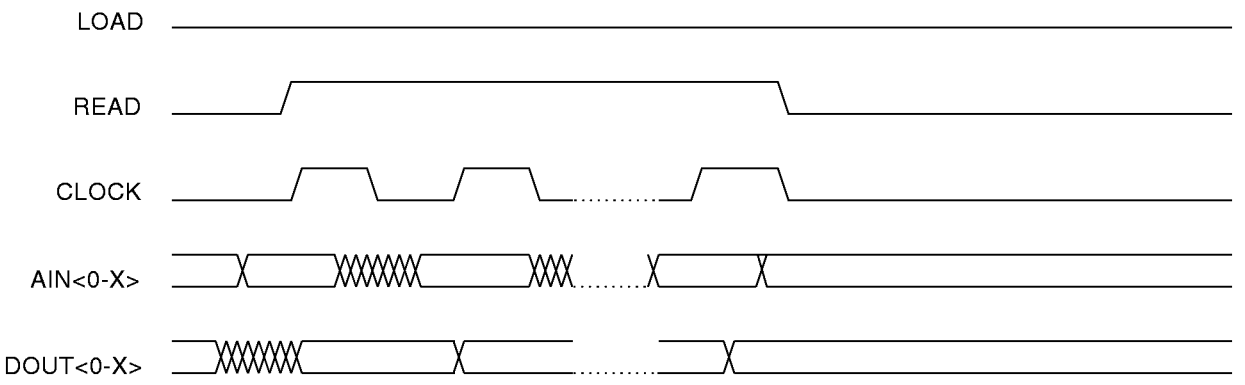
Write Page/Partial Page

Low: TSTMD BLKMD BLKE BLKO MARGIN
High: RESETB
X: READ CLEAR INCR BLKDAT VMARGIN



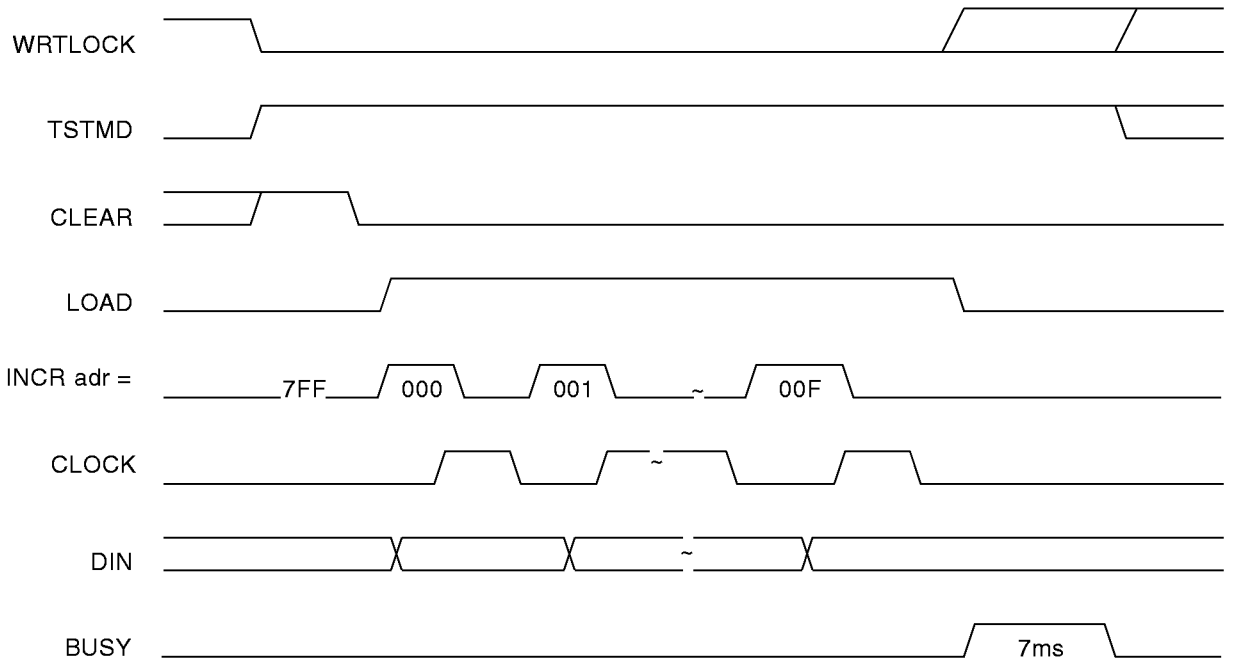
Read

Low: TSTMD BLKMD BLKE BLKO MARGIN
X: WRTLOCK DIN CLEAR INCR BLKDAT VMARGIN



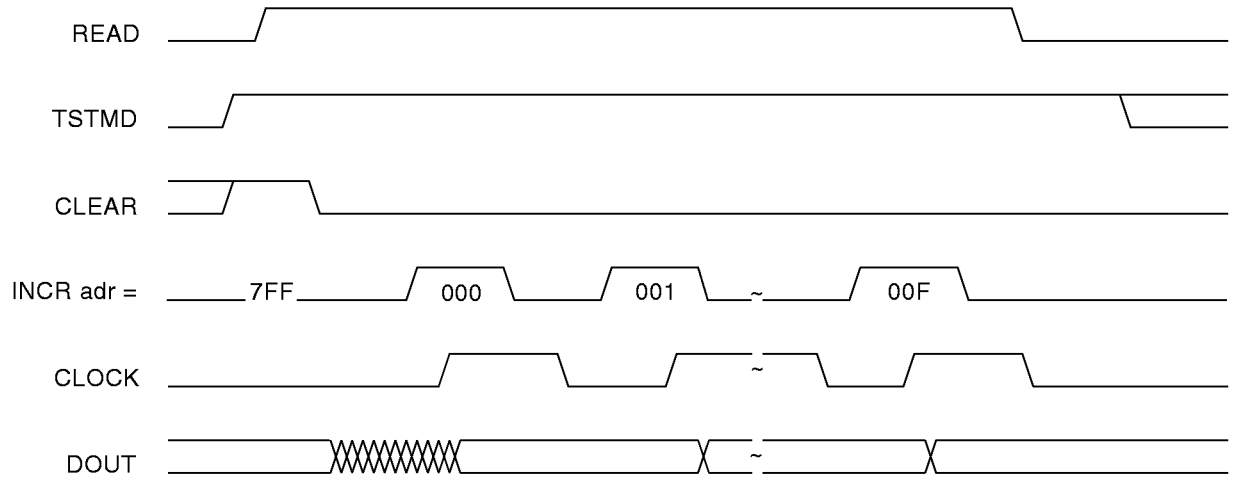
Writing with Address Counter (in test mode)

Low: BLKMD BLKE BLKO MARGIN
X: AIN READ BLKDAT VMARGIN



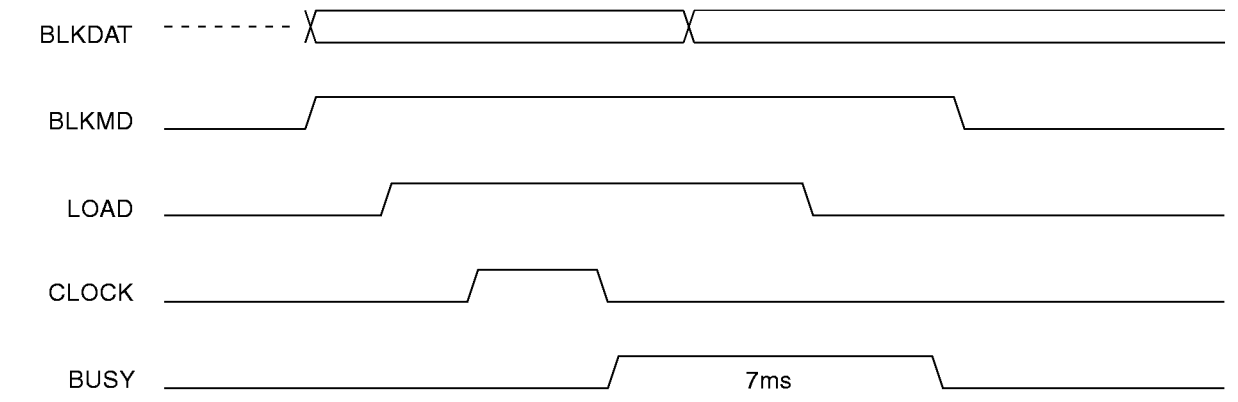
Reading with Address Counter (in test mode)

Low: LOAD TSTMD BLKMD BLKE BLKO MARGIN
X: WRTLOCK AIN INCR BLKDAT VMARGIN



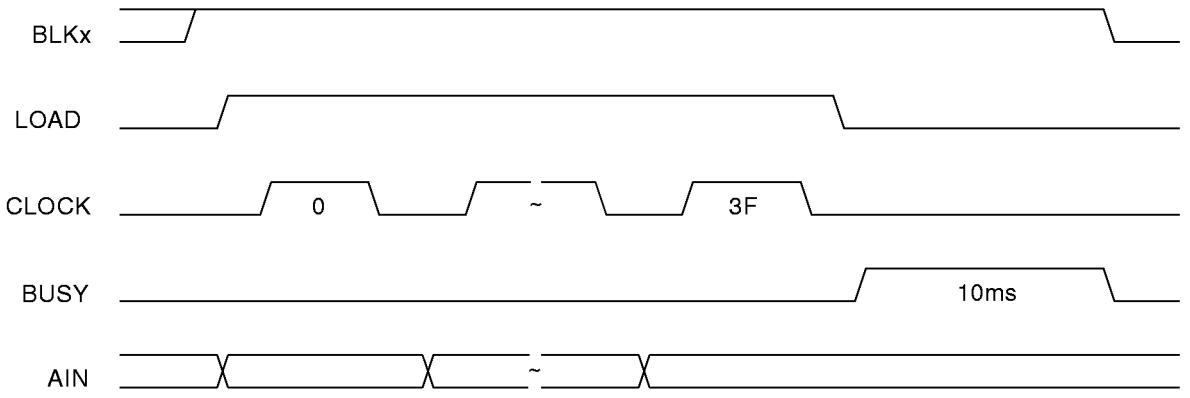
Block Writing (in test mode)

Low: WRTLOCK TSTMD BLKE BLKO MARGIN
X: AIN DIN CLEAR READ INCR VMARGIN



Even/Odd Block Page Writes

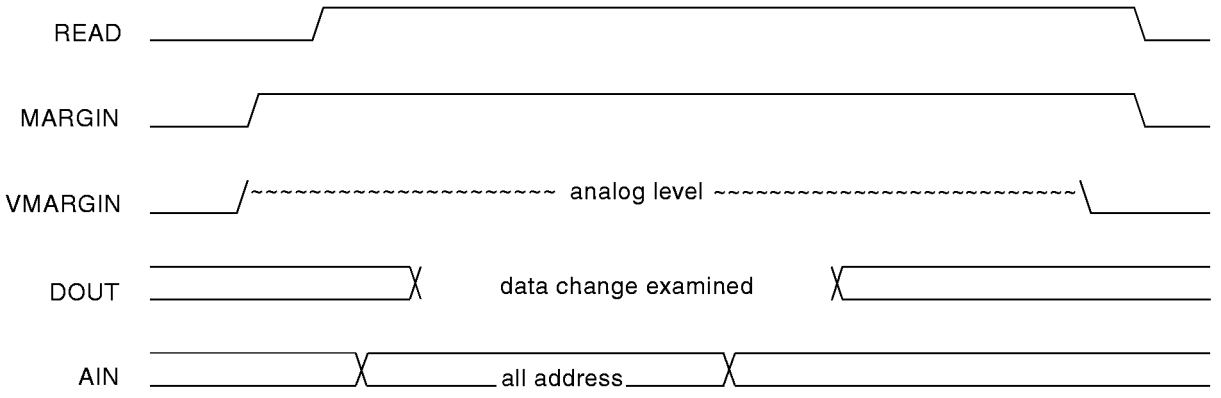
Low: TSTMD BLKMD MARGIN
X: WRTLOCK CLEAR INCR BLKDAT VMARGIN



Notes: 1. Page loading will be written to even pages if BLKE active or odd pages if BLKO active.
2. Page loading can also be accomplished via address counter write operation.

Read with Floating Gate Margin

Low: LOAD TSTMD BLKMD BLKE BLKO
X: WRTLOCK CLOCK CLEAR INCR BLKDAT DIN



Note: 1. Address can also be generated via address counter read operation.

Timing

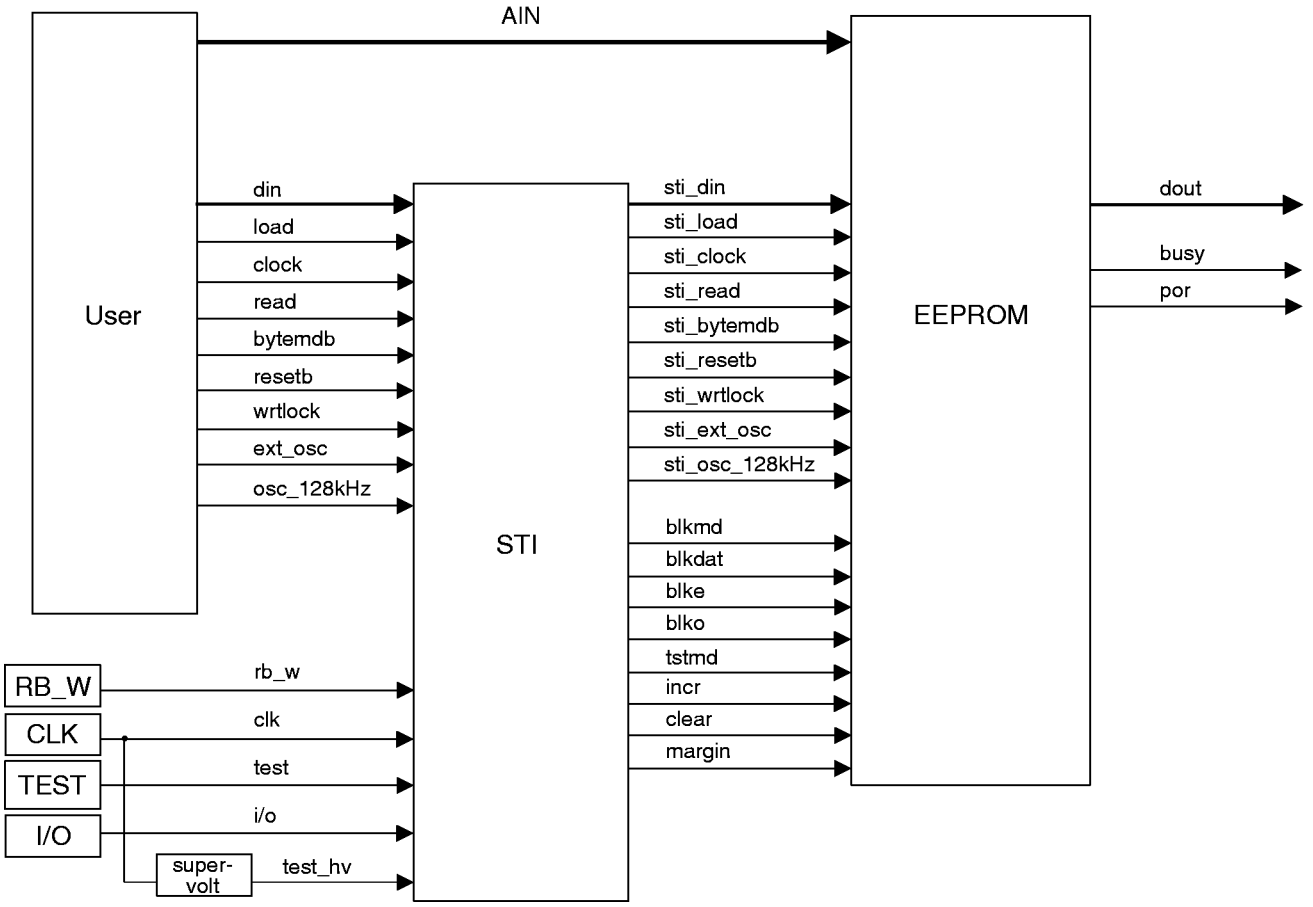
Supply Range 2.2V < Vsupply < 3.9V
Read Access Time < 100 ns
Erase/Write Time < 7 ms

Standard Test Interface (STI)

Description

The generic serial test circuit is used to insure a clean and usable test interface to the embedded EEPROM. This interface currently provides the ability to block, page and byte read/write the EEPROM core as well as perform margin testing of the EEPROM cells. Access to the test circuit is through a four-wire interface which can be multiplexed into customer logic or kept as a stand alone interface with a minimum of restrictions to the customer. The interface also includes provisions to allow additional user test modes to be added as needed. Access to the EEPROM is through an internal address counter.

STI Block Diagram



Programming E^2 with the STI Interface

Note that all numbers are expressed MSB to LSB from left to right. All data is loaded starting with LSB and is read from LSB to MSB.

Pins	Type	Function (in E^2 Mode)
I/O	Bidirectional	Serial data input/output in test modes. While an internal write is taking place, this pin will output a busy signal (low logic level) and ready (high logic level) when finished.
Rb/W	Input	Read not/write. This pin functions as an active-low read, active-high write and controls the data direction of the I/O pin.
TEST	Input	Test mode signal, used to initialize and change test modes. Margin voltage is supplied to the device through this pin during EEPROM margin testing.
CLK	Input	Clock, used to clock in serial data or test mode information.

Test Mode Codes

Hex Number	Binary Number	Name
00H	00000000b	Retest Test
03H	00000011b	Block Write
04H	00000100b	Even Page Block Write
05H	00000101b	Odd Page Block Write
06H	00000110b	Address Preset
07H	00000111b	Margin Read
21H	00100001b	bytemd read/write

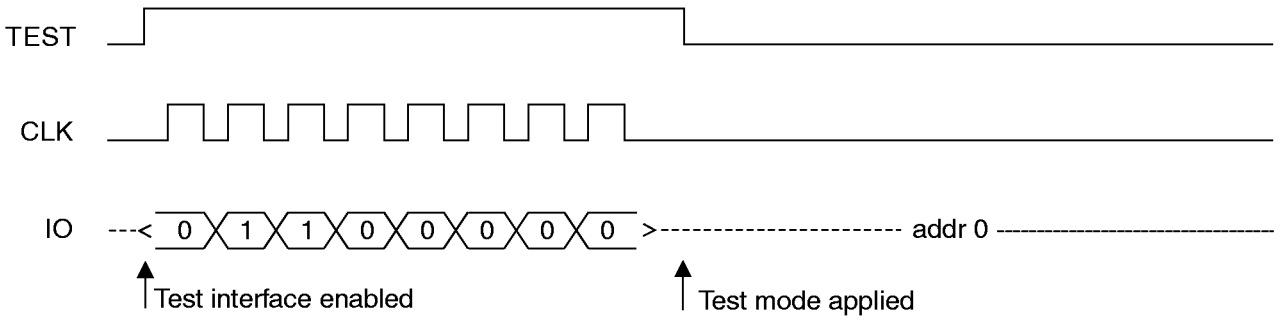
Device Operation

STR: Serial Test Register.

INITIALIZATION: The device will power up with test mode disabled. When allowed, test mode is entered by raising the voltage on TEST to 12 volts. At this time, test mode pins which are multiplexed with customer pins must become enabled for test purposes. Also at this time, customer logic pins must become “don’t cares” to the test control interface since these pins can not be guaranteed to be driven during the test mode. The test mode will remain in effect until either another code is entered into the STR or the device is powered off.

WRITING TEST MODE: With TEST pull high, use CLK to shift each bit of the test code (LSB to MSB) into the STR. Rb/W is a “don’t care” but can be held high to be consistent with a core write. Doing this will not cause a write to the core. The valid test modes will become effective when TEST returns to low and remains in effect until changed. See waveforms.

Test Mode Code Load (address present example)



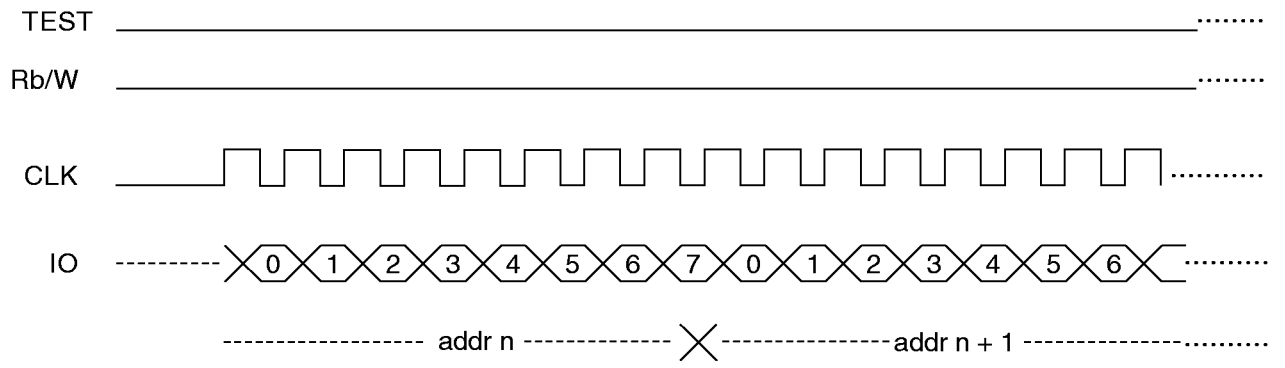
TEST MODE RESET: Writing 00H (MSB - > 00000000b < - LSB) to the STR will cause the device to terminate test mode. The STR will contain 00H on power up to indicate normal device operation.

ADDRESS PRESET: Writing 06H (00000110b) to the STR will cause the EEPROM address counter to be preset to its maximum address.

BYTE OPERATIONS: Writing 01H (00000001b) to the STR will enable normal read/write operations on the EEPROM core. The following operations are supported:

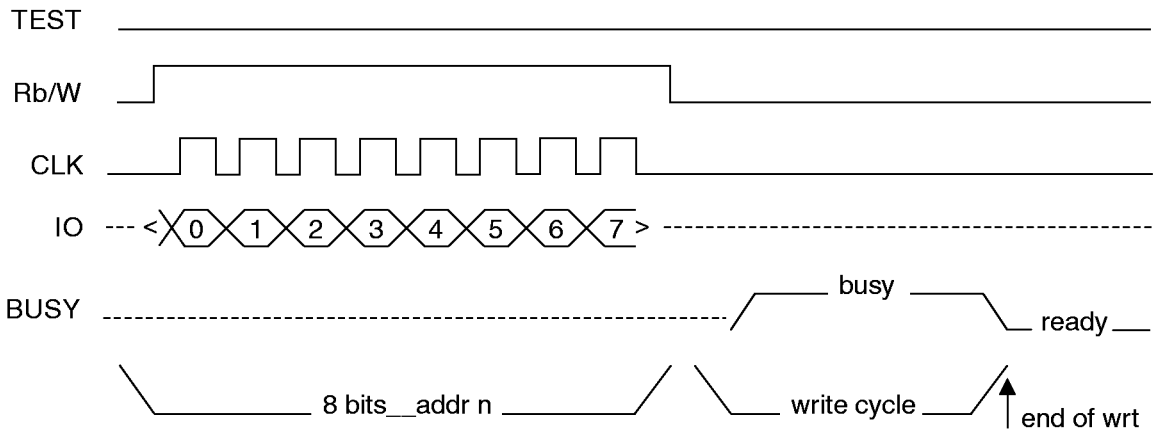
READ: With Rb/W low, data from the core will output starting with the LSB of the addressed byte pointed to by the address counter. Data is not guaranteed to be valid until the first CLK pulse takes place. The address counter will increment as needed with CLK to produce a continuous data stream without regard to the physical nature of the core (bit or byte wide). The address counter will wrap from max address to min address.

Normal Core Read



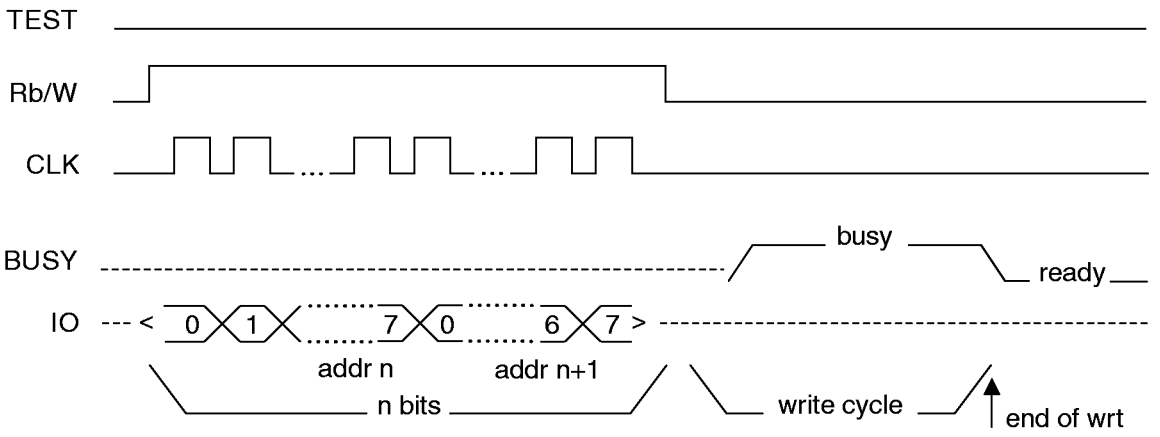
BYTE WRITE: With Rb/W high, shift data starting with the LSB of the byte into the SSR using CLK. When Rb/W falls, the write cycle will be initiated. The ready/busy signal will be present on I/O. A byte write after address preset will write the byte at address 0. After a byte write has finished, the next sequential byte can be written in the same fashion or the device may be clocked up to (apply CLK with Rb/W low) a higher address for the next write sequence.

Core Byte Write



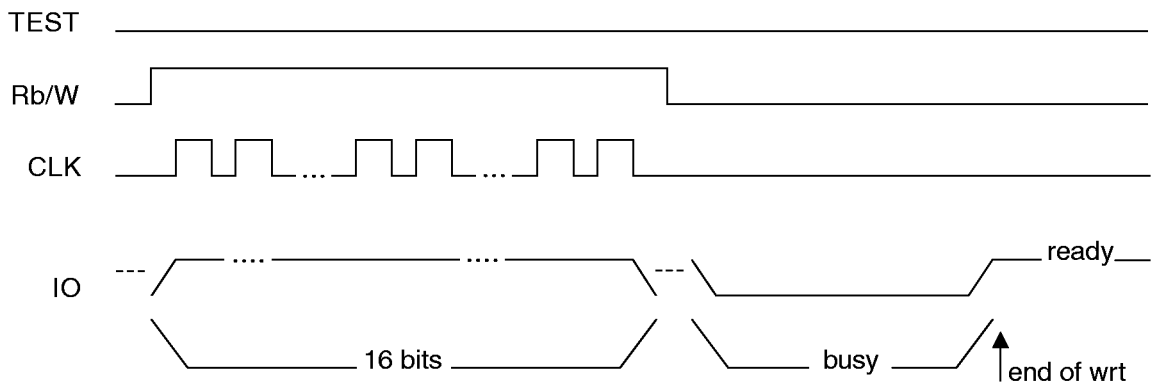
PAGE WRITE: This operation allows up to a wordline (512 bytes) to be written at the same time. Perform the same sequence as in the byte write operation “n” times, holding Rb/W high throughout. The address counter will increment as needed to accomplish this. When Rb/W falls, the write cycle will be initiated. The ready/busy signal will be present on BUSY. A page write performed after the address preset opcode will write the 1st page of the EEPROM (the page starting at address 0). By waiting for a page write to finish and then writing another page, multiple sequential pages can be written.

Core Page Write (two byte example)



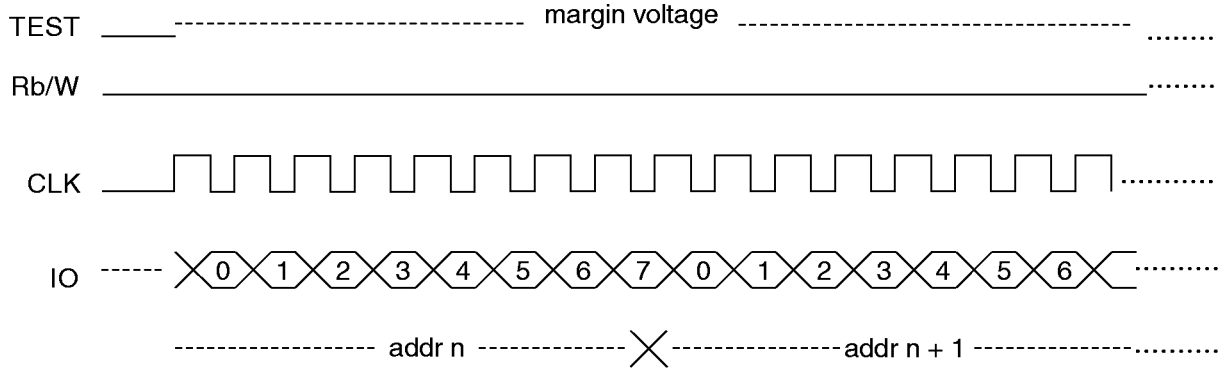
BLOCK MODE: Block modes are performed by entering 03H (00000011b) into the STR, which enables all wordlines and bitlines in the core. A block write (zeros) occurs by taking Rb/W high, pulling I/O low, pulsing clock for two bytes and allowing Rb/W to fall. A block clear (ones) takes place if I/O is high. The write cycle will be initiated when Rb/W falls. The read/busy signal will be present on I/O.

Block Write (two bytes - clear)



CORE MARGIN MODE: This mode is entered with a 07H (00000111b) code. This mode allows cell margins to be tested by placing a test voltage on TEST prior to reading the core. The practical voltage range of this test voltage is -0.7 volts to VDD -0.7 volts because of circuit constraints in the margin path.

Core Margin Read



EVEN PAGE BLOCK MODE: A code of 04H (00000100b) causes all the even wordlines to be selected. A normal page write should then be executed (see Page Write) to load the data into each even page within the core. This mode, in conjunction with the odd page block mode, allows certain test patterns to be written quickly.

ODD PAGE BLOCK MODE: A code of 05H (00000101b) causes all the odd wordlines to be selected. A normal page write should then be executed (see Page Write) to lead the data into each odd page within the core. This mode, in conjunction with the even page block mode, allows certain test patterns to be written quickly.

Advanced Packaging

The ATL50/E^2 Series Embedded Arrays are offered in a wide variety of standard packages, including plastic and ceramic quad flatpacks, thin quad flatpacks, ceramic pin grid arrays, and ball grid arrays. High volume onshore and offshore contractors provide assembly and test for commercial product, with prototype capability in Colorado Springs. Custom package designs are also available as required to meet a customer's specific needs, and are supported through Atmel's package design center. When a standard package cannot meet a customer's need, a package can be designed to precisely fit the application and to maintain the performance obtained in silicon. Atmel has delivered custom-designed packages in a wide variety of configurations.

Packaging Options

Package Type	Pin Count
PQFP	44, 52, 64, 80, 100, 120, 128, 132, 144, 160, 184, 208, 240, 304
Power Quad	144, 160, 208, 240, 304
L/TQFP	32, 44, 48, 64, 80, 100, 120, 128, 144, 160, 176, 216
PLCC	20, 28, 32, 44, 52, 68, 84
CPGA	64, 68, 84, 100, 124, 144, 155, 180, 223, 224, 299, 391
CQFP	64, 68, 84, 100, 120, 132, 144, 160, 224, 340
PBGA	121, 169, 208, 217, 225, 256, 272, 300, 304, 313, 316, 329, 352, 388, 420, 456
Super BGA	168, 204, 240, 256, 304, 352, 432, 560, 600
Low-profile BGA	132, 144, 160, 180, 208
Chip-scale BGA[1]	40, 49, 56, 64, 81, 84, 96, 100, 128

Notes: 1. Partial List