Features

- **0.8 µ drawn (0.6 µ effective) gate length combined with triple level metal provides outstanding speed/density performance.**
- **All ATL80 arrays can operate at 5.0 volts and 3.3 volts for low-power applications. The ATL80 series can also operate in a mixed voltage environment.**
- **Design translation of existing ASIC, FPGA and PLD designs provide for easy alternate sourcing with equivalent performance.**
- **Product testability is improved using techniques such as serial and boundary scan, ATPG, built-in self test and JTAG.**
- **ATL80 arrays can be screened to MIL-STD-883.**

Description

The high-performance ATL80 Series CMOS gate arrays offer superior system performance, flexibility, testability and board utilization. The ATL80 gate arrays employ an advanced technology 0.8 µ-drawn, triple-level metal, Si-gate, CMOS technology processed in a U.S.-based, manufacturing facility.

Atmel's efficient routing scheme combined with tight spacing for three metal layers allows Atmel to provide more gates and faster speeds. With fine pitch bond pads as a standard feature, high I/O gate arrays can easily be accommodated. The ATL80 gate array can have a 3.3 volt or 5.0 volt core, combined with a 3.3 volt and/or 5.0 volt I/O on the same chip. Atmel's I/O can be personalized to accept a 5.0 volt input signal into a 3.3 volt buffer.

Atmel's flexible design system uses industry design standards and is compatible with popular CAD/CAE software and hardware packages. The 0.8 µ macro cell libraries are upward compatible with the existing 1.0 µ libraries and design utilities.

ATL80 Array Organization

Device Number	Raw Gates	Routable Gates	Max Pin Count	Max I/O Pins	Gate(1) Speed
ATL80/2	2,000	1,000	36	28	256 ps
ATL80/5	5,000	3,000	68	60	256 ps
ATL80/10	10,000	6,000	80	72	256 ps
ATL80/15	17,000	10,200	100	92	256 ps
ATL80/25	26,000	15,600	120	112	256 ps
ATL80/40	39,000	23,400	144	136	256 ps
ATL80/50	50,000	30,000	160	152	256 ps
ATL80/75	75,000	45,000	184	176	256 ps
ATL80/95	94,000	60,000	208	192	256 ps
ATL80/150	150,000	75,000	256	236	256 ps
ATL80/220	220,000	110,000	304	280	256 ps
ATL80/280	280,000	140,000	340	310	256 ps
ATL80/350	350,000	175,000	380	350	256 ps
ATL80/450	450,000	225,000	424	384	256 ps
ATL80/600	600,000	300,000	480	440	256 ps

Note: 1. Nominal 2 Input NAND Gate With a Fan Out of 2

ATL80 Series Gate Arrays 0.8 Micron

ATL80/2
ATL80/5
ATL80/10
ATL80/15
ATL80/25
ATL80/40
ATL80/50
ATL80/75
ATL80/95
ATL80/150
ATL80/220
ATL80/280
ATL80/350
ATL80/450
ATL80/600

5

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ATL80 Design

Design Systems Supported

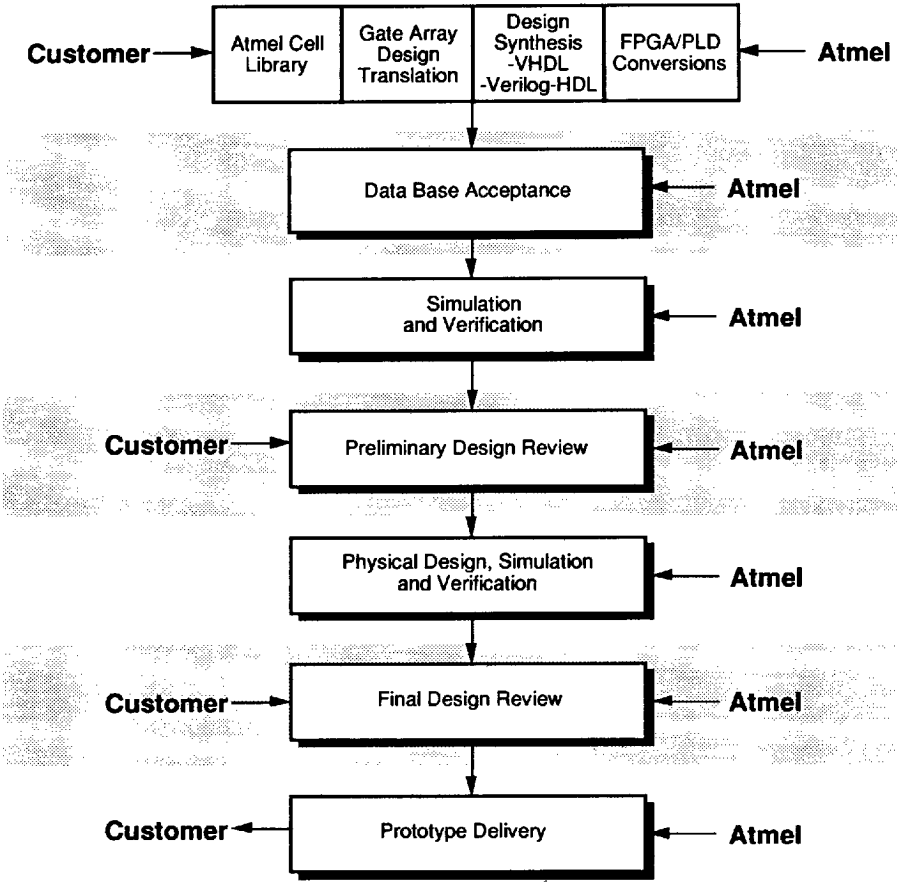
Atmel supports the major CAE/CAD software systems with complete macro cell libraries (symbols, timing and function), as well as utilities for checking the netlist and accurate pre-route delay simulations. Atmel uses Cadence's Verilog-XL as our golden simulator. The following design systems are supported:

Cadence/Composer	Viewlogic
Mentor 8.X	Synopsys

Design Flow

While Atmel provides four options for implementing a gate array design, they all have the same flow. Data base acceptance is the first milestone. This occurs when Atmel receives and accepts the complete design data base. Preliminary design review occurs when the performance of the design is set based on the Cadence simulation. Final design review is the last review of the design before making masks. The back annotation data is incorporated into the simulations. After final design review masks are released and prototypes, in ceramic packages, are delivered.

ATL80 Gate Array Design Flow



Design Options

Schematic Capture

Schematic capture and simulation are performed by the customer using an Atmel supplied macro cell library. The customer can also receive complete back annotation delay data for post-route simulation.

VHDL/Verilog-HDL

Atmel can accept Register Transfer Level (RTL) designs for VHDL (MIL-STD-454, IEEE STD 1076) or Verilog-HDL format. Atmel fully supports Synopsys for VHDL simulation as well as synthesis. Design via VHDL or Verilog-HDL is the preferred method of performing a gate array design.

ASIC Design Translation

Atmel has successfully translated dozens of existing designs from most major ASIC vendors (LSI Logic, Oki, NEC, Motorola, Fujitsu, SMOS, AMI and others) into our gate arrays. These designs have been optimized for speed, gate count, modified to add logic or memory, or replicated for a pin-for-pin compatible, drop-in replacement.

FPGA and PLD Conversions

Atmel has successfully translated existing FPGA/PLD designs from most major vendors (Xilinx, Actel, Altera, AMD and Atmel) into our gate arrays. The design can be optimized for speed or power consumption, modified to add logic or memory or replicated for a pin-for-pin compatible, drop-in replacement. Atmel frequently combines several devices onto a single gate array.

ATL80 Series Cell Library

Atmel's ATL80 series gate arrays use cells from an accurately modeled and highly flexible library. The cell library contains over 120 hard-wired data path elements and has been characterized via extensive SPICE modeling at the transistor level and verified through measurements made on fabricated test arrays. Characterization has been performed over the military temperature and voltage ranges to ensure that the simulation accurately predicts the performance of the finished product. Atmel is continually expanding the ATL80 series cell library with both soft and hard macros. Check with your sales representative for the most recent additions.

Cell Guide

Buffers and Inverters

1x Buffer	1x Inverter
2x Buffer	Dual 1x Inverter
2x Tri-state Buffer	Quad 1x Inverter
2x Tri-state Buffer with Enable Low	Quad Tristate Inverter
3x Buffer	2x Inverter
4x Buffer	2x Tri-state Inverter
8x Buffer	3x Inverter
12x Buffer	4x Inverter
16x Buffer	8x Inverter
Delay Buffer 1.5 ns	10x Inverter
Delay Buffer 2.0 ns	Voltage Level Shifter
Delay Buffer 6.0 ns	Voltage Level Shifter with Power Supply Isolation

AND, NAND, OR, NOR Gates

2 input AND	2 input NOR
2 input AND with High Drive	Dual 2 input NOR
3 input AND	2 input NOR with High Drive
3 input AND with High Drive	3 input NOR
4 input AND	3 input NOR with High Drive
4 input AND with High Drive	4 input NOR
5 input AND	4 input NOR with High Drive
2 input NAND	5 input NOR
Dual 2-input NAND	8 input NOR
2 input NAND with High Drive	2 input OR
3 input NAND	2 input OR with High Drive
3 input NAND with High Drive	3 input OR
4 input NAND	3 input OR with High Drive
4 input NAND with High Drive	4 input OR
5 input NAND	4 input OR with High Drive
5 input NAND with High Drive	5 input OR
6 input NAND	
6 input NAND with High Drive	
8 input NAND	
8 input NAND with High Drive	

Cell Guide

Multiplexers	
2:1 MUX	4:1 MUX
2:1 MUX with High Drive	4:1 MUX w/o Buffered Inputs
Inverting 2:1 MUX w/o Buffered Inputs	4:1 MUX w/o Buffered Inputs, High Drive
Inverting 2:1 MUX w/o Buffered Inputs, High Drive	5:1 MUX with High Drive
2:1 MUX with Enable Low	8:1 MUX
Quad 2:1 MUX with Enable Low	8:1 MUX with Enable Low
Quad 2:1 MUX	8:1 MUX w/o Buffered Inputs High Drive
Inverting 3:1 MUX w/o Buffered Inputs	
Inverting 3:1 MUX w/o Buffered Inputs, High Drive	

AND/OR, OR/AND Gates	
3 input AND OR INVERT	3 input OR AND INVERT
3 input AND OR INVERT with High Drive	3 input OR AND INVERT with High Drive
4 input AND OR INVERT	4 input OR AND INVERT
4 input AND OR INVERT with High Drive	4 input OR AND INVERT with High Drive
4 input AND OR INVERT with 2 inputs to OR	4 input OR AND INVERT with 2 inputs to AND
6 input AND OR INVERT	8 input OR AND INVERT
6 input AND OR INVERT with High Drive	

Exclusive OR/NOR Gates	
1 bit Adder with Buffered Outputs	2 input Exclusive OR with High Drive
7 input Carry Lookahead	2 input Exclusive NOR
2 input Exclusive OR	2 input Exclusive NOR with High Drive

Decoders	
2:4 Decoder	3:8 Decoder with Enable Low
2:4 Decoder with Enble Low	

Flip-flops/Latches	
D Flip-flop	LATCH
D Flip-flop with Clear/Preset	LATCH with Complementary Outputs and Inverted Gate Signal
D Flip-flop with Clear	LATCH with High Drive Complementary Outputs
D Flip-flop with Reset	LATCH with Reset
D Flip-flop with Set	LATCH with Set
D Flip-flop with Set/Reset	LATCH with Set and Reset
JK Flip-flop	
JK Flip-flop with Clear	
JK Flip-flop with Clear/Preset	

Cell Guide

Scan Cells	
Set-scan Flip-flop Set-scan Flip-flop with Reset Set Scan Flip-flop with Set	Set Scan Flip-flop with Set and Reset Set Scan Flip-flop with Preset

I/O Options
Input, Output, Bidirectional, Tristate Output, Internal Clock Driver and Oscillator
Output Drive Value Programmable from 2 mA to 24 mA in 2 mA increments with Slew Rate Control
CMOS or TTL Operation
Schmitt Trigger (Bidirectional, Input)
Inverting and Non-inverting Input Buffers (Bidirectional, Input)
Pullup Resistor - 12K Ω to 372K Ω
Pulldown Resistor - 3.5K Ω to 108.5K Ω

74XX Series Soft Macros
24 cells available

CMOS/TTL Input Interface Characteristics

Interface	Logic High	Logic Low	Switchpoint
CMOS	3.5 V Minimum	1.5 V Maximum	$V_{DD}/2$ Typical
TTL	2.0 V Minimum	0.8 V Maximum	1.4 V Typical

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Maximum Operating Voltage	6.0 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{DD} + 0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

5.0 Volt DC Characteristics

Applicable over recommended operating range from T_a = -55°C to +125°C, V_{DD} = 4.5 V to 5.5 V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
I_{IH}	Input Leakage High	$V_{IN} = V_{DD}$, V_{DD} = 5.5 V		0.01	10	µA
I_{IL}	Input Leakage Low (no pull-up) 108K Ω pull-up (U9)	$V_{IN} = V_{SS}$, V_{DD} = 5.5 V $V_{IN} = V_{SS}$, V_{DD} = 5.5 V	-10 -125	-0.01 -50	 -20	µA µA
I_{OZ}	Output Leakage (no pull-up)	$V_{IN} = V_{DD}$ or V_{SS}, V_{DD} = 5.5 V	-10	0.01	10	µA
V_{IL}	TTL Input Low Voltage				0.8	V
V_{IL}	CMOS Input Low Voltage				0.3 x V_{DD}	V
V_{IH}	TTL Input High Voltage		2.0			V
V_{IH}	CMOS Input High Voltage		0.7 x V_{DD}			V
V_T	TTL Switching Threshold CMOS Switching Threshold	V_{DD} = 5.0 V, 25°C V_{DD} = 5.0 V, 25°C		1.4 2.4		V V
V_{OL}	Output Low Voltage Output buffer has 12 stages of drive capability with 2 mA I_{OL} per stage.	I_{OL} = as rated V_{DD} = 4.5 V		0.2	0.4	V
V_{OH}	Output High Voltage Output buffer has 12 stages of drive capability with -2 mA I_{OH} per stage.	I_{OH} = as rated V_{DD} = 4.5 V	0.7 x V_{DD}	4.2		V
I_{OS}	Output Short Circuit Current (3 x Buffer)(2)	V_{DD} = 5.5 V, $V_{OUT} = V_{DD}$ V_{DD} = 5.5 V, $V_{OUT} = V_{SS}$	10 -100	50 -50	100 -10	mA mA

Note: 2. This is the specification for the 3 x Output Buffer. Output short circuit current for other outputs will scale accordingly. Not more than one output shorted at a time, for a maximum of one second, is allowed.

3.3 Volt DC Characteristics

Applicable over recommended operating range from T_a = -55°C to +125°C, V_{DD} = 3.0 V to 3.6 V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
I_{IH}	Input Leakage High	$V_{IN} = V_{DD}$, V_{DD} = 3.6 V		0.01	10	µA
I_{IL}	Input Leakage Low (no pull-up)	$V_{IN} = V_{SS}$, V_{DD} = 3.6 V	-10	-0.01		µA
	108K Ω pull-up (U9)	$V_{IN} = V_{SS}$, V_{DD} = 3.6 V	-90	-35	-15	µA
I_{OZ}	Output Leakage (no pull-up)	$V_{IN} = V_{DD}$ or V_{SS}, V_{DD} = 3.6 V	-10	0.01	10	µA
V_{IL}	CMOS Input Low Voltage				0.3 x V_{DD}	V
V_{IH}	CMOS Input High Voltage		0.7 x V_{DD}			V
V_T	CMOS Switching Threshold	V_{DD} = 3.3 V, 25°C		1.5		V
V_{OL}	Output Low Voltage Output buffer has 12 stages of drive capability with 1 mA I_{OL} per stage.	I_{OL} = as rated V_{DD} = 3.0 V			0.4	V
V_{OH}	Output High Voltage Output buffer has 12 stages of drive capability with -1 mA I_{OH} per stage.	I_{OH} = as rated V_{DD} = 3.0 V	0.7 x V_{DD}			V
I_{OS}	Output Short Circuit Current (3 x Buffer)(2)	V_{DD} = 3.6 V, $V_{OUT} = V_{DD}$ V_{DD} = 3.6 V, $V_{OUT} = V_{SS}$	5 -60	25 -25	60 -5	mA mA

Note: 2. This is the specification for the 3 x Output Buffer. Output short circuit current for other outputs will scale accordingly. Not more than one output shorted at a time, for a maximum of one second, is allowed.

I/O Buffer DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
C_{IN}	Capacitance, Input Buffer (Die)	5.0 V, 3.3 V		2.4		pF
C_{OUT}	Capacitance, Output Buffer (Die)	5.0 V, 3.3 V		5.6		pF
$C_{I/O}$	Capacitance, Bi-Directional	5.0 V, 3.3 V		6.6		pF
Schmitt Trigger						
V+	TTL Positive Threshold	25°C, 5.0 V		1.8	2.0	V
	CMOS Positive Threshold	25°C, 5.0 V		3.2	3.5	V
V-	TTL Negative Threshold	25°C, 5.0 V	0.8	1.0		V
	CMOS Negative Threshold	25°C, 5.0 V	1.0	1.2		V
ΔV	TTL Hysteresis	25°C, 5.0 V	0.5	0.8		
	CMOS Hysteresis	25°C, 5.0 V	1.0	2.0		
V+	CMOS Positive Threshold	25°C, 3.3 V		2.0	2.4	V
V-	CMOS Negative Threshold	25°C, 3.3 V	1.0	1.3		V
ΔV	CMOS Hysteresis	25°C, 3.3 V	0.5	0.7		

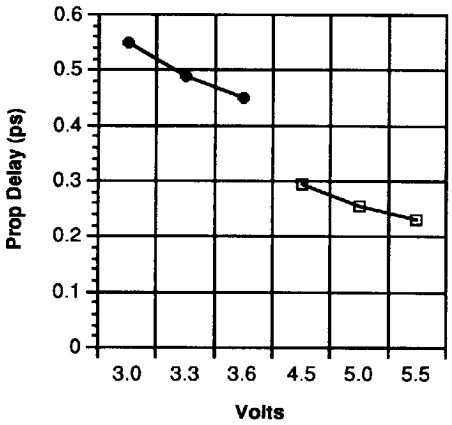
I/O Buffers

- Programmable output drive
  (2 to 24 mA I_{OL}, -2 to -24 mA I_{OH} for 5.0 V
  1 to 12 mA I_{OL}, -1 to -12 mA I_{OH} for 3.3 V)
- 3,000 volts ESD protection
- Built-in configurable test logic

The ATL80 series input/output ring contains the I/O buffer circuitry capable of sourcing and sinking currents up to 24 mA, and responds to CMOS or TTL logic levels. All outputs can be switched to a high impedance state. I/O locations on this ring can accommodate bidirectional cells.

AC Characteristics

Delay vs V_{CC}

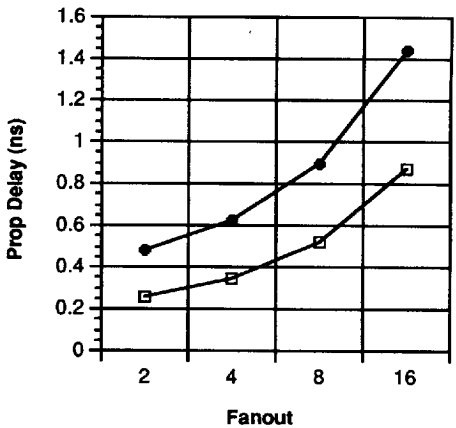


3.3 Volts V_{dd}

5.0 Volts V_{dd}

2 input NAND
Temp = 25°C
FO = 2

Delay vs Fanout

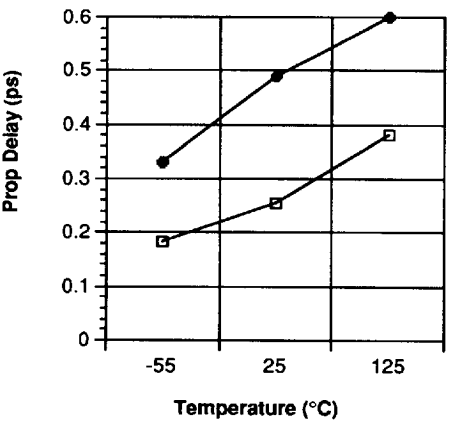


3.3 Volts V_{dd}

5.0 Volts V_{dd}

2 input NAND
Temp = 25°C

Delay vs Temperature

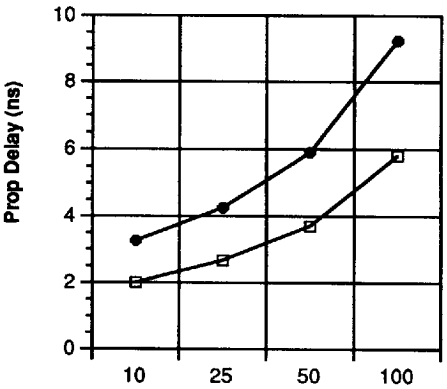


3.3 Volts V_{dd}

5.0 Volts V_{dd}

2 input NAND
FO = 2

Output Buffer vs Load



3.3 Volts V_{dd}

5.0 Volts V_{dd}

PDO4 - Output Buffer 8 mA
Temp = 25°C

Design for Testability

Atmel supports a full range of Design-for-Test improvement techniques which reduce design and prototype debug time, production test time, and board and system test time. These techniques can also improve system level test and diagnostic capability.

The ATL80 arrays support the Joint Test Action Group (JTAG) boundary scan architecture. The required soft and hard macros to implement IEEE 1149.1 compliant architecture are available in our macro cell library. Use of JTAG allows for scan testing with only 4-5 additional pins required.

Atmel can also provide automatic high fault coverage test pattern generation (ATPG) via Synopsys Test Compiler. By following a set of design rules, Test Compiler can automatically insert the scan cells and generate test vectors providing greater than 95% fault coverage. This is the easiest and least expensive method for designing testability into a gate array design.

Advanced Packaging

Atmel supports a wide variety of standard packages for the ATL80 series, but also offers its ATL80 series gate arrays in packages that are custom designed to maintain the performance obtained in the silicon.

All of Atmel's standard packages have been characterized for thermal and electrical performance. When a standard package can't meet a customer's needs, Atmel's package design center can develop a package to precisely fit the application. The company has delivered custom-designed packages in a wide variety of configurations.

Packaging Options

Package Type	Pin Count
PQFP	44, 52, 64, 80, 100, 120, 128, 132, 144, 160, 184, 208, 240, 304
TQFP	44, 48, 52, 64, 80, 100, 120, 128, 144, 160, 176, 216
PLCC	20, 28, 32, 44, 52, 68, 84
CPGA	64, 68, 84, 100, 124, 144, 155, 180, 223, 224, 299, 391
CQFP	64, 68, 84, 100, 120, 132, 144, 160, 224, 340
BGA	121, 169, 225, 313

Military Product Flow Chart

MIL-STD-883 Class B