

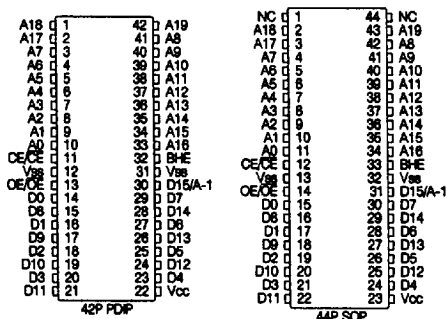
DESCRIPTION

The HY2316050 is a 16Mbit mask-programmable ROM organized either as 2,097,152 x 8bit (Byte mode) or as 1,048,576 x 16bit (Word mode) depending on BHE level. It is fabricated using HYUNDAI's advanced CMOS process technology. The HY2316050 operates with a 5V power supply and all inputs are TTL compatible. It satisfies user option modes with the polarity-programmable $\overline{CE}$ and $\overline{OE}$. It is designed to be compatible with all microprocessors and similar applications where high-performance large-bit storage and simple interfacing are important design considerations.

FEATURES

- High speed- 120ns (Normal Mode)
- 50ns (Page Mode)
- 8 Word Page in 16bit Mode
- 16 byte Page in 8bit Mode
- User-Switchable x8 / x16 Organization
- Power Consumption (max.)
- Operating : 60mA
- Standby (CMOS) : 50 μ A
- Polarity-Programmable Pins
- $\overline{CE}/\overline{CE}^*$, $\overline{OE}/\overline{OE}^*$
- TTL compatible Inputs and outputs
- Tri-state output
- Packages :
- 42 pin 600 mil PDIP
- 44 pin 600 mil SOP

PIN CONNECTION

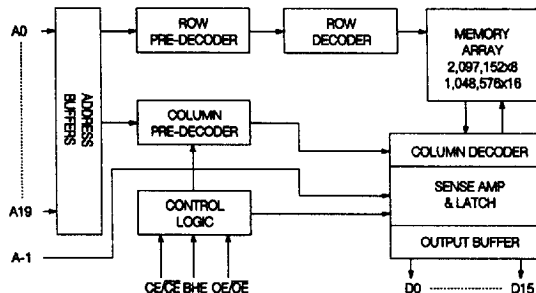


PIN DESCRIPTION

Pin Name	Pin Function
A0-A19	Address Inputs
D0-D15	Data Outputs
BHE	Byte/Word select
D15/A-1	Output D15 (Word mode)/ LSB Address (Byte mode)
$\overline{CE}/\overline{CE}^*$	Chip Enable
$\overline{OE}/\overline{OE}^*$	Output Enable
Vcc	Power
Vss	Ground

* User Selectable Polarity

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TBIAS	Temperature under BIAS	-10 to 85	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN	Voltage on Any Pin Relative to Vss	-0.5 to 7.0	V
VCC	Voltage on VCC Relative to Vss	-0.5 to 7.0	V

Note:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA= 0°C to 70°C, VCC= 5V ± 10%, Vss=0V)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Power Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.2	-	Vcc+0.5	V
VIL	Input Low Voltage	-0.5	-	0.8	V

TRUTH TABLE

MODE	CE/CE	OE/OE	BHE	D15/A-1	DATA	OPERATION
Non-Selected	L/H	X	X	X	High-Z	Standby
Output Disabled	H/L	L/H	X	X	High-Z	Active
Read	H/L	H/L	H	Output	D0-D15	Active
			L	Input	D0-D7	Active

Note: X=L or H

DC CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
I _{LI}	Input Leakage Current	V _{IN} = 0 to V _{CC}	-	10	μA
I _{LO}	Output Leakage Current	V _{OUT} = 0 to V _{CC}	-	10	μA
I _{CC}	Operating Current	ALL DOUT = open, f = 8.3MHz, CE = OE = V _{IL}	-	60	mA
I _{SB1}	Standby Current (TTL)	CE = V _{IH} , ALL DOUT = open	-	1	mA
I _{SB2}	Standby Current (CMOS)	CE = V _{CC} , ALL DOUT = open	-	50	μA
V _{OH}	Output High Voltage	I _{OH} = -400μA	2.4	-	V
V _{OL}	Output Low Voltage	I _{OL} = 2.0mA	-	0.4	V

Note: All Voltages are referenced to V_{SS}

AC CHARACTERISTICS

(TA=0°C to 70°C, VCC=5V ±10%, unless otherwise noted.)

#	SYMBOL	PARAMETER	HY2316050		UNIT
			MIN.	MAX.	
1	t _{RC}	Read Cycle Time	120	-	ns
2	t _{PC}	Page Read Cycle Time	50	-	ns
3	t _{ACC}	Address Access Time	-	120	ns
4	t _{PAC}	Page Address Access Time	-	50	ns
5	t _{OH}	Output Hold from Address Change	0	-	ns
6	t _{CE}	Chip Enable Access Time	-	120	ns
7	t _{OE}	Output Enable Access Time	-	50	ns
8	t _{DF}	Output or Chip Disable to Output High-Z	-	20	ns

AC TEST CONDITIONS

(TA=0°C to 70°C, VCC=5V ±10%)

PARAMETER	VALUE
Input Pulse Level	0.6 to 2.4V
Input Rise and Fall Time	10ns
Output Timing Level	0.8V and 2.0V
Output Load	1TTL Gate and C _L = 100pF

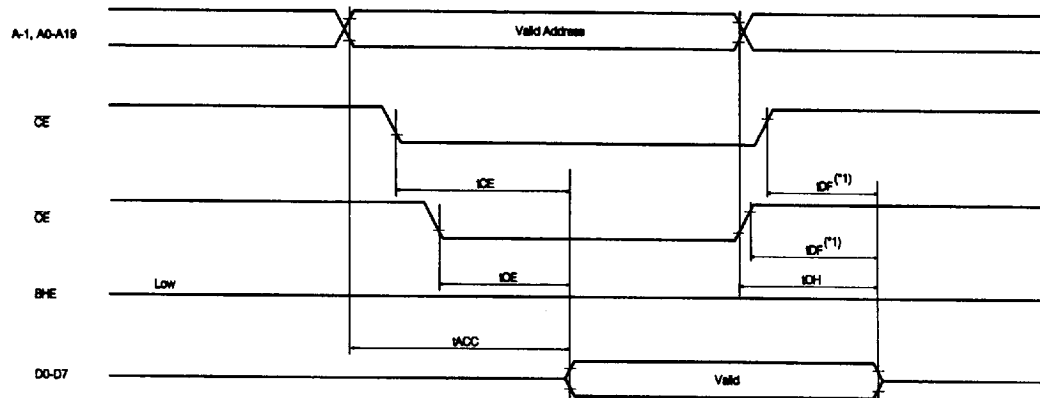
CAPACITANCE

(TA=25°C, f=1MHz, VCC=5V ±10%)

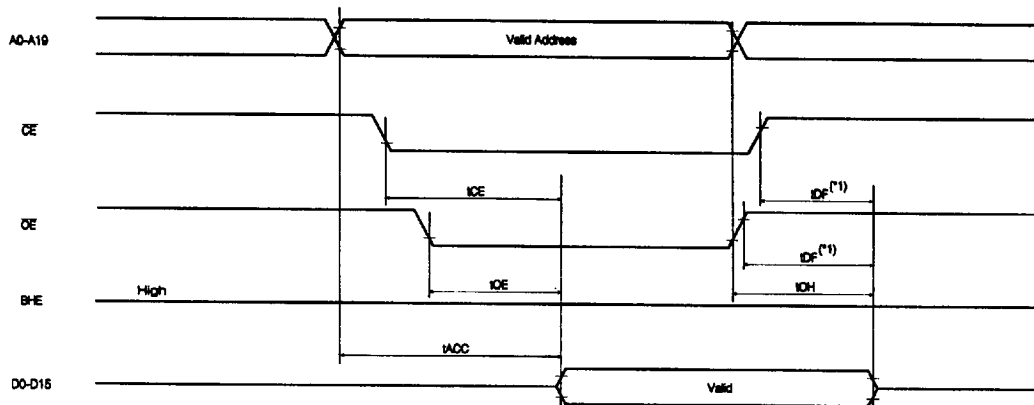
SYMBOL	PARAMETER	TEST CONDITION	TYPE	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = 0V	-	15	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	-	15	pF

TIMING DIAGRAM

READ CYCLE



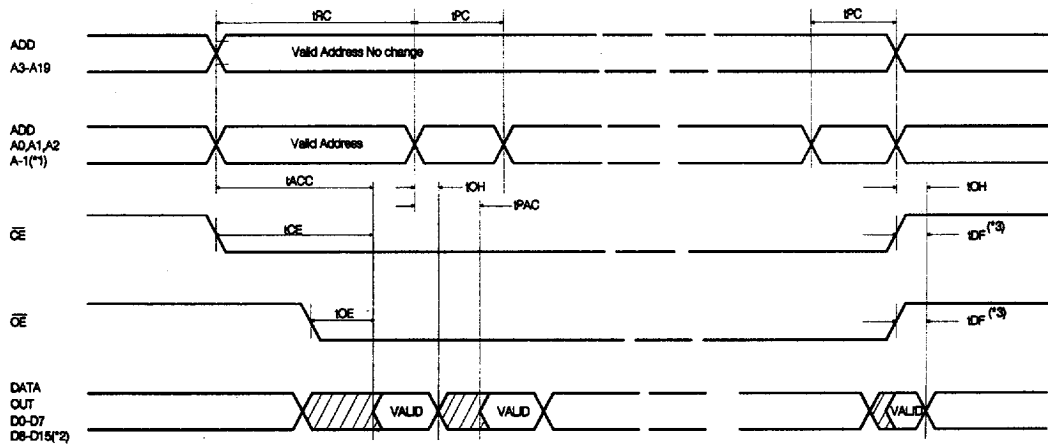
8 BIT RANDOM READ



(*1) t_{OF} is defined as the time which the outputs achieve the open circuit condition and is not referenced to V_{OH} or V_{OL} Level.

16 BIT RANDOM READ

TIMING DIAGRAM



NOTES

(*1) Byte Mode only A-1 is least significant Bit Address (BHE=VIL)

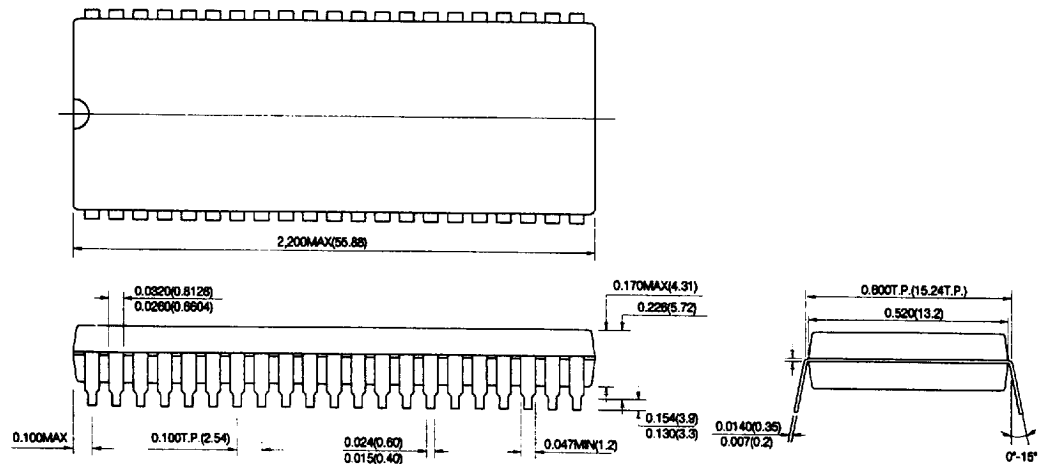
(*2) Word Mode only (BHE=VIH)

(*3) t_{Df} is defined as the time which the outputs achieve the open circuit condition and is not referenced to V_{OH} or V_{OL} Level.

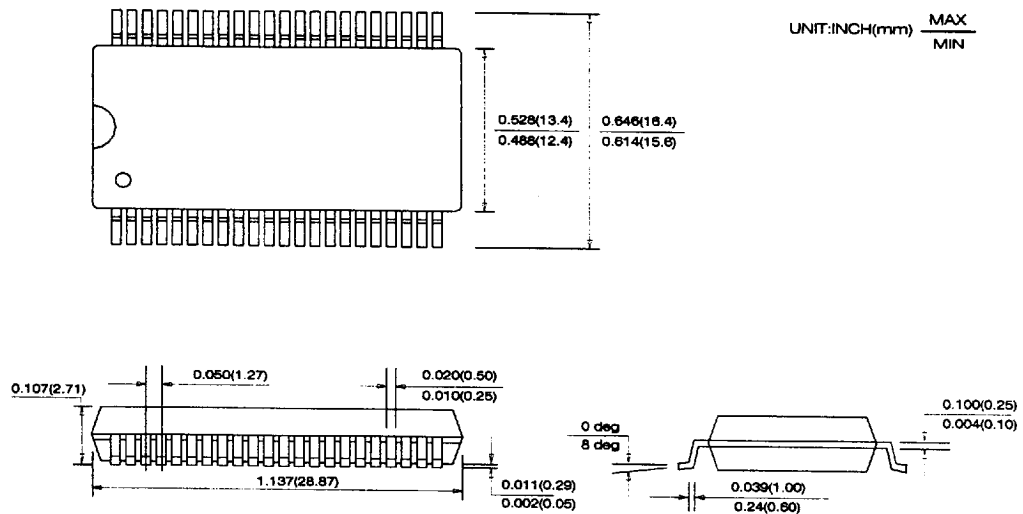
PAGE MODE

PACKAGE INFORMATION

42 Pin Plastic Dual In-Line Package - 600mil (P)



44 Pin Plastic Small Outline Package - 600mil (G)



ORDERING INFORMATION

PART NO	SPEED	PACKAGE
HY2316050P	120/50 ns	42P PDIP
HY2316050G	120/50 ns	44P SOP