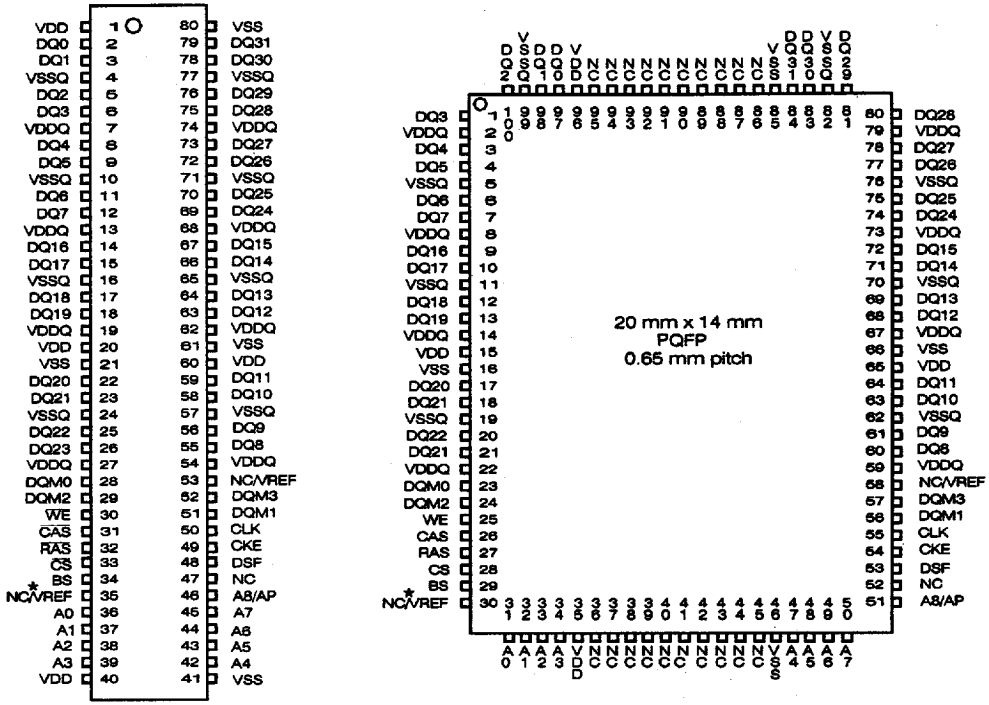
Introduction

Overview

The eight megabit Synchronous Graphics RAM (SGRAM) is a single port, application specific memory device designed for graphics applications. It is organized as 128K words per bank x 32 bits per word x 2 banks. Internally, the SGRAM is organized as two separate banks, each comprising 512 rows x 256 columns x 32 bits per data word. To refresh the SGRAM, the 512 rows of each bank. 1024 rows in total, must be accessed within every 16 millisecond refresh interval. The synchronous interface of the SGRAM is similar to that of Synchronous DRAMs (SDRAMs) and is designed to achieve very high data rates. For a wide range of workstation and personal computer applications, the single 32 bit data port delivers sufficient bandwidth to refresh a video display while concurrently allowing rapid updates of the frame buffer by a graphics controller device.

Features

- **Fully synchronous. All signals referenced to a positive clock edge.**
- **Up to 100 MHz frequency operation.**
- **Dual Banks for continuous high speed data streams.**
- **Separate byte enable signals facilitate byte read and wite operations.**
- **Persistent Write Per Bit(WPB) operation allows individual write control to each I/O.**
- **8x8(x4) Block Write allows as many as 256 bits of data to be written in every t_{BWC} period.**
- **Single 3.3 V power supply.**
- **Supports JEDEC standard low voltage TTL(LVTTL) interface.**
- **Programmable three stage pipeline delivers best trade off between peak data rate and read latency.**
- **Programmable burst length (1, 2, 4, 8, full page).**
- **Supports change of column address on consecutive read or write cycles.**
- **Incrementing burst mode delivers high speed video and increases flexibility for various draw algorithms.**
- **Automatic Precharge simplifies control.**
- **Auto Refresh using an on chip refresh counter and toggle bank select. 1024 cycle, 16 ms refresh.**
- **Self Refresh provides minimum power, full internal refresh control.**
- **Two high density package options:**
  - **80 pin, 400mil wide TSOP II**
  - **100 pin, 20mm x 14mm Plastic Quad Flat Pack.**
- **Compatible with emerging JEDEC standards.**



Pin	Description
A7-A0	Row and Column Address
A8/AP	Row Address / Auto Precharge Flag
BS	Bank Select & Column Address
DQ31-DQ0	Input / Output and Write Per Bit Mask
CLK	System Clock
CKE	Clock Enable
CS	Chip Select
RAS	Row Address Strobe
CAS	Column Address Strobe

Pin	Description
WE	Write Enables
DQM3-DQM0	Data Byte Mask Enable
DSF	Special Function Select
VDD	Supply Voltage, 3.3 volts
VDDQ	Supply Voltage, Q Outputs, 3.3v
VSS	Ground
VSSQ	Ground, Q Outputs
NC	No Connect
* VREF	Input Reference Voltage (HSTL, LVCTT Interface)

Figure 1. Pin Diagrams and Nomenclature.

Note : * Future Version.

Terms and Conventions

IOi, DQi, planei : The individual I/Os comprising the 32 bit DRAM port. DQi may also be used to refer to the specific package pin corresponding to I/Oi(planei).

byte 0 refers to data stored in or accessed from DQ7-DQ0.
byte 1 refers to data stored in or accessed from DQ15-DQ8.
byte 2 refers to data stored in or accessed from DQ23-DQ16.
byte 3 refers to data stored in or accessed from DQ31-DQ24.

write mask, or write mask register: A register comprising 32 bits, each bit controlling a write operation to one of the 32 planes. In write per bit mode, write mask bit i enables or disables a write operation to IOi (planei). The write mask is thus a write control register.

signal(CLK): The state of *signal* when CLK goes high.

address mask, column mask, or column address mask: The mask formed by DQ0-DQ7 for byte 0,DQ8-DQ15 for byte 1, DQ16-DQ23 for byte 2, and DQ24-DQ31 for byte 3 which replaces the column address bits A0-A3 during Block Write operations. The address mask contains only *address* information.

A signal is said to be **asserted** when it is in its active state, regardless if the signal is active high or active low. A signal is said to be **negated** if it is in its inactive state, regardless if the signal is active high or active low.

long word: the 32 bits of data, DQ0-DQ31, corresponding to a single memory address.

don't care state: designates that a signal can be in either the logic low state (≤ a specified minimum voltage) or in the logic high state(≥ a specified maximum voltage).

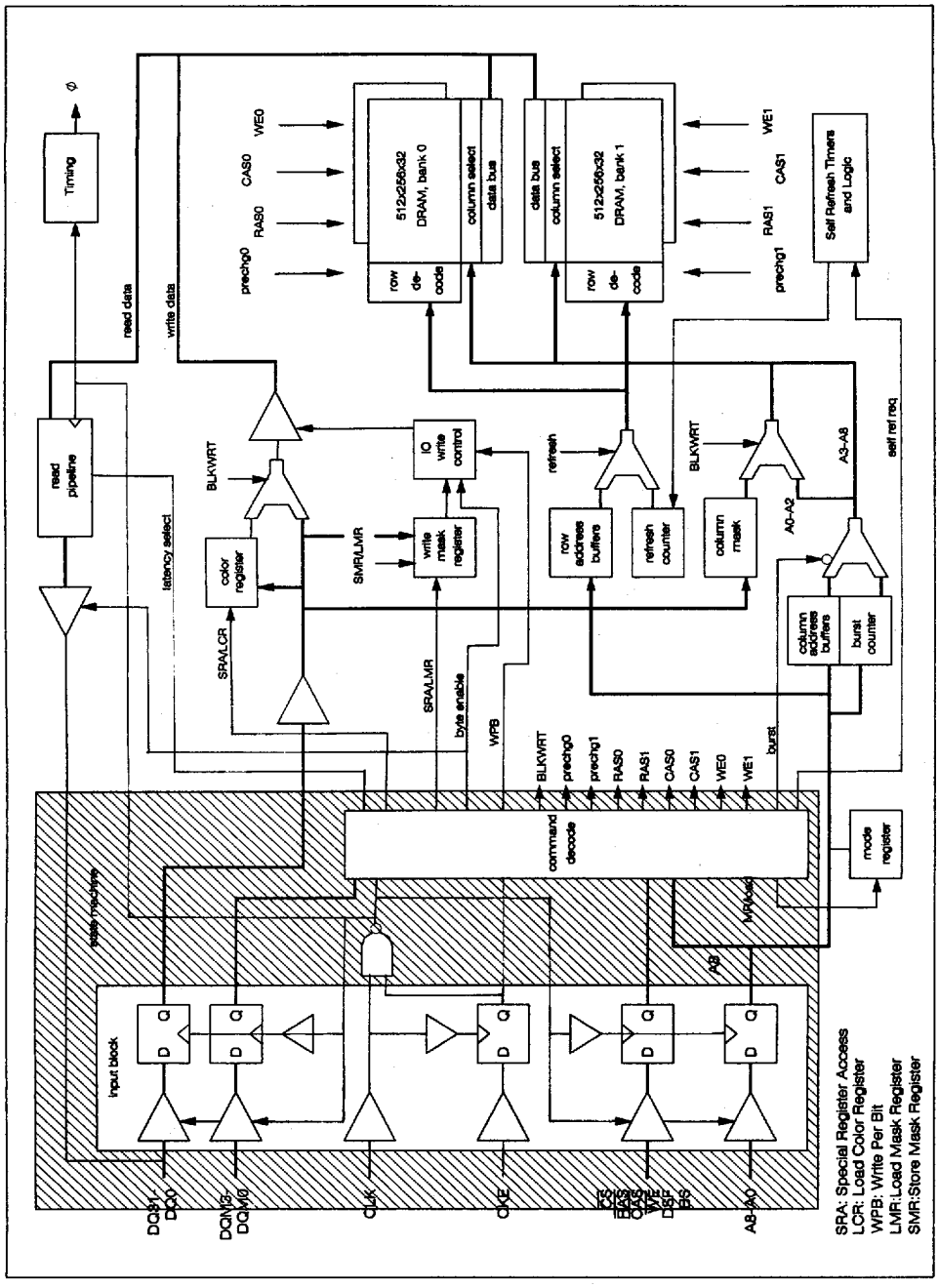


Figure 2. Top level block diagram of the 8 Mb SGRAM.

Architecture

Detailed Pin Descriptions

CLK (system clock); clock, input

CLK is the main system clock input. All other inputs are registered to the SGRAM on the rising edge of CLK. There is one exception to this. If the Clock Enable input, CKE, is asserted while CLK has been disabled, then CLK is re-enabled asynchronously by CKE. Output data on DQ can change only after the rising edge of CLK.

BS (Bank Select); address, input

The SGRAM is comprised of two separate banks of memory, none, one, or both of which can be active at any given time. When bank activate, read, write, read(or write) with auto precharge, or precharge commands are invoked within a single bank, BS selects which bank the command is executed on. BS=0 selects Bank 0 and BS=1 selects Bank1. BS is used in conjuction with A8/PC during precharge command invokation. When A8/PC=0, BS selects one of the two banks for precharge. When A8/PC=1, BS is ignored and both banks are selected for precharge. BS is also used as an op code bit during Mode Register and Special Register operations. The Mode Register operation is used to select $\overline{CAS}$ latency (the number of clock cycles after a read command is issued before the first bit of data is available), burst length, and burst type. It is also used to select certain internal test modes to be used by Hyundai test engineers. The Special Register operation is used to load the color register and write per bit mask register for use during write and block write cycles.

A8/PC, A7-A0 (address); address, input

Seventeen address bits of information are required to decode one of 128K memory addresses for each bank. The address is divided into a 9-bit row address and an 8-bit column address. The row address is presented on A8/PC and A7-A0 on the rising edge of CLK during row activate commands. The column address is presented on A7-A0 on the rising edge of CLK during read, write, and block write commands. During read and write commands, A8/PC selects / deselects auto precharge. The auto precharge feature is not supported for block write commands. A8/PC=0 deselects auto precharge and A8/PC=1 selects auto precharge. During precharge commands, A8/PC=0 causes the bank selected by BS to be precharged while A8/PC=1 unconditionally causes both banks to be precharged.

DQ31-DQ0 (RAM data); data, IO; address(block write), input

During normal DRAM operations, DQ31-DQ0 provide the datapath into and out of RAM. Depending on the $\overline{CAS}$ latency selected, data from the selected memory address is delivered to DQ31-DQ0 within one, two, or three clock cycles. DQ31-DQ0 return to tristate independent of the state of DQMi(see below) during the clock cycle following any of the following events:

1. The last bit in the read burst has been output
2. A terminate burst command is invoked.
3. A write command is invoked to either bank.

DQM3- DQM0 are used as separate read enables for the four bytes comprising DQ31-DQ0.

During write cycles, DQ31-DQ0 provide the data to be written to RAM. During block write cycles, DQ31-DQ0 serve as address selects to DRAM locations to be written with the contents of the on chip color register. During Special Register operations, DQ31-DQ0 provide data to be written to the color register or provide write mask bits to be written to the write per bit mask register.

CKE(clock enable); control, input

The state of CKE is input to the SGRAM on each rising edge of CLK. As long as CKE remains asserted (high) during clock cycles, the SGRAM can perform row activate, read, write, block write, precharge, auto refresh, Mode Register, or Special Register operations. When CKE is first negated during the rising edge of CLK (called a clock disable cycle), the SGRAM can enter one of three modes of operation, depending on the current state of the SGRAM and the values of the $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ inputs at that time.

If both banks of the SGRAM are idle (i.e., in the precharged state) during clock disable, the SGRAM will enter either a power down state or a self refresh state, depending on the values of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$. Once in the power down state, the SGRAM will consume minimum power, and no other cycles can be initated until power down mode is exited. Once in self refresh mode, the SGRAM will continually cycle through the 512 rows in each bank, refreshing the entire DRAM. Once in self refresh mode, no other cycles can be executed except to exit refresh mode and return to an idle state.

If one or both banks of the SGRAM are active, the SGRAM will enter clock suspend mode. During clock suspend mode, all clock cycles to the SGRAM will be treated internally as NOPs (No Operation), and the active banks(s) will remain active. For details on the various states and cycles involving CKE, see Table 2.

$\overline{CS}$ (chip select); control, input

During most normal operating states (that is, not self refresh or power down), $\overline{CS}$ serves as a general device select. Accordingly, when $\overline{CS}$ is asserted (low) at the positive edge of CLK, the SGRAM is enabled and the cycle defined by $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DSF, BS, and A8/PC is invoked. When $\overline{CS}$ is negated during the positive edge of CLK, the SGRAM performs a NOP, whereby the state of the SGRAM does not change except that any burst read or burst write in progress continues. The state of $\overline{CS}$ can also be used to enter and exit self refresh and power down modes. See Table 2 for details.

$\overline{RAS}$ (row address strobe); control, input

$\overline{RAS}$ is a control input used in conjunction with the other control inputs to define a new command to be executed and a new state to be entered within the SGRAM. When asserted on the positive edge of CLK, $\overline{RAS}$ is generally used to activate a new row in one of the two banks or to precharge one or both banks. $\overline{RAS}$ can also be asserted in conjunction with other control inputs when CKE is negated to select between entering power down mode and entering self refresh mode. See Table 2 for details.

$\overline{CAS}$ (column address strobe); control, input

$\overline{CAS}$ is a control input which functions as a new column address select. $\overline{CAS}$ is asserted in conjunction with other control inputs to latch a new column address (A7-A0) and activate a read or write command, $\overline{CAS}$ can also be asserted in conjunction with the other control inputs to invoke Mode Register, Special Register, and auto refresh operations. See Table 2 for details.

$\overline{WE}$, (write enable, write per bit select); control, input

$\overline{WE}$ is asserted in conjunction with $\overline{CAS}$ to invoke write and block write cycles to the selected column. $\overline{WE}$ is also asserted in conjunction with other control inputs to invoke Mode Register, Special Register, Bank Precharge, and Terminate Burst commands. See Table 2 for details.

DQM3-DQM0(read and write data mask byte enable); control, input

DQM3, DQM2, DQM1, and DQM0 act as read and write byte enables for byte 3, byte 2, byte 1, and byte 0 respectively. If DQMi is held high at the positive edge of CLK during read or burst read cycles, all of the data outputs associated with bytei will go to tristate after a latency of two clock cycles (i.e., the outputs will go to tristate during the clock cycle following the clock cycle in which DQMi was high, independent of the $\overline{CAS}$ read latency setting).

If DQMi is held high at the positive edge of CLK during write or burst write cycle, the data supplied to the inputs associated with bytei, during *that* cycle will not be written to the DRAM. Table 1 below shows the state assignments associated with DQM.

Current State	DQMi	$\overline{CS}$	Action
Read	L	H	Enable output, bytei
Read	H	H	Disable output, bytei
Write	L	H	Enable write to bytei
Write	H	H	Disable write to bytei

Table 1. State and Function Truth Table for DQM3-DQM0

DSF (special function select); control, input

DSF is used in conjunction with other control inputs to invoke Special Mode Register set cycles (for the purpose of loading the write per bit mask and color registers), write per bit, and block write operations. See Table 2 for details.

VREF (HSTL, LVCTT input reference voltage); input (Future Version)

VREF is the input reference voltage used to implement either the HSTL or the LVCTT terminated load voltage interface. VREF is the reference voltage used by the internal input buffers of the SGRAM and compared to the input voltage supplied to those input buffers via the device pins. Voltages on the input pins which are more positive than VREF(by a designated margin) are interpreted as input high levels. Voltages on the input pins which are more negative than VREF(by a designated margin) are interpreted as input low levels.

Description of Functional Units

The block diagram shown in Figure 2 should be referenced for discussions of the major functional blocks.

Input Block

All inputs to the SGRAM are registered at the positive edge of the system clock CLK. Two separate internal clock systems exist, one gated by the clock enable signal CKE and the other ungated. The gated clock system controls the various internal blocks, including RAM bank access, the state machine, and the read/write paths. The ungated clock is used to strobe the CKE input master slave DQ flip flop so that the gated internal clock can be internally disabled and re-enabled. The latched address, data, and control inputs are input to the state machine and command decode to select and control a cycle to be executed.

Command Decode and State Machine

The Command Decode consists of state registers and an instruction decoder. The Command Decode combines with the registered input block to form the state machine of the SGRAM. The state machine accepts new control inputs from the input block on each cycle to selectively change the state of the state machine and issue a new command to the SGRAM according to Table 2.

Mode Register

The mode register is a ten bit register used to program the $\overline{CAS}$ latency for burst read operations and the burst length for read and write bursts. The mode register is loaded using the address pins, A8/PC-A0, plus the bank select input BS during Mode Register Access operations. See Table 2 for details on invoking a Mode Register access. The mode register is shown in Figure 7.

Programmable Pipeline

To optimize performance for a wide variety of applications, the SGRAM has a programmable pipeline which adjusts the number of stages, and thus the access latency of data read from DRAM. The SGRAM can be programmed via a Mode Register Access to one, two, or three cycles of latency relative to CLK. Figure 7 shows how the three possible latencies for read and write operation are programmed via the mode register. Higher latency allows faster clock cycles to be used, which for relatively long data bursts results in substantial bandwidth improvements.

Write Mask Register

The write mask register is a 32 bit register used to control the internal write enables to each IO, or plane, in RAM. The write mask register is loaded during a Special Register "Load write Mask Register" (LMR). Once a Load Mask Register cycle is executed, the SGRAM goes into "persistent" write per bit mode, and will use the contents of the write mask on every write per bit write cycle thereafter until another LMR cycle is excuted.

Color Register

The color register is a 32 bit register used as an alternate data source during block write operations. The register is loaded from the DQi inputs during Special Register "Load Color Register" (LCR) cycles and is used as data during block write cycles. Once loaded, the color register cannot be altered except by another LCR cycle.

Column Address Mask

During block write cycles, A8-A3 select a group of eight contiguous columns for write operation using the color register as the data source. The column mask is loaded from the DQ inputs at write time and is used to enable any arbitrary subset of these eight columns in RAM to be written using the contents of the color register. Separate 8-bit masks are loaded on DQ7-0, DQ15-8, DQ23-16, and DQ31-24, meaning that the subset of columns written to memory can be different for each byte. The column mask can be changed during each $\overline{CAS}$ cycle.

Refresh Counter

The Refresh Counter is a 10-bit counter used for auto refresh and self refresh operations. During refresh cycles, the refresh counter is input to the row decoder instead of the outputs of the row address buffers. The refresh counter increments after each refresh cycle, cycling through all 512 rows of each bank, or 1024 rows in total. Refresh is performed in a ping pong manner between DRAM banks. That is, refresh cycles will alternate between bank 0 and bank 1 on successive refresh cycles.

Timing

The timing block contains the various clock and control signals used to perform the various functions of the SGRAM. These signals are generally referenced to the input CLK signal and control addressing, sensing, and the read and write datapaths within the SGRAM.

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
Voltage on VDD, VDDQ pins relative to ground	-1.0 to 4.6	V
Voltage on input pin relative to ground	-1.0 to 4.6	V
Voltage on input /output pin relative to ground	-1.0 to 4.6	V
Short circuit output current	50	mA
Power Dissipation	1.1	W
Operating termperature (ambient)	0 to 70	°C
Storage temperature (plastic package)	-55 to 125	°C

1. Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage, Vcc	3.0	3.3	3.6	V
V_{DDQ}	Supply voltage, VccQ (data outputs)	3.0	3.3	3.6	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.0		Vcc + 0.3	V
V_{IL}	Low-level input voltage	-0.3		0.8	V
T_A	Operating free air ambient temperature	0		70	°C
C_L	External load capacitance on DQ			30	pF

PIN CAPACITANCE VALUES

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
C_{IC}	Input capacitance: CLK, CKE, $\overline{RAS}$, $\overline{CAS}$, $\overline{CS}$, $\overline{WE}$, DSF, DQM	2		4	pF
C_{IA}	Input capacitance; BS, A8/PC, A7-A0	2		4	pF
$C_{I/O}$	Input / Output capacitance: DQ	2		5	pF

DC ELECTRICAL CHARACTERISTICS

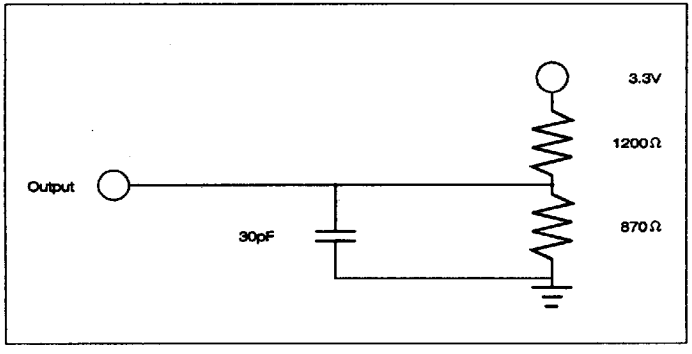
SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
V_{OH}	High - level output voltage	I_{OH} = -2 mA	2.4		V
V_{OL}	Low - level output voltage	I_{OL} = 2 mA		0.4	V
I_L	Input leakage current	0 ≤ Vin ≤ 4.0V All other pins at ground	-10	+10	µA
I_{OZ}	Output leakage current	0 ≤ Vout ≤ V_{DD}, DQ disabled	-10	+10	µA

OPERATING CURRENTS

Parameter	V_{IL} / V_{IH} unless otherwise noted (volts)	clock period (ns)	CAS latency	Symbol	max (mA) outputs open			Notes
					100 MHz	80 MHz	66 MHz	
Operating, burst length=1, tRC=tRC min	V_{IL} max / V_{IH} min			Icc1	TBD	TBD	TBD	
Standby, one or both banks row active	V_{IL} max / V_{IH} min	tCK min		Icc6	TBD	TBD	TBD	
	V_{IL} max / V_{IH} min	∞		Icc6	TBD	TBD	TBD	
Standby, both banks idle (not Power Down)	V_{IL} max / V_{IH} min	tCK min		Icc6	TBD	TBD	TBD	
	V_{IL} max / V_{IH} min	∞		Icc6	TBD	TBD	TBD	
	0.2 / V_{CC} - 0.2	∞		Icc6	TBD	TBD	TBD	
Power Down;	CKE = V_{IL} max	tCK min		Icc7	2	2	2	2
	CKE = V_{IL} max	∞			1.5	1.5	1.5	3
	CKE = 0.2	∞		Icc6	1.5	1.5	1.5	3
Burst read / write;	V_{IL} max / V_{IH} min	tCK min		Icc4	TBD	TBD	TBD	
Block write;		tCK min		Icc4	TBD	TBD	TBD	
Auto Refresh;tRC ≥ tRC min				Icc9	TBD	TBD	TBD	
Self Refresh;	0.2 / V_{CC} - 0.2			Icc10	1.5	1.5	1.5	

NOTES:

2. All other inputs changing every 30ns.
3. All inputs stable.



Output load circuit for AC measurements.

AC CHARACTERISTICS

TIMING PARAMETERS AND DIAGRAMS

Synchronous Timing Parameters (C_{LOAD} = 30pF)									
Parameter		Symbol	-10		-12		-15		Unit
			min	max	min	max	min	max	
Clock cycle time	CAS latency = 3	t_{CK3}	10	-	12	-	15	-	ns
	CAS latency = 2	t_{CK2}	15	-	18	-	22.5	-	ns
	CAS latency = 1	t_{CK1}	30	-	36	-	45	-	ns
Access time from CLK	CAS latency = 3	t_{AC3}	-	8	-	10	-	12	ns
	CAS latency = 2	t_{AC2}	-	13	-	16	-	17	ns
	CAS latency = 1	t_{AC1}	-	28	-	32	-	36	ns
CLK pulsewidth high		t_{CH}	3	-	4	-	5	-	ns
CLK pulsewidth low		t_{CL}	3	-	4	-	5	-	ns
Data - out hold time		t_{OH}	3	-	3	-	3	-	ns
Data - out low impedance time		t_{LZ}	2	-	2	-	2	-	ns
Data - out high impedance time		t_{HZ}	2	10	2	12	2	14	ns
Set - up time to CLK, all inputs except CKE at Power Down Exit		t_{SU}	2	-	3	-	3	-	ns
Set - up time to CLK, CKE at Power Down Exit		t_{SUCKP}	5	-	5	-	5	-	ns
Hold time from CLK, all inputs		t_H	2	-	3	-	3	-	ns

Asynchronous Timing Parameters								
Parameter	Symbol	-10		-12		-15		Unit
		min	max	min	max	min	max	
Auto Refresh to Auto Refresh or Row Activate to Row Activate command period	t_{RC}	90	-	106	-	125	-	ns
Activate row to precharge or burst terminate command period (same bank)	t_{RAS}	60	-	70	-	80	-	ns
Precharge to activate row command period	t_{RP}	30	-	36	-	45	-	ns
Activate row to read / write command period	t_{RCD}	30	-	36	-	45	-	ns
Activate bank to activate opposite bank command period	t_{RRD}	20	-	24	-	30	-	ns
Block Write command period	t_{BWC}	20	-	24	-	30	-	ns
Data - in to precharge command	t_{DPL}	10	-	12	-	15	-	ns
Mode Register, Special Access Command Period	t_{MRC}	15	-	15	-	15	-	ns
Transition time (V_{IL} max ↔ V_{IH} min)	t_T	1	5	1	5	1	5	ns
Refresh period, 1024 rows (milliseconds)	t_{REP}	-	17	-	17	-	17	ns

Summary of Functions and Function Invokation

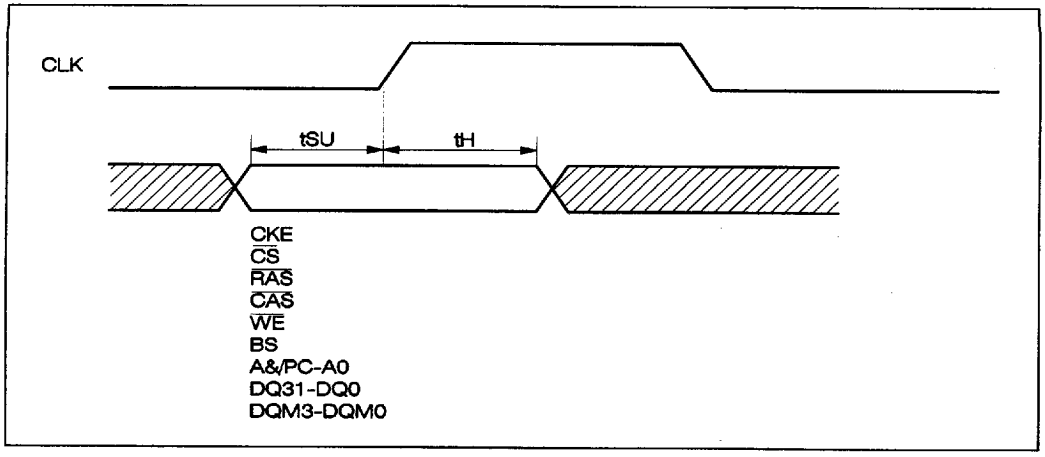


Figure 3. General Cycle Invokation Scheme for SGRAM

General Cycle Select

The available functions of the SGRAM are selected according to the values of the various control inputs at each rising edge of CLK and the internal state of the SGRAM at that time. Figure 3 shows how each control input must be valid with an adequate set up and hold time relative to the rising edge of CLK to perform the desired command. Table 2 shows the complete state table and command set for the SGRAM.

General State Transition and Command Sequence for One Bank

With few exceptions, the two banks of the SGRAM operate autonomously according to which bank is selected by the BS signal for any given cycle type. Figure 4 shows a simplified arrangement of the possible state transitions for each bank operating separately. Normally, a row of DRAM in one of the two banks is activated. While the bank is activating, only NOP cycles are allowed to that bank. After a certain time period, the bank enters its active state, designated by "Row Active". Once in the Row Active state, commands for executing Read, Read with Auto Precharge, Write (including block write and write per bit), and Write with Auto Precharge can be executed, which transition the bank to the appropriate state and allow read or write bursting to occur. Reads and Writes can be intermixed along the same row, or page address, however certain timing parameters and clock cycle latencies must be observed when switching between the read and write states. Read and Write operation to the selected bank(without Auto Precharge selected) can be terminated in one of four ways:

1) By issuing a precharge command to the selected bank
   → Goes to Precharging state
2) By issuing a burst terminate command
   → Goes to Row Active state
3) By issuing a read or write command to the opposite bank
   → Current bank goes to Row Active state
4) By reaching the end of the burst (burst length=1, 2, 4, or 8 only).
   → Goes to Row Active state

NOTE: If the burst length is set to full page, the burst will not terminate even after all addresses in the full page burst have been read or written. The burst can only be terminated by issuing one of commands 1-3 above.

Read and Write operation to the selected bank(with Auto Precharge selected) can be terminated only by reaching the end of the selected burst, after which that bank goes to the precharging state. Auto Precharge is not supported for burst length equal to full page.

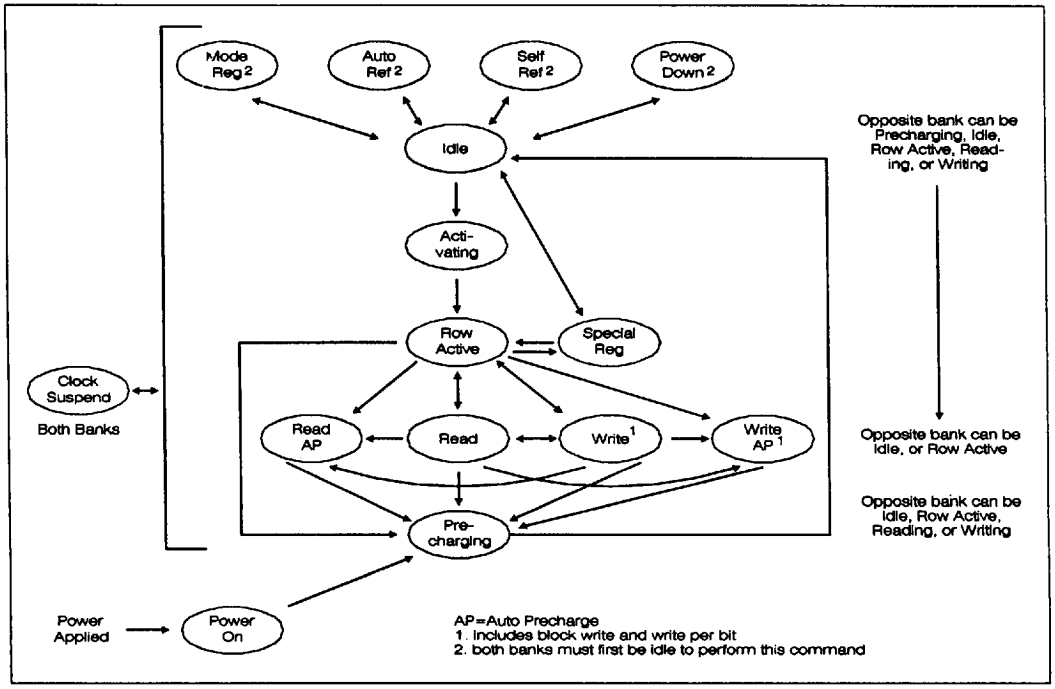


Figure 4. Simplified state transition diagram for each bank.

After precharge of the selected bank is invoked, that bank enters the "Precharging" state for some specified period of time during which only NOP cycles can be excuted to that bank. After the specified precharge interval is expired, the bank re-enters the Idle state. It is important to note that while either bank is transitioning from one state to another according to Figure 4, the opposite bank can be active. Due to the single read and write port of the SGRAM, the two banks cannot be reading or writing simultaneously. For example, if bank 0 is in the read state and bank 1 is in the row active state, a new read command given with bank 1 selected by BS, will cause bank 1 to enter the read state and bank 0 to terminate its burst and enter the row active state. While a bank is in the row active, read, or write state, the clock signal can be suspended. This causes the external clock signal to be ignored and all cycles to be decoded as NOPs. Suspending the clock affects both banks, regardless of which ones are active.

Table 2 describes the detailed state transition and command invokation sequence of a specified bank.

Detailed State Transition and Command Description

Table 2. State and Function Truth Table for Selected Bank [1]

Current State of Selected Bank	CLK↑										Action to Selected Bank (Unless otherwise noted)
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	BS	A8	A7-A0	DQMi	DQi	
Idle	L	L	L	L	L	opcode			X	X	Mode Register Set
	L	L	L	L	H	X	X	opcode	X	X	Special Register Set
	L	H	H	H	X	X	X	X	X	X	NOP
	H	X	X	X	X	X	X	X	X	X	
	L	L	H	L	X[2]	BA	RA	X	X		
	L	L	H	H	L	BA	RA	RA	X		Activate Row,Bank Deselect WPB Mask
	L	L	H	H	H	BA	RA	RA	X		Activate Row, Bank Select WPB Mask
Row Active	L	L	L	L	H	X	X	opcode	X	X	Special Register Set
	L	H	H	H	X	X	X	X	X	X	NOP
	H	X	X	X	X	X	X	X	X	X	
	L	L	H	L	X[2]	BA	L	X	X	X	Precharge Selected Bank
	L	L	H	L	X[2]	X	H	X	X	X	Precharge Both Banks
	L	H	L	L	L	BA	L	CA	byte enable	data in	Begin Write
	L	H	L	L	H	BA	L	CA	byte enable	addr mask	Begin Block Write
	L	H	L	L	L	BA	H	CA	byte enable	data in	Begin Write, Auto Precharge
	L	H	L	L	H	BA	H	CA	byte enable	data in	Begin Block Write, Auto Precharge
	L	H	L	H	L	BA	L	CA	byte enable	data out	Begin Read
	L	H	L	H	L	BA	H	CA	byte enable	data out	Begin Read, Auto Precharge
Read	L	H	H	H	X	X	X	X	X	data out	NOP, continue burst to end → Row Active
	H	X	X	X	X	X	X	X	X	data out	
	L	L	H	L	X[2]	BA	L	X	X	data out	Term Burst, Prechg Sel. Bank
	L	H	L	L	X[2]	X	H	X	X	data out	Term Burst, Prechg Both Banks
	L	H	L	L	L	BA	L	CA	X	data out	Term Burst, Begin Write[3]
	L	H	L	L	L	BA	H	CA	X	data out	Term Burst, Begin Write, Auto Precharge[3]
	L	H	L	L	H	BA	L	CA	X	data out	Term Burst, Begin Block Write[3]
	L	H	L	L	H	BA	H	CA	X	data out	Term Burst, Begin Block Write, Auto Precharge[3]
	L	H	L	H	L	BA	L	CA	X	data out	Term Burst, Begin New Read

Table 2. State and Function Truth Table for Selected Bank [1] (Continued)

Current State of Selected Bank	CLK↑										Action to Selected Bank (Unless otherwise noted)
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	BS	A8	A7-A0	DQM_i	DQ_i	
Read, cntd	L	H	L	H	L	BA	H	CA	X	data out	Term Burst, Begin New Read. Auto Precharge
	L	H	H	L	X[2]	X	X	X	X	data out	Term Burst→Row Active
Write	L	H	H	H	X	X	X	X	X	data in	NOP, continue burst to end→Row Active
	H	X	X	X	X	X	X	X	X	data in	
	L	L	H	L	X[2]	BA	L	X	X	X	Term Burst, Precharge Selected Bank
	L	L	H	L	X[2]	X	H	X	X	X	Term Burst, Precharge Both Banks
	L	H	L	L	L	BA	L	CA	X	X	Term Burst, Begin New Write
	L	H	L	L	L	BA	H	CA	X	X	Term Burst, Begin New Write, Auto Precharge
	L	H	L	L	H	BA	L	CA	X	X	Term Burst, Begin New Block Write
	L	H	L	L	H	BA	H	CA	X	X	Term Burst, Begin New Block Write, Auto Precharge
	L	H	L	H	L	BA	L	CA	X	X	Term Burst, Begin New Read
	L	H	L	H	L	BA	H	CA	X	X	Term burst, Begin New Read, Auto Precharge
	L	H	H	L	X[2]	X	X	X	X	X	Term Burst→Row Active
Read, Auto Prchg	L	H	H	H	X	X	X	X	X	data out	NOP, continue burst to end→Precharge[4]
	H	X	X	X	X	X	X	X	X	data out	
Write, Blk Write,Auto-Prchg	L	H	H	H	X	X	X	X	X	data in	NOP, continue burst to end→Precharge[4]
	H	X	X	X	X	X	X	X	X	data in	
Precharging	L	L	H	L	X	BA	L	X	X	X	NOP→Idle after t_{RP}
	L	H	H	H	X	X	X	X	X	X	NOP→Idle after t_{RP}
	H	X	X	X	X	X	X	X	X	X	
Row Activating	H	X	X	X	X	X	X	X	X	X	NOP→Row Active after t_{RCD}[5]
	L	H	H	H	X	X	X	X	X	X	
Mode Reg. Accessing	L	H	H	H	X	X	X	X	X	X	NOP
	H	X	X	X	X	X	X	X	X	X	
Special Reg. Accessing	L	H	H	H	X	X	X	X	X	X	NOP
	H	X	X	X	X	X	X	X	X	X	

NOTES:

1.Assumes CKE high on the previous clock cycle.

2. Assignment is 'x' in the Hyundai design, however as of August 30, 1994 the JEDEC committe specifies 'L'. To insure compatibility among vendors, the user is advised to treat this assignment as 'L'

3. Read burst must terminate one cycle before the start of a write sequence. This can be accomplished in one of two ways. First, if the last bit of the burst is output two cycles before the start of the write sequence, the burst will terminate and the output will tristate during the cycle before the write command is issued. Second, the burst can be terminated by bringing DQMi high and issuing a terminate burst command two cycles before the write command. This will also guarantee that the output will tristate and the read pipeline will be flushed during the cycle before the write command is issued.

4. Within a Read or Write burst sequence with Auto Precharge selected, no Read or Write commands are allowed to the opposite bank. However, a read or write burst(with or without auto precharge selected) can be invoked in the opposite bank on the clock cycle corresponding to the last address of the burst in progress in the current bank.

5. t_{RCD} specifies the minimum period beginning from the start of a row activate command and the start of a read burst, write burst, or block write command in the same bank. Only NOP commands are allowed during this period to the selected bank. After the t_{RCD} minimum period has expired, but before the minimum row activation period t_{RAS} has expired, no precharge or burst terminate commands can be invoked on that bank. This is analogous to the minimum t_{RAS} period found in previous generation asynchronous DRAMS.

Table 3. State and Function Truth Table, Operations Involving Both Banks

Current State	CLK↑												Action
	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	A9	A8	A7-A0	DQMi	DQi	
	prev	curr											
Power Down	L	L	X	X	X	X	X	X	X	X	X	X	Maintain Power Down
	L	H	L	H	H	H	X	X	X	X	X	X	Exit Power Down→BBI
	L	H	H	X	X	X	X	X	X	X	X	X	Exit Power Down→BBI
Self Refresh[1]	L	L	X	X	X	X	X	X	X	X	X	X	Maintain Self Refresh
	L	H	L	H	H	H	X	X	X	X	X	X	Exit Self Refresh→BBI
	L	H	H	X	X	X	X	X	X	X	X	X	
Both Banks Idle(BBI)	H	L	L	H	H	H	X	X	X	X	X	X	Enter Power Down
	H	L	H	X	X	X	X	X	X	X	X	X	Enter Power Down
	H	L	L	L	L	H	X	X	X	X	X	X	Enter Self Refresh
	H	H	L	H	H	H	X	X	X	X	X	X	NOP
	H	H	H	X	X	X	X	X	X	X	X	X	NOP
	H	H	L	L	L	L	L	opcode			X	X	Mode Register Access
	H	H	L	L	L	L	H	X	X	opcode	X	X	Special Register Access
	H	H	L	L	L	H	X[2]	X	X	X	X	X	· Auto Refresh
CLK Suspend	L	L	X	X	X	X	X	X	X	X	X	X	Maintain CLK Suspend
	L	H	X	X	X	X	X	X	X	X	X	X	Exit CLK Suspend
Auto refreshing	H	H	L	H	H	H	X	X	X	X	X	X	NOP→Both Banks Idle after tRC
	H	H	H	X	X	X	X	X	X	X	X	X	
Any state other than avove	H	L	Any valid command for specified state										Enter CLK Suspend[3]
	H	H											See Table2

Notes:3

1. Exiting Self Refresh occurs asynchronously by bringing CKE from low to high.

2. Assignment is 'x' in the Hyundai design, however as of August 30. 1994 the JEDEC committee specifies 'L'. To insure compatibility among vendors, the user is advised to treat this assignment as 'L'.

3. The valid command specified during the Enter CLK Susupend cycle will be executed, and the next clock cycle will be ignored as well all subsequent clock cycles until CLK Suspend is exited.

Operation(cycle description, timing overview)

Mode Register Access

Description of Register Functions

The SGRAM has an on chip mode register which is programmed by the user to select the read latency, burst length and burst type to be used during read / write operations to the DRAM.

To achieve very high data rates, the SGRAM is equipped with a read pipeline which can be programmed by the user to operate with one, two, or three cycles of clock latency. Read latency is defined as the number of the first positive clock edge following the initial read invokation cycle (which we arbitrarily define as cycle 0) at which the first piece of data is guaranteed to be valid. Figure 5 illustrates read latencies of one, two, and three. The higher the latency, the higher the clock frequency the SGRAM can run at, and the higher the peak data rate.

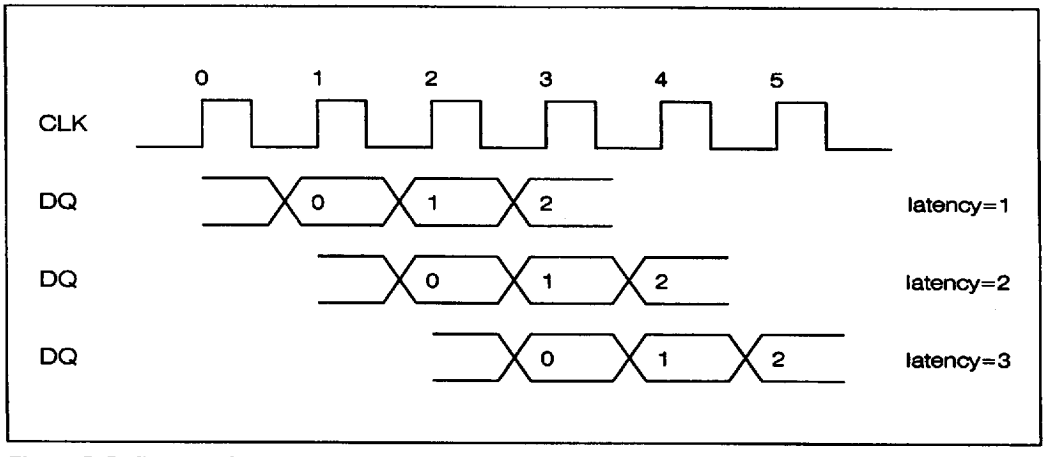


Figure 5. Definition of Read Latency With Examples

Whenever a read (or write) command is invoked, the SGRAM initiates a read (or write) to the appropriate column address selected by A7-A0. This is defined as the beginning of the read(or write)burst. Subsequent clock cycles can be used to perform high speed reads (or writes) to column addresses adjacent to the column address supplied on A7-A0 when the read or write was invoked. The number of column addresses which can be read or written, including the original address supplied on A7-A0 is defined as the burst length. The SGRAM supports burst lengths of one, two, four, eight, and a full page of column addresses.

The SGRAM supports sequential mode address bursting. In sequential mode, read or write is done to the address selected by A7-A0 at the beginning of the burst. On successive burst cycles, the column address is internally incremented and a read (or write) is performed to the incremented address. The process can continue until a read(or write) to the most significant address in the burst has been executed. On the next burst cycle, the internal address will wrap to the least significant address of the burst and a read (or write) to that address will be executed. Successive burst cycles will cause the column address to internally increment and a read (or write) to the incremented address will occur until reads (or writes) to all addresses in the burst have been executed. Table 4 show the sequence of burst addressing for burst lengths of two, four, eight, and full page.

Table 4. Address sequence for different burst lengths

Starting column address A0(decimal)	Burst Sequence
0	0,1
1	1,0

Burst Length = 2

Starting column address A1-A0(decimal)	Burst Sequence
0	0,1,2,3
1	1,2,3,0
2	2,3,0,1
3	3,0,1,2

Burst Length = 4

Starting column address A2-A0(decimal)	Burst Sequence
0	0,1,2,3,4,5,6,7
1	1,2,3,4,5,6,7,0
2	2,3,4,5,6,7,0,1
3	3,4,5,6,7,0,1,2
4	4,5,6,7,0,1,2,3
5	5,6,7,0,1,2,3,4
6	6,7,0,1,2,3,4,5
7	7,0,1,2,3,4,5,6

Burst Length = 8

Starting column address A7-A0(decimal)	Burst Sequence
0	0,1,2,....,255
1	1,2,3,....,255,0
2	2,3,4,....,255,0,1
3	3,4,5,....,255,0,1,2
⋮	⋮
255	255,0,1,....,254

Burst Length = full page

Loading the Mode Register

Figure 6 shows the general timing and control for loading the mode register per Table 2. Figure 7 shows the assignment of the op code bits to the mode register and how the mode register bits control latency and burst operation. The figure also shows the assignments for entering Hyundai vendor specific test functions(to be determined).

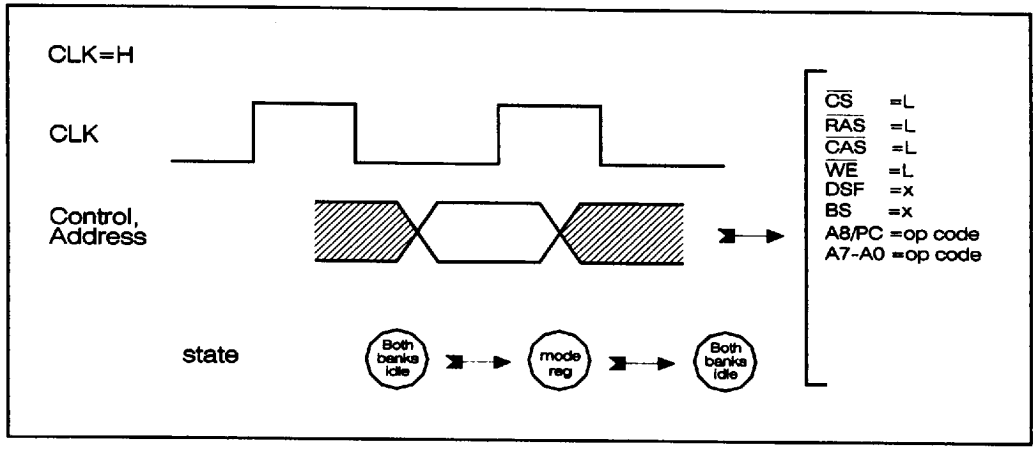


Figure 6. Timing of mode register access(program latency and burst length.)

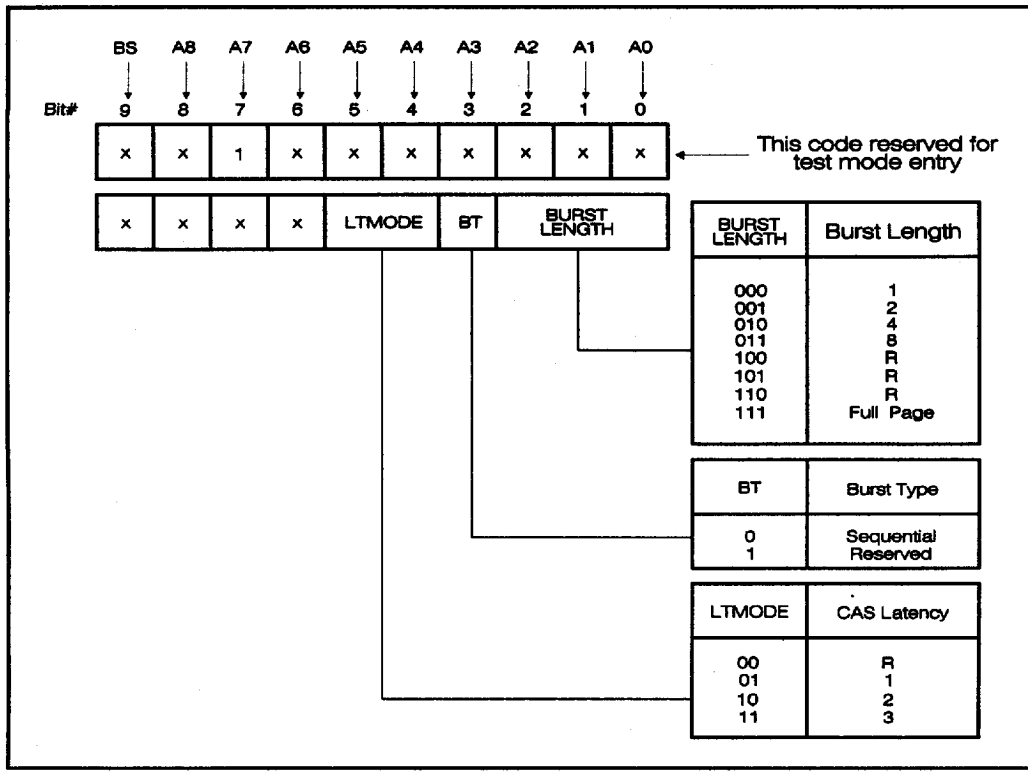


Figure 7. Loading of the mode register and mode register bit decoding

Row activate

A single row in either bank of DRAM can be activated using a row activate command. A bank can be activated even when the opposite bank is active. A row activate command cannot be given to a bank if that bank is already active. Also, a row activate command cannot be given to either bank if the SGRAM is currently in the power down, self refresh, auto refresh(for the period specified by t_{RC}), or clock suspend states. Once a row activate command has been issued to the bank selected by the bank address (supplied by BS), the selected bank leaves its idle state and goes into its row activating state. Accordingly, the row address is latched and the appropriate row in the bank is selected. Data from that row of memory is sensed and latched by the bank's sense amplifiers, to be used for later read (or write) operations. Figure 8 shows a row activation cycle per Table 2 with and without write per bit selected. t_{RCD} specifies the minimum period beginning from the start of a row activate command and the start of a read burst, write burst, or block write command in the same bank. Only NOP commands are allowed during this period to the selected bank. After the t_{RCD} minimum period has expired, but before the minimum row activation period t_{RAS} has expired, no precharge or burst terminate commands can be invoked on that bank. This is analogous to the minimum t_{RAS} period found in previous generation asynchronous DRAMS.

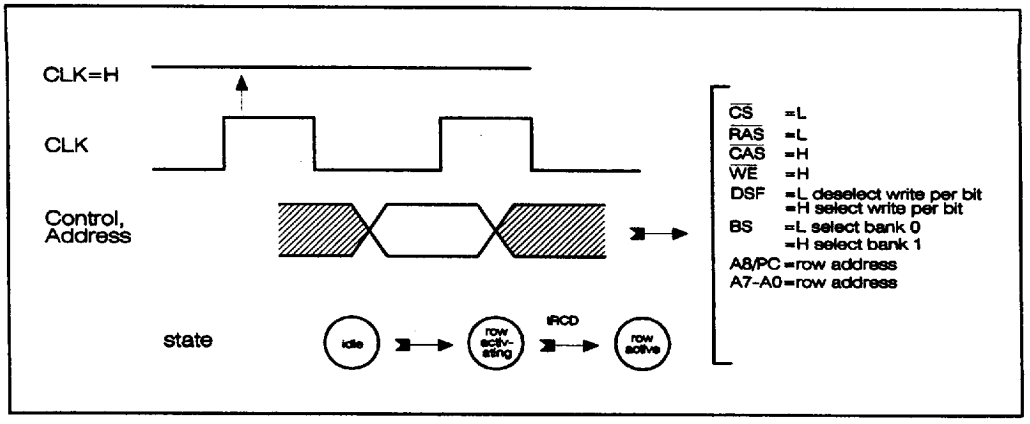


Figure 8. Row activate command to idle bank.

Read Operation with Programmable Pipeline

Normal Read Bursts (Auto Precharge deselected).

Figure 9 shows the basic timing and control for initiating a burst read operation without Auto Precharge selected. Output of data depends on the read latency and burst length selected (See Mode Register Access for details.) The higher the latency, the higher the operating frequency the SGRAM can run at, and the higher the the peak data rate. See Table 6 and Figures 25 through 27 for details. Figures 25 through 27 illustrate burst writes following burst reads on the same page. The examples assume a burst length of four but burst lengths of 1, 2, 4, 8, or full page can also be used. By issuing NOPs after the initial read command, the SGRAM will continue reading data starting from the starting column address to the end of the read burst. Data will be read to the DQ outputs(assuming the corresponding DQM signals remains enabled low) until the last address in the burst has been read out. On the next clock cycle (burst length=1, 2, 4, or 8), the DQ outputs will go to hi-z and the bank will re-enter the row active state. If burst length is set to full page, the active bank does not automatically return to the row active state, even after all addresses within the burst have been read or written. The internal column address will continue to increment modulo 256 and read operation will continue.

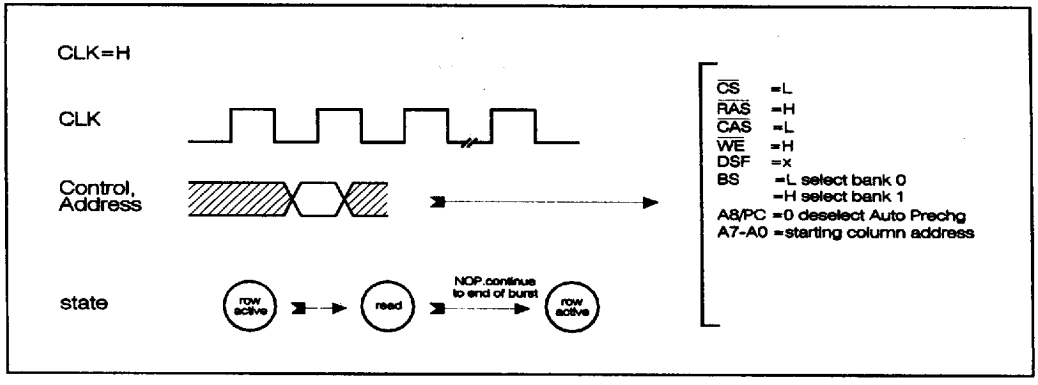


Figure 9. Burst read sequence, Auto Precharge Deselected.

While in a read burst with Auto Precharge deselected, the user can issue the following command sequences.

1. Issue NOPs, continue reading data starting from the starting column address to the end of the read burst. Data will be read to the DQ outputs (assuming DQM remains enabled low) until the last address in the burst, defined by the burst length and type, has been read out. On the next clock cycle, the DQ outputs will go to hi-z and the bank will re-enter the row active state.

2. Initiate another read command (with or without Auto Precharge selected) before the end of the burst and begin a new read burst starting from any column address. The burst in progress is terminated and the first address of the new burst is read to the output after a number of clock cycles defined by the $\overline{CAS}$ latency. See Figure 10 for details.

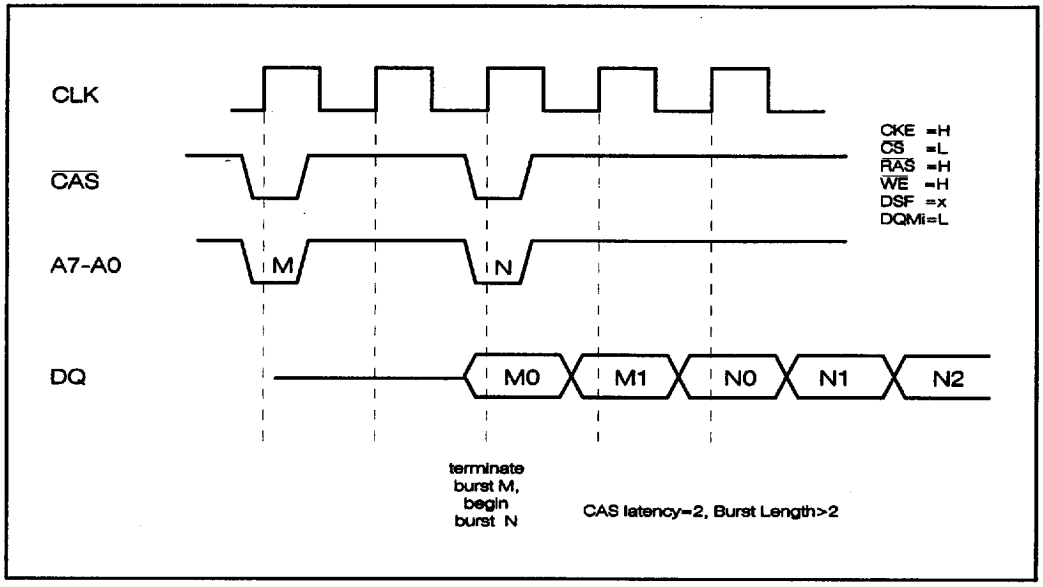


Figure 10. Timing of read initiation with read burst in progress.

3. Initiate a new write burst or block write command before the end of the burst and begin a new write burst or block write starting from any column address. The burst in progress is terminated and the first address of the new write burst or block write is written. Figure 11 illustrates the timing and control for this sequence. The appropriate DQMi read/write byte enable signals must be asserted two clock cycles before the write command is issued (JEDEC specifies DQM latency is always two, regardless of the $\overline{CAS}$ latency. The DQ outputs are guaranteed to be in hi-z after a period t_{HZ} from the beginning of the clock cycle following the clock cycle in which DQMi is asserted. Also the specification parameter t_{RTW}, the time interval measured from the beginning of the last read burst cycle to the beginning of the write command cycle, must be observed. For high frequency operation, meeting t_{HZ} and t_{RTW} may require an additional clock cycle before the write command.

4. Issue a terminate burst command and return to the row active state. The timing and control for this sequence is shown in Figure 12 for the case where $\overline{CAS}$ latency is three and burst length is greater than two. Note that in this example the terminate burst command occurs on the third clock cycle after the initial read command. The terminate burst command causes the data associated with the burst counter address at the beginning of the burst terminate cycle (M3 in Figure 12) to be output to DQ after the number of clock cycles defined by the clock latency. On the next clock cycle, DQ goes to hi-z and the bank goes to the row active state.

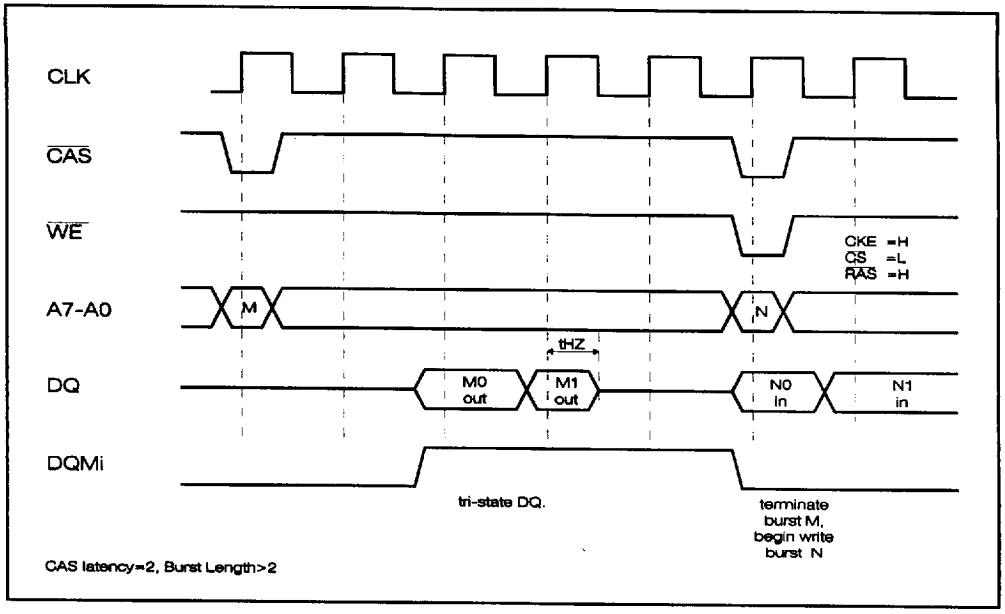


Figure 11. Timing of write initiation with read burst in progress.

5. Issue a precharge command (so long as the t_{RAS} period has expired) for the selected bank or for both banks, depending on the logic level of A8/PC, thus terminating the burst, and return to the idle state after the precharge interval t_{RP}. Like the terminate burst command, the last data read out is that associated with burst address during the precharge command cycle. The major difference between a precharge command and a burst terminate command is that the burst terminate command returns the bank to its row active state while the precharge command returns the bank to its idle state after the designated precharge interval. The timing and control for the precharge cycle is shown in Figure 13 for the case where $\overline{CAS}$ latency is two and burst length is greater than two.

6. Suspend the clock. Suspending the clock can be done in accordance with Table 3. While in the clock suspended state, the state of both banks will remain unchanged.

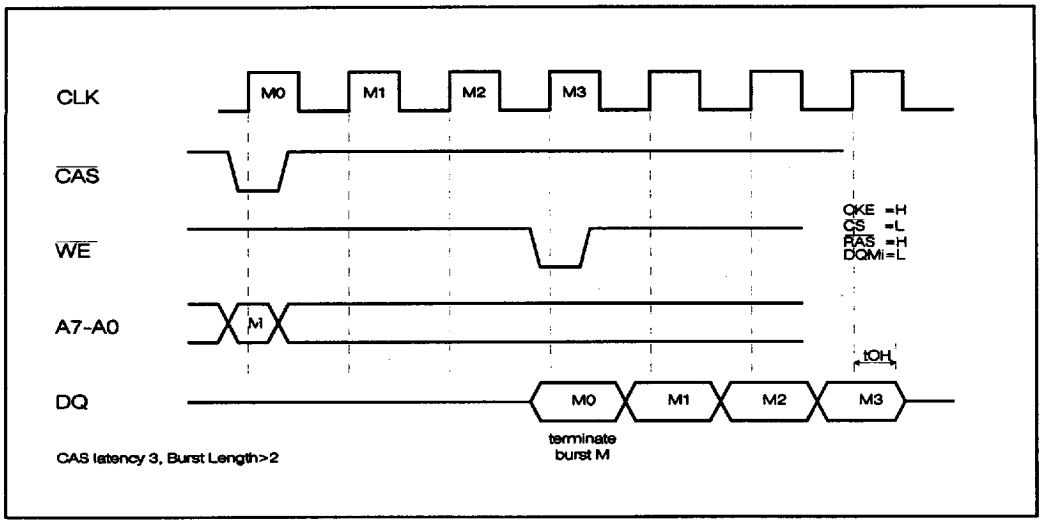


Figure 12. Timing of burst terminate command with read burst in progress.

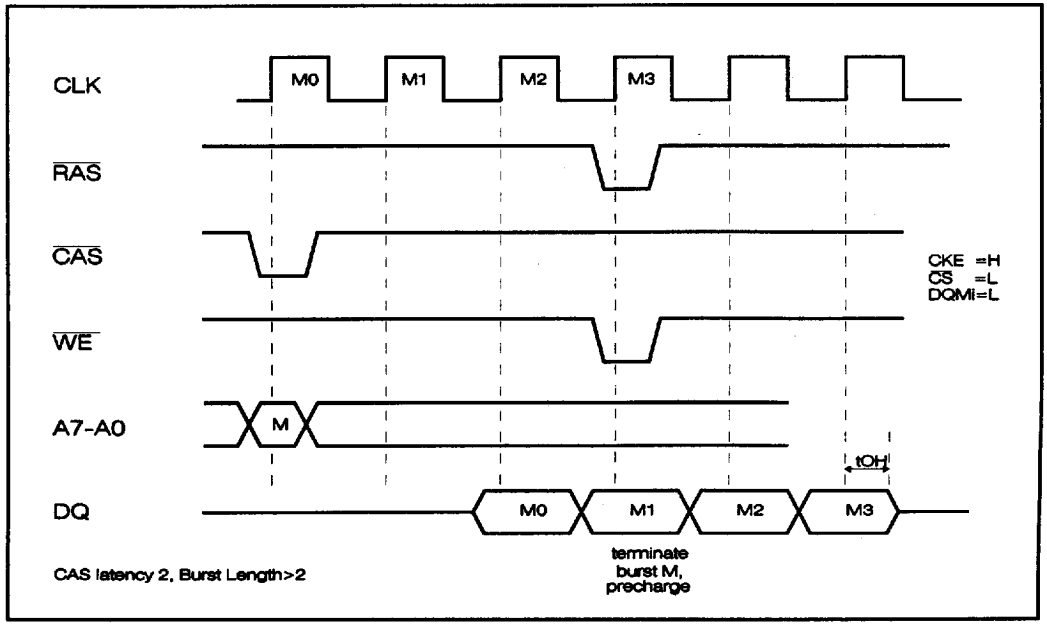


Figure 13. Timing of precharge command with read burst in progress.

Read Bursts with Auto Precharge Selected

Read with Auto Precharge can be selected with burst length set to 1, 2, 4, or 8 and is similar to normal read (Auto Precharge deselected) operation except that the read burst cannot be terminated by issuing another command. Once the read with Auto Precharge command is invoked within a bank, only NOP commands can be issued to that bank. At the clock cycle corresponding to the last column address in the burst the bank will enter precharge and return to the idle state after the tRP period has expired. Data will appear at the output according to the setting of the $\overline{CAS}$ read latency. Note that while a burst read with Auto Precharge selected cannot be terminated, data can be prevented from appearing at the DQ outputs by masking it off with the DQM control inputs. Figure 14 illustrates a burst read sequence with Auto Precharge selected for the case where $\overline{CAS}$ latency is two and burst length is two.

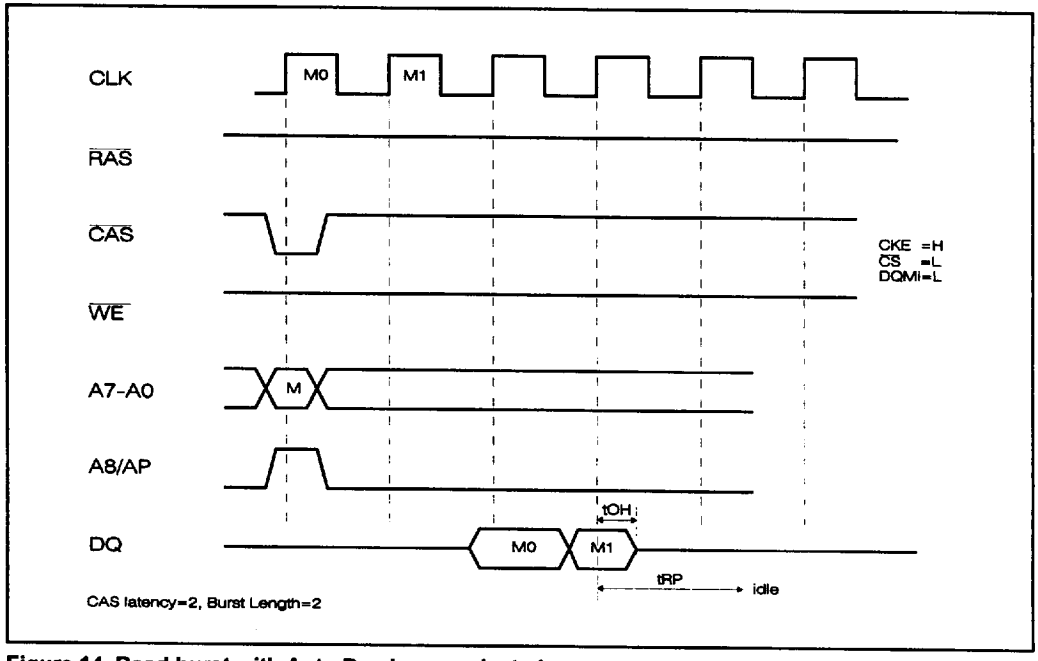


Figure 14. Read burst with Auto Precharge selected.

Write Operation

There are several variations of write operation to the two banks of DRAM. Write bursts can be initiated to either bank with and without Auto Precharge selected. Also, write per bit and block write operations can be invoked. The basic write operation showing the relationship to the programmed $\overline{CAS}$ latency and burst length will be described first, and the variations for Auto Precharge, write per bit, and block write will be described subsequently. It is important to note that Auto Precharge, write per bit, and block write are orthogonal variations to the basic write operation. That is, each of them can be invoked independently of the others.

Basic Write Operation

The latency for write operation is defined as the clock cycle difference between the clock where write command and column address are asserted and the clock cycle where the first data to be written is presented and is always equal to zero. That is the data for a write operation is presented on the same clock cycle as the corresponding address, regardless of what value of $\overline{CAS}$ latency is programmed into the mode register. Figure 15 shows this relationship.

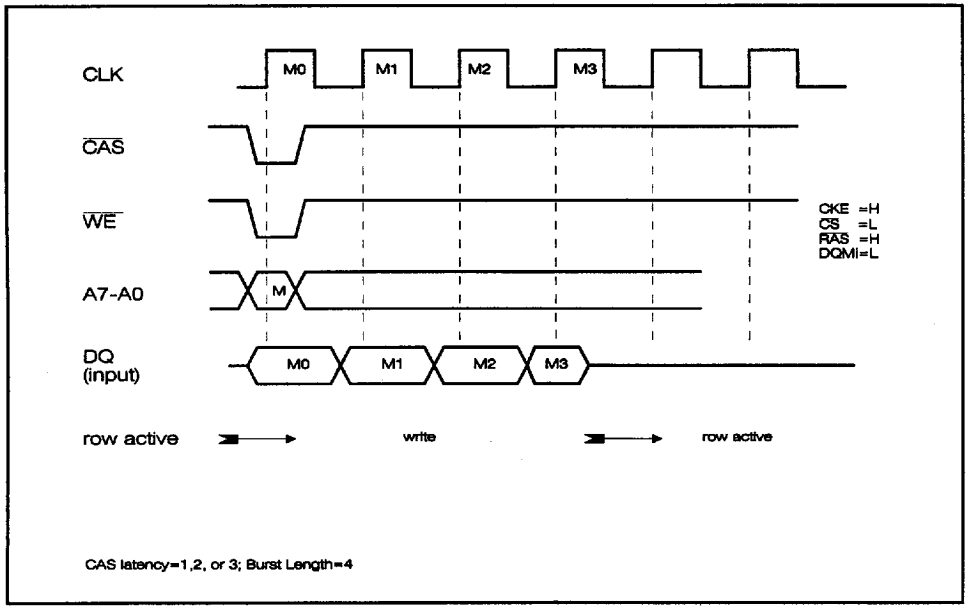


Figure 15. Write burst with Auto Precharge deselected.

Write Operation with Auto Precharge

Write operation with Auto Precharge can be selected with burst lengh set to 1, 2, 4, or 8 and is similar to write operation without Auto Precharge except that once initiated the write burst cannot be terminated by another command. To complete the burst, NOPs must be excuted and data input supplied for each address in the burst until the end of the burst has been reached. Alternatively, the DQM control inputs can be asserted to prevent writes from occuring during the burst sequence. On the clock cycle following the last address in the burst, the bank will begin precharging and will re-enter the idle state after the precharge period, t_{RP}. Figure 16 illustrates the sequence.

Write Operation With Write Per Bit

The SGRAM features a write per bit capability similar in function to previous generation Video RAMs. Write per bit allows the write to each of the 32 DQs to be controlled individually by employing a 32 bit write per bit mask(or write mask) register which can be dynamically loaded via a Special Register Access cycle. The 32 bits in the write mask register have a one to one correspondence with the 32 DQs. A logic level 1 in bit position i in the mask register enables a write to DQi during write per bit write cycles. A logic level 0 in bit position i masks off, or disables, the write to DQi during write per bit write cycles.

To invoke write per bit write cycles, the write per bit function must be selected when activating a row / bank. So long as that bank remains active, all subsequent write cycles to that row / bank will use the write mask to control which DQs get written with the input data present on the DQ pins during the write cycles. Figure 17 illustrates write per bit operation. The figure shows that Auto Precharge is deselected although Auto Precharge can be selected in exactly the same way as in other write operations previously discussed.

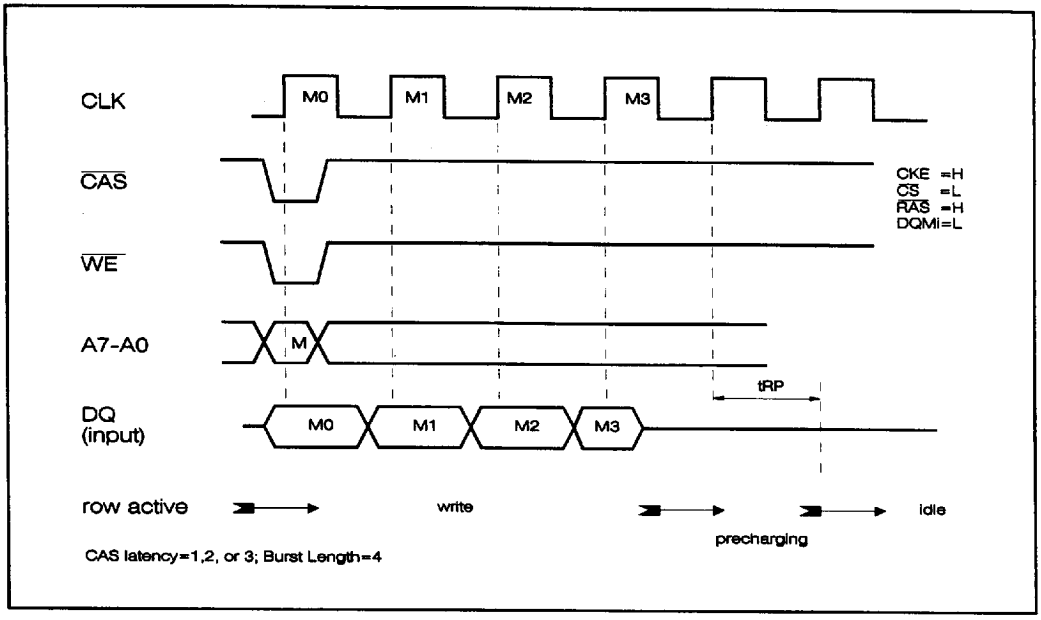


Figure 16. Write burst with Auto Precharge selected.

Block Write Operation

The SGRAM features a block write function similar to that of previous generation Video RAMs. Block write allows as many as eight times the number of bits to be written in a single cycle compared to standard write operations previously described. A 32 bit on chip color register can be loaded via a special register cycle. Once loaded, the color register acts as a data source for subsequent block write operations. The DQ pins then act as address pointers and are collectively known as an "address mask", replacing the three least significant column address bits, A2-A0. Each byte has its own independent address mask. DQ31-DQ24, DQ23-DQ16, DQ15-DQ8, and DQ7-DQ0 serve as address masks for bytes 3, 2, 1, and 0 respectively.

Considering byte 0, for example, DQ7-DQ0 act as individual address pointers to the eight column addresses represented by the eight binary combinations of A2-A0. Rather than using A2-A0 to select one address out of the possible eight to be written with the contents of the color register, the eight DQ7-DQ0 lines allow write selectability to each of the eight addresses represented by the eight combinations of A2-A0. A logic high level on DQi causes the appropriate address in memory to be written with the contents of the color register while a logic low level on DQi inhibits the appropriate address from being written. In essence, any subset of the eight column addresses(for each byte) can be written in a single block write cycle. Considering all four bytes represented by DQ31-DQ0, as many as 256 bits(8 bits × 8 column addresses × 4 bytes) can be written with the contents of the color register in every block write cycle. Figure 18 shows the write data and control for block write operation to all four bytes of the SGRAM.

Block write can be combined with write per bit and byte write (via the DQM pins) control to achieve full byte and bit mask-ability for the 256 bits selected during block write cycles. In other words, any subset of 256 bits can be written during every block write cycle. Furthermore, block write cycles can be intermixed with read cycles and non block write cycles while a bank / row is selected, however the block write command period t_{BWC} must be observed. For high frequency operation, this could result in one additional clock cycle at the end of a sequence of block write cycles. Since block write can conditionally write to eight adjacent column address locations at once, there is no provision for performing burst block writes by invoking a block write cycle followed by NOPs. In

other words, each time a block write operation is desired, a block write command including the block address A7-A3 must be invoked. Figure 19 shows the timing and control for block write. In this example, write per bit operation is selected during the row activation cycle. During the subsequent block write and write cycles, the write per bit mask register will serve as a plane mask to the 32 planes, or I/Os, of the SGRAM. During the block write cycles, the DQ pins serve as address mask bits while the color register serves as the input data source. Block write commands are not burstable. For each block write operation, a new block write command must be issued.

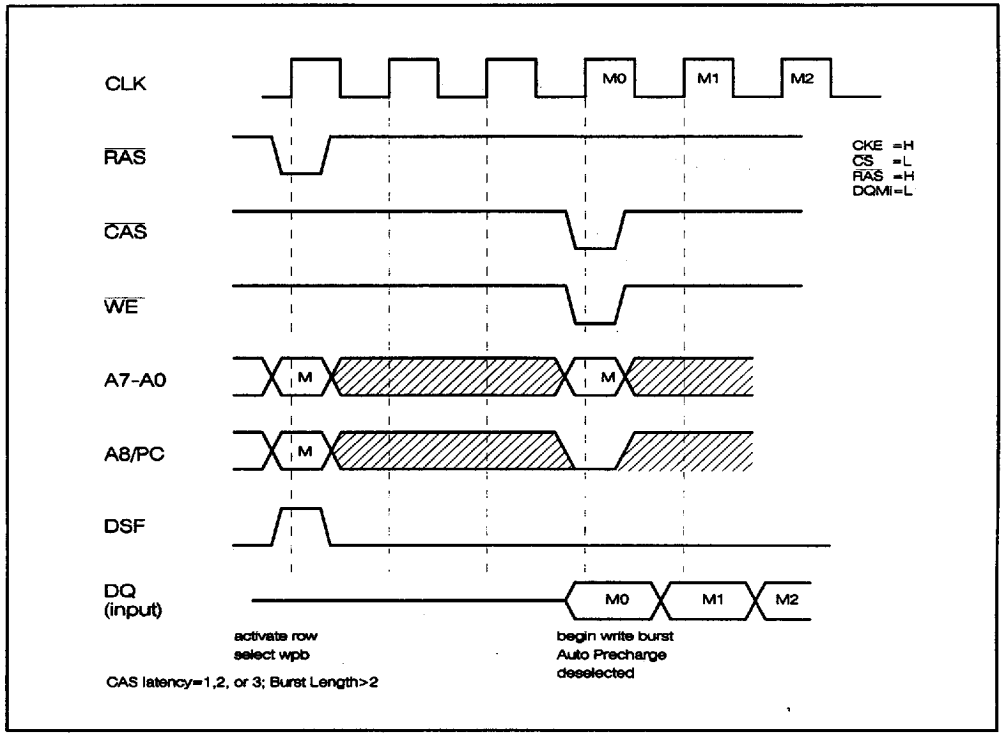


Figure 17. Write burst with write per bit selected, Auto Precharge deselected

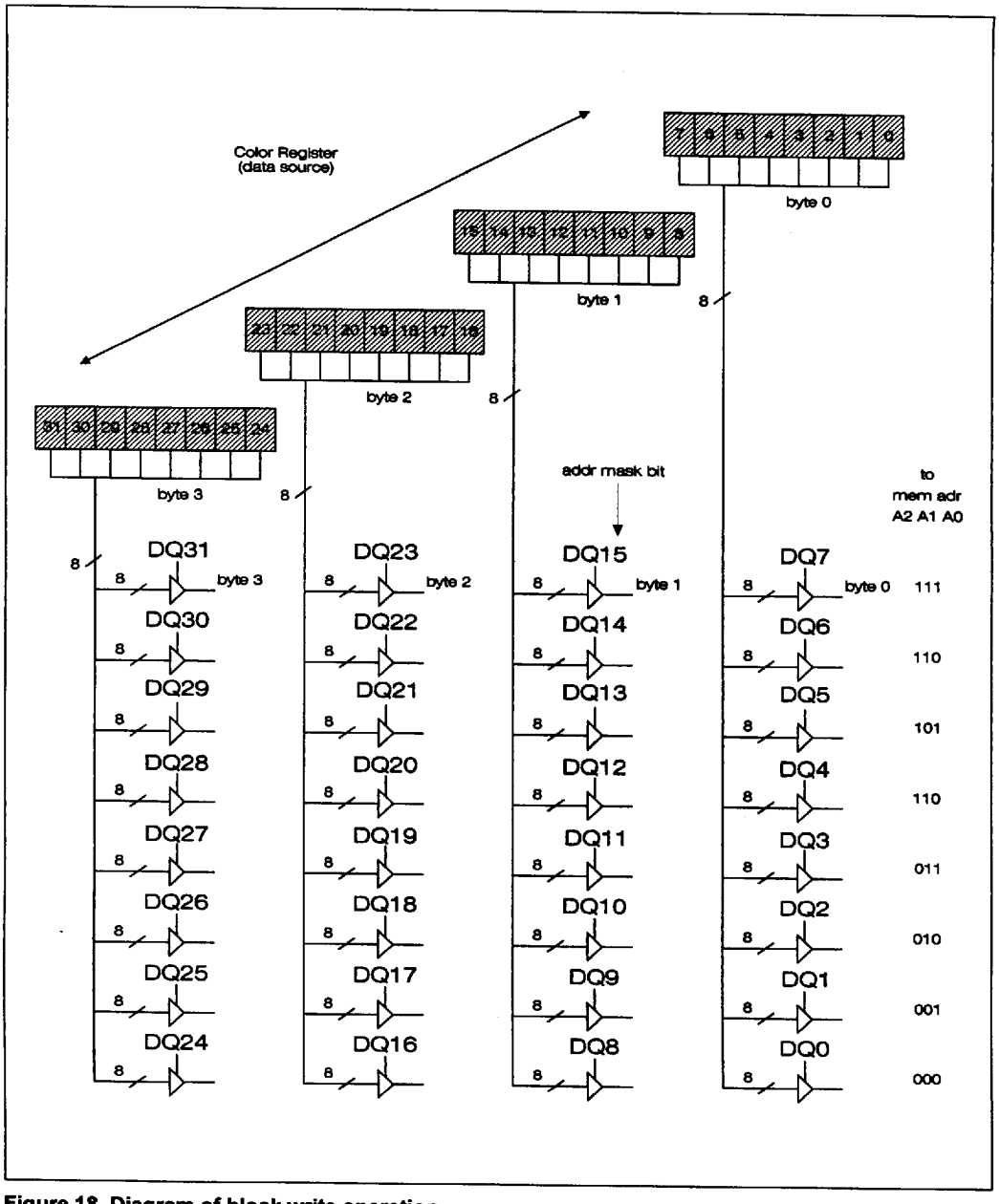


Figure 18. Diagram of block write operation

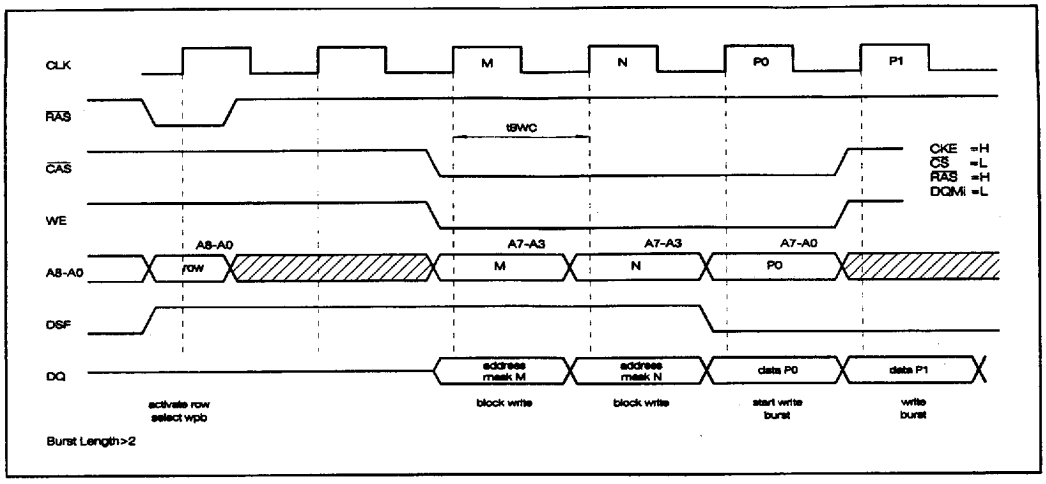


Figure 19. Timing and control for block write cycles.

Special Mode Register Operations (loading the color register, wpb mask)

To support write per bit and block write operations, the SGRAM has a write per bit mask register and a color register. Every Special Register Access allows one of these registers to be written with the contents of the DQ pins. The write per bit register and the color register are not byte writable. The DQM pins have no impact during Special Register Access operations. Write per bit operation is not available when loading the write per bit mask register or the color register. Special register access cycles are invoked as described in Table 2 and can only be invoked when both banks are in either the idle or row active state. Figure 20 shows the general timing and control for the special register access cycle and illustrates how the opcode supplied on address bits A6 and A5 determine which of the two registers, the write mask register or the color register, gets loaded from the DQ pins.

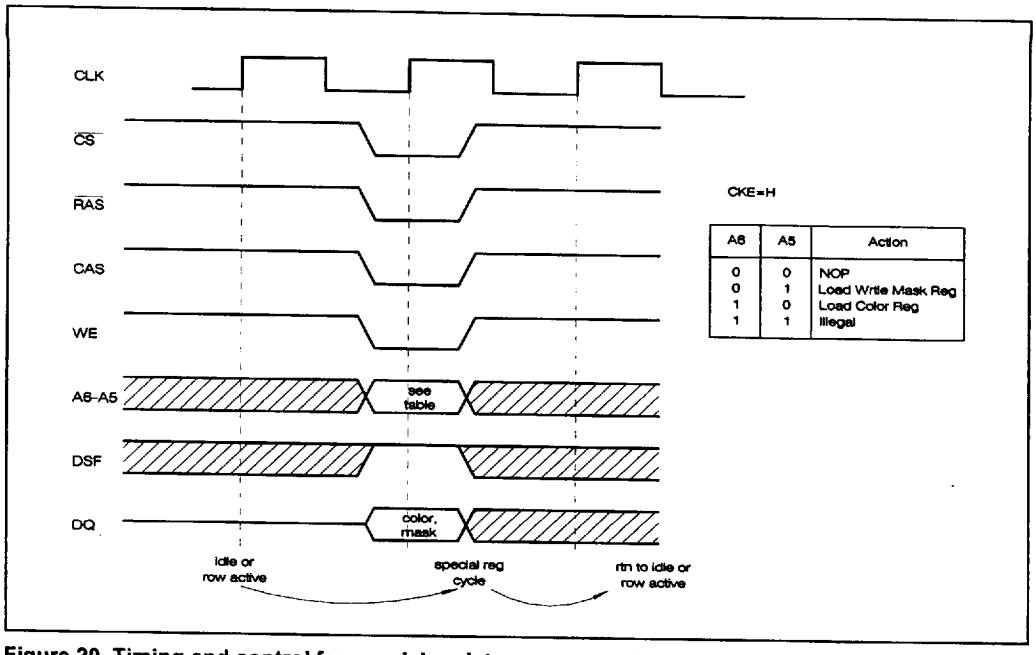


Figure 20. Timing and control for special register access cycle.

Refresh Operation

Since the SGRAM is a dynamic memory device, the stored data must be refreshed periodically or it will be lost. To avoid data loss, all rows in both banks must be accessed during the maximum refresh interval specified by t_{REF}. A row of data in either bank of RAM is refreshed whenever that row is activated. For example, activating a row for the purpose of reading or writing addresses along that row causes the data in that row to be refreshed. In addition to normal read and write operation, the SGRAM has two modes of refreshing the banks of memory: Auto Refresh and Self Refresh.

Auto Refresh

Auto Refresh is similar to $\overline{CAS}$ before $\overline{RAS}$ refresh found on previous generation asynchronous DRAMs. One Auto Refresh cycle refreshes one row of memory using a 10 bit, on chip refresh counter as the row address and bank select. The refresh counter is incremented during each Auto Refresh cycle. The upper nine bits of the counter supply the address of one of the 512 rows in each bank to be refreshed and the least significant bit selects the bank in which the refresh will occur. Thus, successive Auto Refresh cycles alternate between the two banks. Because Auto Refresh operation alternates between banks, both banks must be idle when Auto Refresh commands are invoked. Figure 21 shows two successive Auto Refresh cycles. Once an Auto Refresh cycle has been invoked, it is controlled internally until its duration. NOP cycles must be inserted during the entire Auto Refresh cycle time defined by t_{RC}.

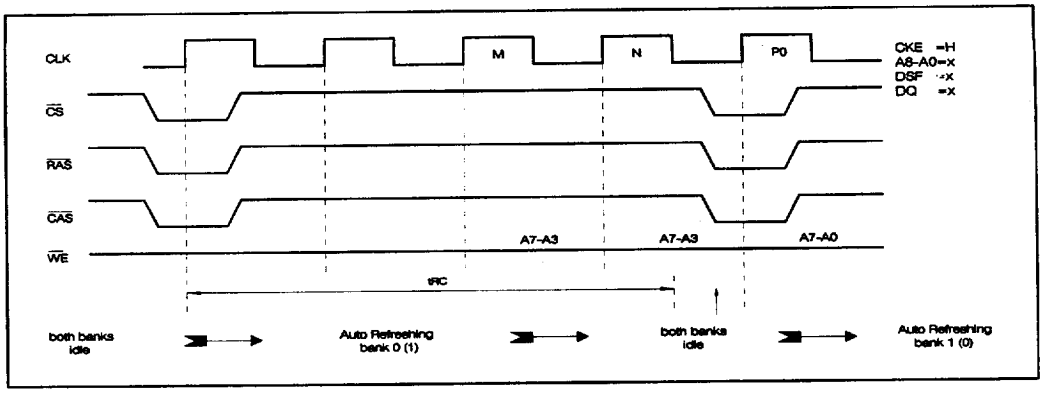


Figure 21. Timing and control for Auto Refresh Operation

Self Refresh

The SGRAM features an on chip refresh cycle timing generator which can be used in conjunction with the row refresh counter to refresh the two banks of DRAM entirely under internal control. Self Refresh can be invoked only when both banks are idle. While the device is in Self Refresh mode, CKE is the only enabled input to the device. All other inputs, including the clock are disabled and any input is ignored. Self Refresh mode is entered by invoking an Auto Refresh command with CKE low. Once this command is invoked, the cycle timing generator performs a burst refresh, sequencing through all 1024 rows(512 rows in each bank, alternating each refresh cycle between banks) with a per row refresh cycle time of approximately 1 microsecond. To conserve power, once the burst refresh has been completed to all 1024 rows the cycle timing generator automatically slows down to a per row refresh period of approximately 16 microseconds and refresh operation continues until Self Refresh mode is exited. Important:Upon exiting Self Refresh mode, the time elapsed since the least recently refreshed row was refreshed can vary from a few milliseconds to 16 milliseconds. It is thus imparative that the least recently refreshed row be refreshed immediately and that the most recently refreshed row be refreshed within the specified maximum refresh period. One way for the user to ensure this is to perform a burst of 1024 Auto Refresh commands immediately after exiting Self Refresh mode. This is especially critical for those systems employing burst refresh. For systems employing distributed refresh, a single Auto Refresh operation should be performed immediately. Since Self Refresh and Auto Refresh operations use the same internal row address counter, the first row to be refreshed by the Auto Refresh cycle will be the row least recently refreshed when Self Refresh was exited. From then on, distributed refresh should guarantee that the row most recently refreshed when Self Refresh was exited is refreshed within the specified maximum refresh interval. Self refresh mode is exited by starting the clock(if the clock had been stopped) and then asserting CKE after the clock waveform has stabilized. The low-to-high transition of CKE will re-enable the clock and other inputs asynchronously. A minimum time, specified by t_{SREX}, must be satisfied before any command other than Exit Self Refresh is invoked. Figure 22 shows how Self Refresh mode is entered and exited. See Table 2 for more information.

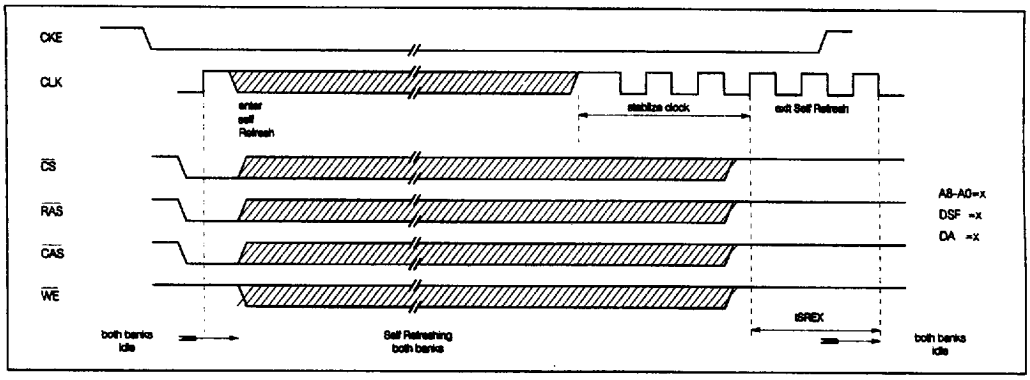


Figure 22. Timing and control for Self Refresh Operation

Power Down

The SGRAM has two internal clock buffers. A low current capacity clock buffer feeds the CKE input buffer while a high current clock buffer feeds the state machine and all DRAM circuits. During the Power Down state, the large clock buffer is disabled but the small clock buffer is not. In contrast to the Self Refresh state, entering and exiting Power Down is completely synchronous with respect to CKE. That is, CKE is sampled on every clock cycle, rather than asynchronously changing the state of the SGRAM. Power Down is the lowest power state available. During Power Down, the SGRAM is not refreshed. Therefore, the minimum refresh interval specification must be observed during power down or else data will be lost. Figure 23 shows an example of the timing and control for entering and exiting Power Down. Exiting Power Down requires one clock cycle, as shown in the figure, Other commands can be issued on the clock cycle following the Exit Power Down command cycle.

Clock Suspend

Clock Suspend is very similar to Power Down, except that the Clock Suspend command is invoked by sampling the CKE signal low while one or both banks are not idle. While the clock is suspended, only the CLK input to the small CLK buffer and the CKE input are enabled, and the state of CKE is sampled on every clock cycle. Internally, the banks remain in the state they were in when the clock was suspended. For example, if bank 0 was in the middle of a read burst when the clock suspend command was invoked, the read state will be maintained while the clock is suspended and the internal burst address counter will not increased. The final read before clock suspension will be initiated at the clock cycle in which the clock suspend command was invoked. All subsequent clock cycles leading up to the exit clock suspension command will be ignored. On the clock cycle following the the cycle in which the exit clock suspend command is invoked, the burst can be resumed from the next memory location designated by the burst length programmed in the Mode Register, or other legal commands can be issued to either the active or both banks. While the clock is suspended, the SGRAM is not refreshed. Therefore, the minimum refresh interval specification must be observed to prevent loss of data. Figure 24 illustrates how Clock Suspend is entered and exited. See Table 2 for more information.

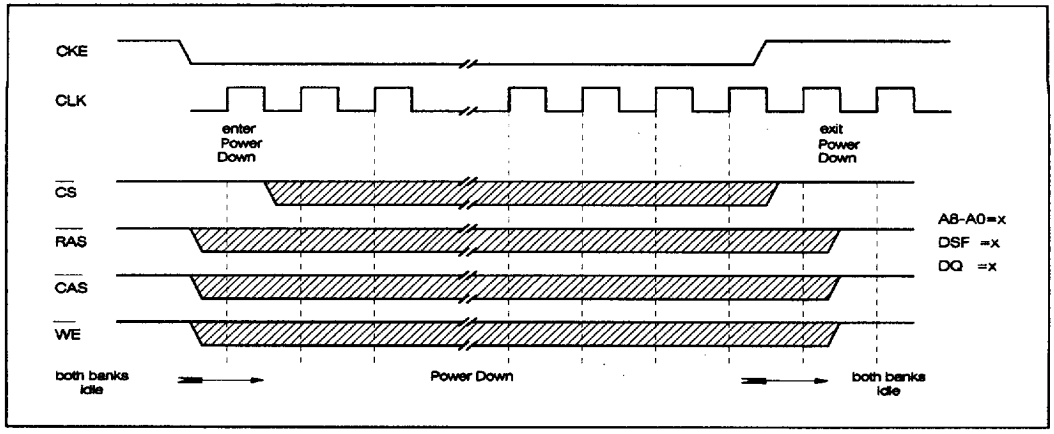


Figure 23. Example timing and control for Power Down Operation

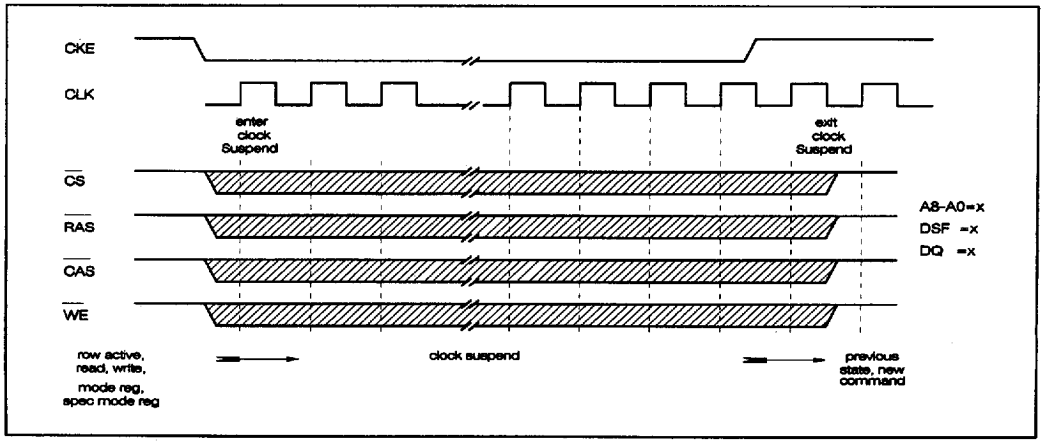


Figure 24. Example timing and control for Clock Suspend Operation

Table 5. Relationship Between Frequency and Minimum Latency

Parameter	Symbol CL / tCK	100MHz			83MHz			66MHz			Notes
		3 10	2 15	1 30	3 12	2 18	1 36	3 15.0	2 22.5	1 45	
Read command to output valid data	tCAS	3	2	1	3	2	1	3	2	1	
Active command to column command (same bank)	tRCD	3	2	1	3	2	1	3	2	1	
Active command to active command (same bank)	tRC	9	6	3	9	6	3	9	6	3	=(tRAS+tRP)
Active command to precharge command (same bank)	tRAS	6	4	2	6	4	2	6	4	2	
Precharge command to active command (same bank)	tRP	3	2	1	3	2	1	3	2	1	
Last data in to precharge command (same bank)	tRWL	1	1	1	1	1	1	1	1	1	
Block write to precharge command	tBWL	2	2	2	2	2	2	2	2	2	=(tRWL+1)
Active command active command (different bank)	tRRD	2	2	1	2	2	1	2	2	1	
Last data in to active command (Auto precharge, same bank)	tAPW	4	3	2	4	3	2	4	3	2	=(tRWL+tRP)
Block write to active command (Auto precharge, same bank)	tAPBW	5	4	3	5	4	3	5	4	3	=(tBWL+tRP)
Self refresh exit to command input	tSEC	9	6	3	9	6	3	9	6	3	=tRC
Precharge command to high impedance	tHZP	3	2	1	3	2	1	3	2	1	
Last data out to active command	tAPR	1	1	1	1	1	1	1	1	1	=(tEP+tRP)
Last data out to precharge	tEP	-2	-1	0	-2	-1	0	-2	-1	0	
Column command to column command	tCCD	1	1	1	1	1	1	1	1	1	
Write command to data in latency	tWCD	0	0	0	0	0	0	0	0	0	
Block write cycle time	tBWC	2	2	1	2	2	1	2	2	1	
Special mode register set to block write	tSBW	1	1	1	1	1	1	1	1	1	
DQM to data in	tDID	0	0	0	0	0	0	0	0	0	
DQM to data out	tDOD	2	2	2	2	2	2	2	2	2	
CKE to CLK disable	tCLE	1	1	1	1	1	1	1	1	1	
Burst stop to output valid data hold	tBSR	2	1	0	2	1	0	2	1	0	
Burst stop to output high impedance	tBSH	3	2	1	3	2	1	3	2	1	
Burst stop to write data ignore	tBSW	0	0	0	0	0	0	0	0	0	
MRS to Active command	tRSA	1	1	1	1	1	1	1	1	1	
SMRS to Active command	tSSA	1	1	1	1	1	1	1	1	1	
Active command to SMRS	tASS	3	2	1	3	2	1	3	2	1	
MRS to data in latency	tMSD	0	0	0	0	0	0	0	0	0	
SMRS to data in latency	tSSD	0	0	0	0	0	0	0	0	0	
Register set to register set	tRR	1	1	1	1	1	1	1	1	1	

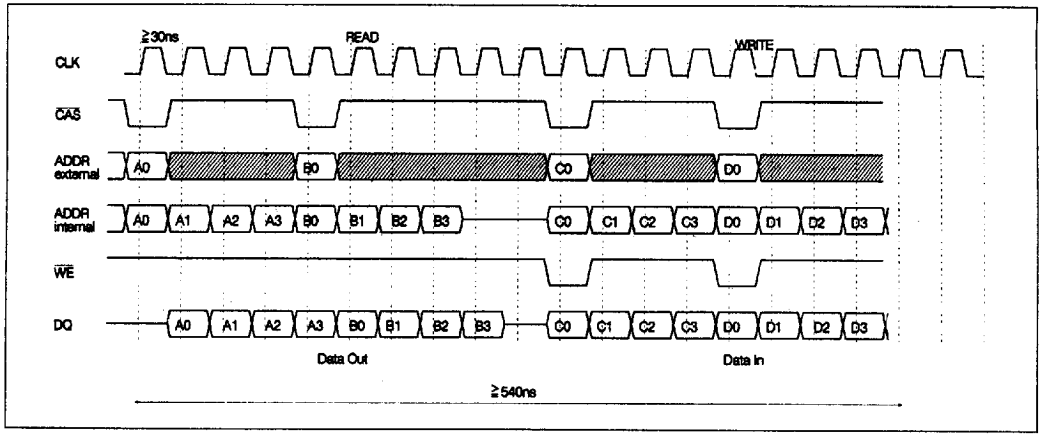


Figure 25 Timing of pipeline operation, latency = 1, burst length =4.

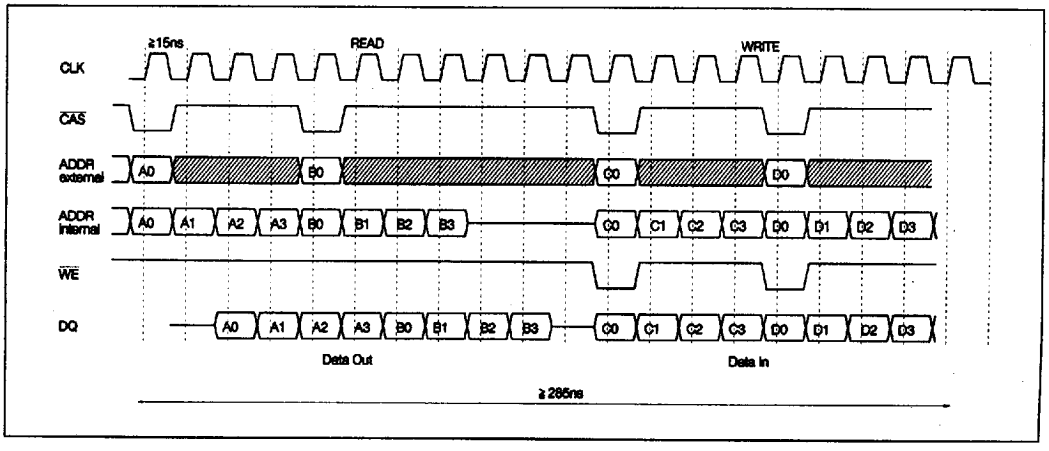


Figure 26. Timing of pipeline operation, latency = 2, burst length = 4.

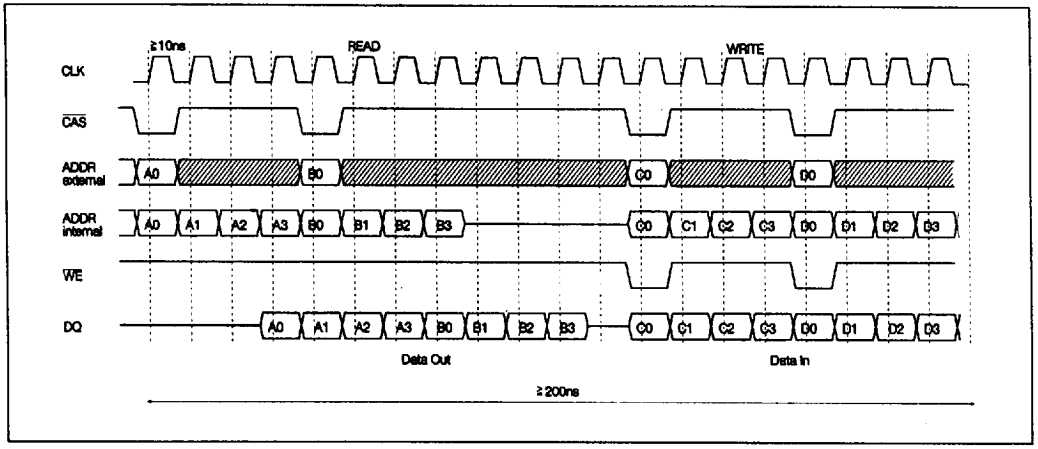


Figure 27. Timing of pipeline operation, latency = 3, burst length = 4.

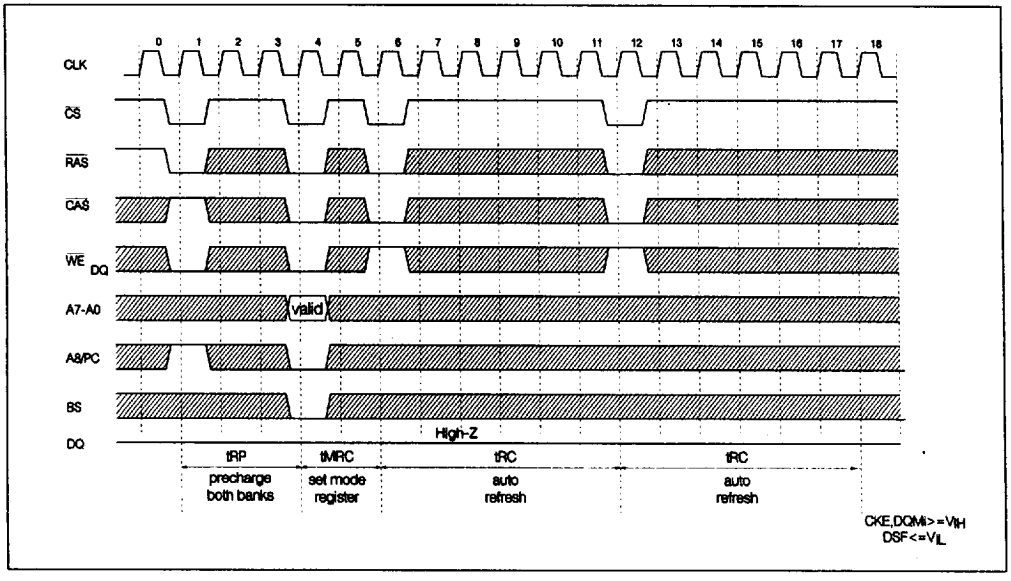
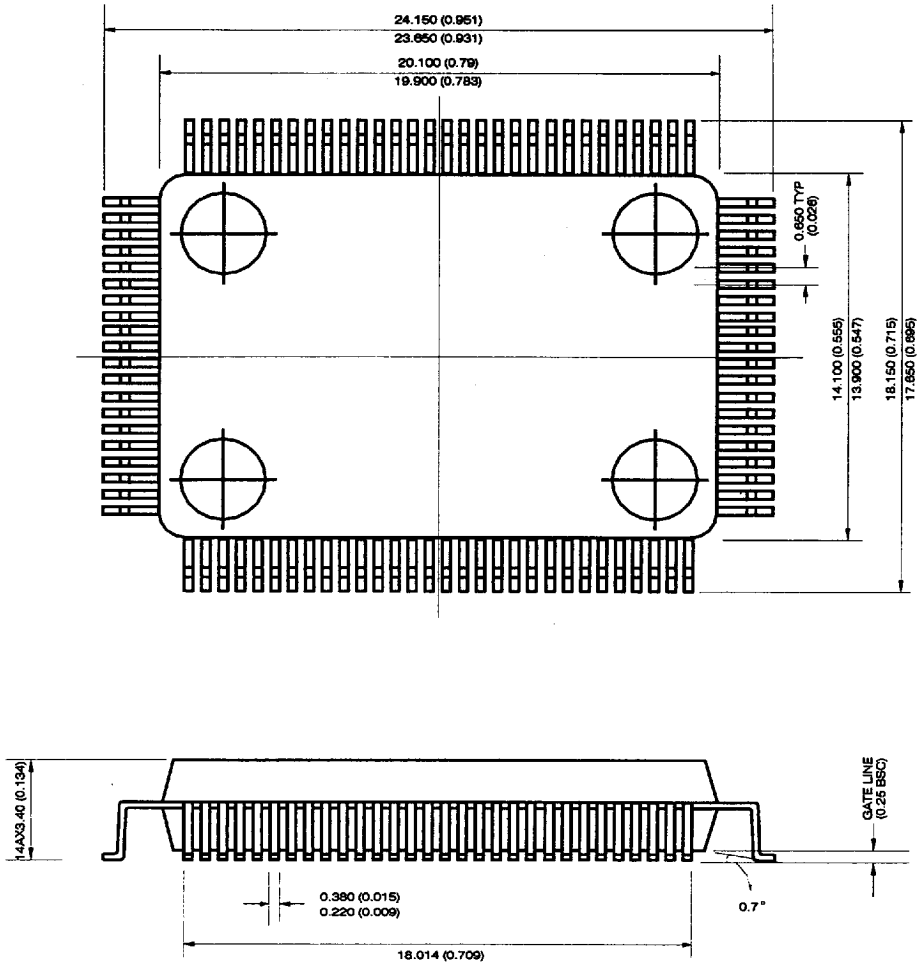


Figure 28. Power - On Sequence (using $\overline{CS}$ = H as chip deselect)

PACKAGE INFORMATION

20 × 14 mm² Plastic Quad Flat Package (PQFP)



ORDERING INFORMATION

PART NO	SPEED	PACKAGE
HY588321QF	10/12/15	20 x 14mm^2 100pin PQFP
HY588321TC	10/12/15	400 mil 80pin TSOP-II