



Integrated Device Technology, Inc.

BiCMOS STATIC RAM 64K (8K x 8-BIT) RESETTABLE RAM

**ADVANCE
INFORMATION
IDT71B65**

FEATURES:

- High-speed asynchronous RAM clear on Pin 1 (clears all RAM bits to 0)
- High-speed address access time
 - Commercial: 15/20/25ns (max.)
 - Military: 20/25/35ns (max.)
- High-speed chip select (\overline{CS}_1) time
- Produced with BiCEMOS™ high-performance technology
- Single 5V(+10%) power supply
- Input and output directly TTL-compatible
- Standard 28-pin 300 mil DIP, 28-pin SOJ, 32-pin LCC

DESCRIPTION:

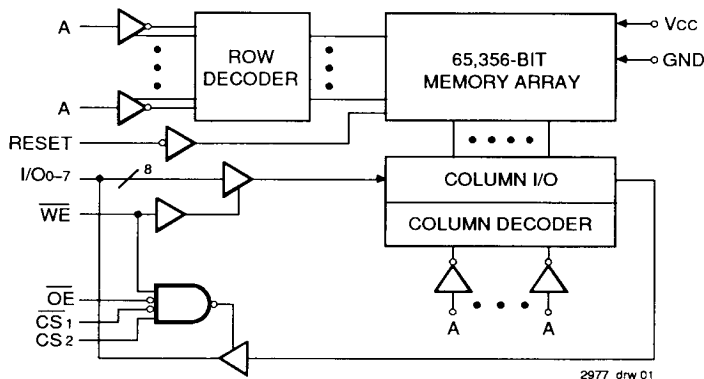
The IDT71B165 is a high-speed 65,536-bit static RAM, organized 8K x 8, with reset function. The RESET pin provides a single RAM clear control which clears all words in the internal RAM to zero when activated. This allows the memory bits for all locations to be cleared at power-on or system reset, or for a fast clear to be available to graphics, histogramming and other designs where a byte-by-byte RAM clear would cause noticeable system speed degradation.

This product is fabricated using IDT's high-performance, high reliability BiCEMOS technology. Address access time of 15ns and chip select (\overline{CS}_1) time of 8ns are available.

All inputs and outputs of the IDT71B65 are TTL-compatible and the device operates from a single 5V supply, simplifying system designs.

The IDT71B65 is packaged in a 32-pin LCC, a 28-pin 300 mil DIP and a 28-pin SOJ, providing high board level densities.

FUNCTIONAL BLOCK DIAGRAM



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MILITARY AND COMMERCIAL TEMPERATURE RANGES

DECEMBER 1990

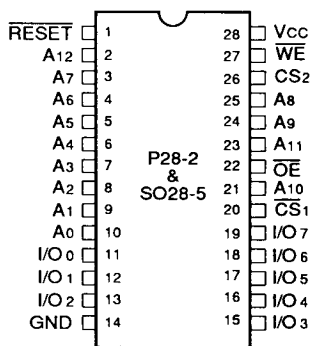
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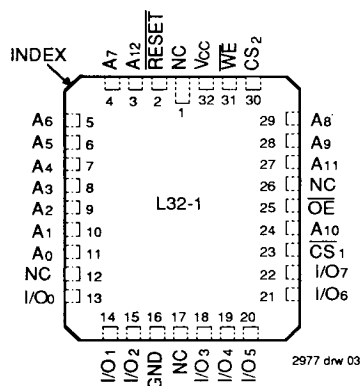
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PIN CONFIGURATIONS



2977 drw 02

**DIP/SOIC
TOP VIEW**



2977 drw 03

**LCC/PLCC
TOP VIEW**