SHARP

ARM evaluation start-up kit with Embedded Linux™

# LH0E776

# Summary Specification

Ver. 1.00

SHARP Corporation

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## 1. Overview

LH0E776 board is an evaluation board for embedded Linux (axLinux) or other OSes and it has the LH79532 -micro controller chip that has the ARM7TDMI™ core embedded.
An Embedded system is thus realized by this small format A7 size board.
LH0E776 board includes the LH79532, Flash ROM, SDRAM, Ethernet, RS232C and other communication methods.
Moreover LH0E776 board has a JTAG-ICE port for JTAG debugging.

## 2. Feature

### 2-1. Contents of the package

- LH0E776 board (1)
- AC Adapter (1)
- LH0E776 Introduction (1), General Precautions (1), MAC address (1)
- CD-ROM (1)

CD-ROM contains the following contents

| | |
|---|---|
| :/tool | GNU Tool Chain for ARM software/ for axLinux application |
| :/bin | Boot Image<br>axLinux Image<br>Flash ROM data of shipment |
| :/src | axLinux Source |
| /SamplePrograms | Sample Programs |
| :/doc | LH0E776 Introduction, Hardware Specification, Board circuit diagram etc. |

### 2-2. Principal device

| | |
|---|---|
| CPU : | LH79532 |
| Flash ROM : | 4M bytes (2M words by 16 bit, 90ns, SHARP LH28F320BJE-PBTL90) |
| SDRAM : | 32M bytes (Two of 8M words by 16 bit, 7.5ns, TOSHIBA TC59SM716AFT-75) |
| Ethernet IC : | 10Base-T communication IC |
| Other : | 7 bit LEDs and Dip switches for debugging |
| Communication : | Ethernet 10Base-T<br>RS-232C - 2 ports |
| Debugging : | JTAG connector |
| Extend : | External memory interface connector, LCD panel connector |

**Block Diagram**

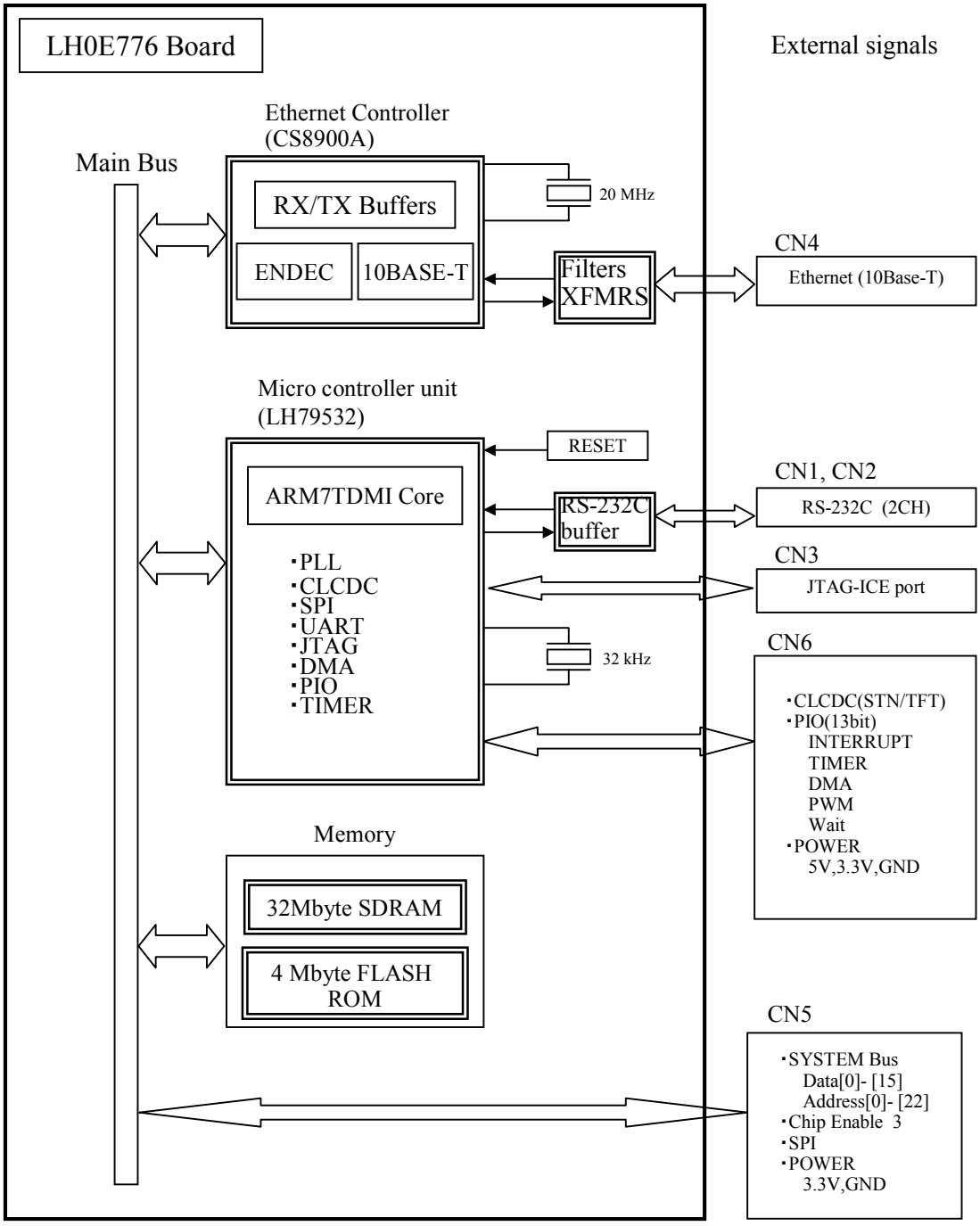



**Fig. 1. LH0E776 board Block Diagram.**

## 3. Memory Map

There are 8 external chip select signals (External I/O Chip Select : nCE[0]-[7]) in LH79532 pin mapping. And for nCE[6]-[7] –these two signals can be used as SDRAM select signal (nDCS[0] –[1]).

**Table 1. LHE776 Chip select assignement.**

| External Chip Select | |
|---|---|
| CE0 | Flash ROM<br>External Interface * |
| CE1 | CS8900A (I/O mode) |
| CE2 | CS8900A (Memory mode) |
| CE[3]-[5] | External Interface (CN5) |
| CE6(DCS0) | SDRAM |
| CE7(DCS1) | No Connection |

**Table 2. LH0E776 Memory Mapping.**

| ADDRESS | RPC_MAP = '0' | RPC_MAP = '1' |
|---|---|---|
| 0x00000000 | Flash, Ethernet I/O | SDRAM |
| 0x40000000 | SDRAM | SDRAM |
| 0x80000000 | Flash, Ethernet I/O | Flash, Ethernet I/O |
| 0xC0000000 | /// | /// |
| 0xFFFF0000 | /// | |
| 0xFFFF0400 | /// | /// |
| 0xFFFF0800 | DMA | DMA |
| 0xFFFF2000 | LCDC | LCDC |
| 0xFFFF2400 | /// | /// |
| 0xFFFF2800 | /// | /// |
| 0xFFFF4000 | UART0 | UART0 |
| 0xFFFF4400 | UART1 | UART1 |
| 0xFFFF4800 | /// | /// |
| 0xFFFF4C00 | PIO | PIO |
| 0xFFFF5000 | PWM | PWM |
| 0xFFFF5400 | SPI | SPI |
| 0xFFFF5800 | Counter/Timer | Counter/Timer |
| 0xFFFF5C00 | /// | /// |
| 0xFFFF7000 | RTC | RTC |
| 0xFFFF7400 | INTC | INTC |
| 0xFFFF7800 | RPC | RPC |
| 0xFFFF7C00 | PLL | PLL |
| 0xFFFF8000 | WDT | WDT |
| 0xFFFF8400 | /// | /// |
| 0xFFFF8800 | /// | /// |
| 0xFFFFA000 | MainASB | MainASB |
| 0xFFFFA400 | EBI | EBI |
| 0xFFFFAC00 | Cache Ctrl. | Cache Ctrl. |
| 0xFFFFB000 | /// | /// |
| 0xFFFFC000 | SDRAMC | SDRAMC |
| 0xFFFFC800 | /// | /// |
| 0xFFFFE400 | /// | /// |

**NOTE:** /// - Reserved.

# 4. Explanation for individual blocks

**Clock**

The LH79532 uses an internal oscillator circuit known as PLL. It connects to a 32kHz crystal and provides variable frequency from 10MHz to 50MHz. It can also generate the frequency from 1MHz by dividing PLL clock in the PLL controller.
The ethernet controller IC (Cirrus Logic CS8900A) connects to a 20MHz crystal and runs at 20MHz.

**Memory**

Flash ROM : 4M bytes
2M words by 16 bit Flash ROM is mounted on the LH0E776 board. A 16 bit width bus connects the Flash ROM to the LH79532. The chip select signal CE0 is assigned to the Flash ROM.

SDRAM : 32M bytes
Two of 8M words by 16bit SDRAM are mounted on the LH0E776 board. A 32 bit width bus connects these two SDRAM chips to the LH79532. The chip select signal DCS0 is assigned to these SDRAM.

The Flash ROM is assigned CE0, when LH0E776 board boots (RPC_MAP=0), CE0 will be assign 0x00000000 as the memory address. So, when LH0E776 board starts up, program counter begins at the start of the Flash ROM address.

If the RPC_MAP of LH79532's internal register is changed, the Memory Map of LH0E776 board will be switched. In such a case, the SDRAM controller should have already been initialized and configured before switching.

**Ethernet**

The ethernet controller IC of the Cirrus Logic CS8900A enables network communication through the 10Base-T.
The chip select signal CE1 is for I/O mode use and CE2 is for Memory mode use on the CS8900A. Please see the CS8900A data sheet for further details.
There are two Ethernet status LEDs. The red one indicates Link status and the green one indicates Activity status.

**LEDs/Dip switches**

LH0E776 board has 7 bit LEDs and Dip switches connecting to PIO[25]-[31](PIOB[0]-[6]). PB0-PB6 are displayed on the LH0E776 board.
Writing to PIOB of the LH79532 registers will turn to on or off these LEDs.* It is also possible to turning on or off these LEDs by switching corresponding Dip switches.
Reading PIOB of LH79532 registers make possible judging on or off statuses of Dip switches.

You can also use these 7 bit PIOB as SPI or INTR. Please refer to PIOB Multiple functions of LH79532 data sheet.

# 5. External Interface

**Ethernet interface**

LH0E776 board includes an Ethernet controller IC and can provide Ethernet 10Base-T communication.

**Table 3. Ethernet connecter pin assignment.**

| RJ45 pin | Function |
|---|---|
| 1 | ERX- |
| 2 | ERX+ |
| 3 | ETX- |
| 6 | ETX+ |
| 4,5,7,8,9,10 | NC |

**UART(RS232C) interface**

LH79532 has 2 UART channels and therefore LH0E776 board has 2 D-SUB 9 pin plug which acts as RS232C ports.
Channel 0 of CN1 provides RXD, TXD signals and RTS, CTS signals as modem control signal.
Channel 1 of CN2 provides only RXT, TXD signals.

**Table 4. RS232C connecter pin assignment.**

| RS232C pin | Function |
|---|---|
| 2 | RXD |
| 3 | TXD |
| 5 | GND |
| 7 | RTS (Channel 0 only) |
| 8 | CTS (Channel 0 only) |
| 1,4,6,9 | NC |

**JTAG interface**

There is a 20 pin connector for JTAG-ICE debugging.

**Table 5. JTAG connecter pin assignment.**

| JTAG pin | Function |
|---|---|
| 1,2 | SPU |
| 3 | NTRST |
| 5 | TDI |
| 7 | TMS |
| 9 | TCK |
| 13 | TDO |
| 15 | NSRST |
| 17,19 | NC |
| 4,6,8,10,11,12,14,16,18,17,19,20 | GND |

**External expansion interface**

LH0E776 board has two external expansion interfaces (CN5-60pin, CN6-36pin). The external expansion interfaces provide address bus, data bus, memory control signals, LCD panel signals, PIO signals of the LH79532 and also provide power resource (3,3V and 5.0V) and GND. See the Table 6 and Table 7 in detail.

It is possible to use the PIOs as SPI, INTC, PWM, TIMER, DMA signals by internal multiplexing LH79532.

**Table 6. External interface signals (CN5 – 60pin).**

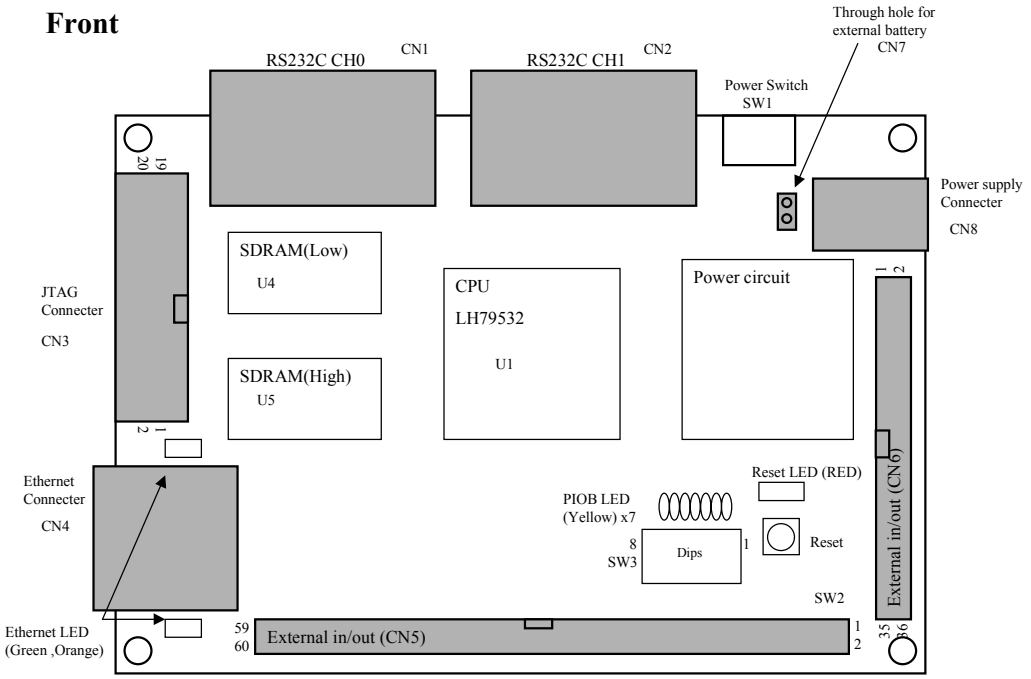
| Pin# | Signal | Pin# | Signal |
|---|---|---|---|
| 1 | RA[0] | 31 | RD[4] |
| 2 | RA[1] | 32 | RD[5] |
| 3 | RA[2] | 33 | RD[6] |
| 4 | RA[3] | 34 | RD[7] |
| 5 | RA[4] | 35 | RD[8] |
| 6 | RA[5] | 36 | RD[9] |
| 7 | RA[6] | 37 | RD[10] |
| 8 | RA[7] | 38 | RD[11] |
| 9 | RA[8] | 39 | RD[12] |
| 10 | RA[9] | 40 | RD[13] |
| 11 | RA[10] | 41 | RD[14] |
| 12 | RA[11] | 42 | RD[15] |
| 13 | RA[12] | 43 | nCE[0] |
| 14 | RA[13] | 44 | nCE[3] |
| 15 | RA[14] | 45 | nCE[4] |
| 16 | RA[15] | 46 | nCE[5] |
| 17 | RA[16] | 47 | nWE[0] |
| 18 | RA[17] | 48 | nWE[1] |
| 19 | RA[18] | 49 | nRE |
| 20 | RA[19] | 50 | PIO[41](PIOB[16]) / nWAIT |
| 21 | RA[20] | 51 | nRESETO |
| 22 | RA[21] | 52 | PIO[15](PIOB[0]) / SPI_CLK |
| 23 | RA[22] | 53 | PIO[16](PIOB[1]) / SPI_ENB |
| 24 | RA[23] | 54 | PIO[17](PIOB[2]) / SPI_OUT |
| 25 | RA[24] | 55 | PIO[18](PIOB[3]) / SPI_IN |
| 26 | RA[25] | 56 | PIO[19](PIOB[4]) / INTR0 |
| 27 | RD[0] | 57 | VCC3.3 |
| 28 | RD[1] | 58 | VCC3.3 |
| 29 | RD[2] | 59 | GND |
| 30 | RD[3] | 60 | GND |

**Table 7. External interface signals (CN6 – 36pin).**

| Pin# | Signal | Pin# | Signal |
|---|---|---|---|
| 1 | PIO[33](PIOB[8]) / PWM0 / CTOUT2 | 19 | PIO[10](PIOA[10]) / CLVD[3] |
| 2 | PIO[34](PIOB[9]) / PWM1 / CTOUT3 | 20 | PIO[11](PIOA[11]) / CLVD[4] |
| 3 | PIO[35](PIOB[10]) / DEOT0 | 21 | PIO[12](PIOA[12]) / CLVD[5] |
| 4 | PIO[36](PIOB[11]) / nDACK0 | 22 | PIO[13](PIOA[13]) / CLVD[6] |
| 5 | PIO[37](PIOB[12]) / DREQ0 | 23 | PIO[14](PIOA[14]) / CLVD[7] |
| 6 | PIO[38](PIOB[13]) / DEOT1 / PWM2 | 24 | PIO[15](PIOA[15]) / CLVD[8] / INTR4 |
| 7 | PIO[39](PIOB[14]) / nDACK1 / PWM3 | 25 | PIO[16](PIOA[16]) / CLVD[9] / INTR5 |
| 8 | PIO[40](PIOB[15])/DREQ1/PWM_SYNC | 26 | PIO[17](PIOA[17]) / CLVD[10] / INTR6 |
| 9 | VCC3.3 | 27 | PIO[18](PIOA[18]) / CLVD[11] / INTR7 |
| 10 | VCC3.3 | 28 | PIO[19](PIOA[19]) / CLVD[12] / nUDSR0 |
| 11 | PIO[2](PIOA[2]) / CLCP | 29 | PIO[20](PIOA[20]) / CLVD[13] / nUDTR0 |
| 12 | PIO[3](PIOA[3]) / CLAC | 30 | PIO[21](PIOA[21]) / CLVD[14] / nUDCD0 |
| 13 | PIO[4](PIOA[4]) / CLLP | 31 | PIO[22](PIOA[22]) / CLVD[15] / nURI0 |
| 14 | PIO[5](PIOA[5]) / CLFP | 32 | PIO[23](PIOA[23]) / CLVD[16] / nUCTS0 |
| 15 | PIO[6](PIOA[6]) / CLPOWER | 33 | PIO[24](PIOA[24]) / CLVD[17] / nURST0 |
| 16 | PIO[7](PIOA[7]) / CLVD[0] | 34 | Vpow (AC Adapter Voltage) |
| 17 | PIO[8](PIOA[8]) / CLVD[1] | 35 | GND |
| 18 | PIO[9](PIOA[9]) / CLVD[2] | 36 | GND |

# 6. Board Layout

**Front**

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