# Novel Material for Improved Quality of RF-PA in Base-Station Applications

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## NOVEL MATERIALS FOR IMPROVED QUALITY OF RF-PA IN BASE-STATION APPLICATIONS

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#### Abstract:

New materials and production technology have been introduced into LDMOS RF-PA transistors to provide advanced thermal features and increased thermal conductivity ( $K_{th}$ ). Recently  $K_{th}$  of WCu flanges has been increased by nearly 25% from near 160 W/mK to near 200 W/mK. Further improvements in the latest generation of the RF-PA utilize novel flange materials such as Cu-laminate with even higher  $K_{th}$ , by more than 25% compared to WCu. The development of Cu-laminate flange structures, involved optimization between achieving higher  $K_{th}$  and preserving desired mechanical properties for low stress and long-term reliability. Such optimization provided desired flatness for the RF-PA; yielding in lower interfacial thermal resistance between the RF-PA transistor flange and the next level heat sink. Furthermore, well characterized, highly thermally conductive, and very robust AuSi die attach was employed for efficient and reliable thermal coupling. Constellation of such materials and production technology improved overall quality of the RF-PA, enabling successful implementation in base-stations.

#### **INTRODUCTION**

The RF-PA components examined in this work belong to LDMOS (Laterally Diffused Metal Oxide Semiconductor) family recently implemented in WCDMA BS. The LDMOS Si device technology has many advantages such as high power gain, high RF efficiency, excellent linearity, ruggedness, need of only a single voltage supply, and inherently better thermal structure. Hence, LDMOS device technology has nearly replaced the previous Si bipolar technology for RF-PA applications in the cellular base-station market. LDMOS device technology has been evolving since 1<sup>st</sup> generation (1993) to its current 6<sup>th</sup> generation device structures. In the present work here, two types of RF-PA (WCu and Cu-laminate) devices have been used with the novel packaging materials in accomplishing higher thermal performance and high quality picture.

High power Radio Frequency Power Amplifier semiconductor devices (RF-PA) used in cellular basestation (BS) infrastructure equipment dissipate substantial amount of power and consequently can reach higher junction temperatures ( $T_j$ ). Failure mechanisms are accelerated at higher temperatures and hence proper attention must be paid to RF-PA's thermal management and long-term reliability assessment. Overall quality of an RF-PA is dictated by manufacturing technology, mounting method and materials used to provide low junction-to-heat sink thermal resistances ( $R_{jh}$ ). An integrated and comprehensive approach from device layout, die thinning, package material selection, to manufacturing process has been rigorously used to achieve low  $R_{jh}$  in the RF-PA.

Effective heat spreading in the Si through optimized device layouts is used to lower device thermal resistance, while providing high RF electrical performance. Thermal resistance due to Si chip thickness was reduced by thinning Si to 100 microns. Furthermore, a well characterized, highly thermally conductive, and very robust AuSi die attach is practiced. Near void free and very thin bond line thickness are key in reaching best in class die bond and enabling a lower thermal resistance. Further, AuSi die attach does not show any hardening or fatigue behavior after long thermo mechanical cycling (being a hard solder, behaves elastically). Understanding the stress created in the Si and designing the stress to be well below the strength of Si is key in the successful implementation of AuSi die attach in concert with the novel flange material and 100 micron thick Si chip. For such purpose, Finite Element (FE) simulations have been combined with dedicated measurements to develop suitable model for stress analysis. The validated FE simulations helped in correct understanding of the involved thermal resistance

and heat transfer properties across the whole assembly. Such combination of experimental and numerical simulations supported designer's guideline by obtaining the component performances at elevated temperatures and information about safe operational margins. Such information is necessary to allow utilization of whole functional capacity of the component and avoid over specification of the system.

### EXPERIMENTAL TECHNIQUE AND RESULTS

The basic LDMOS device structure has three electrodes - Drain, Source, and Gate. Current flow between the Drain and the Source is controlled by the Gate. Heat dissipation occurs in the current flow path having temperature extremes in the high resistive region. A simplified view of the device cross-section is given in Fig 1 highlighting the heat dissipating structure, marked as a "heat source finger".



Figure 1. Cross-section of the LDMOS RF-PA device structure.



Figure 2. a) An SEM image of AuSi diebond of an LDMOS Si device to a metal flange. Bond line thickness is thin ( $\sim 5\mu m$ ), of uniform thickness and void free. b) The microstructure shows a uniform dispersion of Si in the Au matrix.

In a typical device layout, a single heat dissipating structure (finger) is a few micrometers (~3 $\mu$ m) wide, a few hundred micrometers (~500  $\mu$ m) long, and located a few micrometers (~10  $\mu$ m) below the surface. The whole RF-PA presents multiples of such device structures (fingers), which are arranged in parallel. Thermal density in the active area of the device is in the range of  $3\times10^7$ W/m<sup>2</sup>. It is interesting to compare this thermal flux with that on the sun's surface ( $6.6 \times 10^7$ W/m<sup>2</sup>) [1]. The thermal flux in the active region of the RF-PA device is one of the highest among semiconductor devices and this highlights the challenges in the proper thermal management.

A well characterized, highly thermally conductive, and very robust AuSi die attach material is used to bond the die to metal flange. Near void free and very thin bond line thickness are key in reaching best in class die bond and enabling a lower thermal resistance. An SEM view of AuSi die attach cross section and its microstructure is given in Fig 2.

Both types of the RF-PA (WCu and Cu-laminate) have been examined by lifetime acceleration experiments. Long-term loading experiments have been performed at elevated junction temperatures by

using two tones RF signal technique. At the same time RF-electrical parameters (linearity, gain, and efficiency) were monitored and combined with infrared (IR) thermographs. The loading measurements were performed at temperatures below and above the typical recommended values. The RF-PA with impedance matching circuitry (Device Under Test - DUT) were assembled on water-cooled plates with adjustable flow rate. This feature provided possibility to adjust for several working conditions starting from low to high and harsh temperatures. LabView based Data Acquisition System (DAQ) was used to monitor stimulation parameters and perform thermal mapping by means of a set of thermocouples. The DUTs were separated in 4 groups where each group was stimulated to reach predefined working conditions. The experiment was adjusted to covered junction temperatures (at surface of the die) in range of  $T_{jmax}$ =160–225°C. At the same time, the case temperatures ( $T_c$  - temperature on the surface of the flange at the center of symmetry of component, see Fig 3b) were adjusted and varied in range of  $T_c$ =70–110°C. Several series of IR measurements were done to correlate the device power, maximum junction temperatures and RF-electrical parameters. The DUTs were decapped and black painted for IR imaging as shown in Fig 3a. Figure 3b shows cross section of the DUT and position of thermocouples for thermal mapping and characterisation.





Figure 3. a) The RF-PA mounted into impedance matching circuitry (DUT) ready for stimulation and IR imaging. b) Cross-section view on the DUT for temperature mapping by several thermocouples.

IR measurements with both types of the components (WCu and Cu-laminate) were performed with the same stimulation and assembly conditions. Results of the measurements are presented in Fig 4. As can be seen, the Cu-laminate component has nearly 29% reduction in  $R_{jc}$  and a more uniform temperature distribution across the die compared to the standard WCu based device. Such advanced components were further examined by long-term loadings at elevated temperatures. Results of the IR measurements for the Cu-laminate component are presented in Fig 5.

Analyzing the thermal resistance in the heat-flow path of Cu-laminate components, the major contributors can be proportioned as Si die (~35%), die bond (~10%), metal flange (~40%) and the thermal interface between the component and next level heat-sink (~15%). In addition to a reduction of about 18–35% in  $R_{jc}$ , a more uniform temperature distribution across the die and the package was observed. Furthermore, the Cu-laminate structure with active RF-PA component showed high out-of-plane stability resulting in remarkable flatness of the flange. Such flatness allowed reduction of interfacial thermal resistances, sufficient heat transfer and further lowering of  $T_{jmax}$ .

For a set of working conditions at elevated temperatures ( $T_{jmax}$ = 160-225°C  $T_c$ = 70-110°C) the RF electrical parameters were monitored over long period (1.5 months) to observe stability at severe loadings. Results of the RF stability experiments with Cu-laminate components are presented in Fig 6. At elevated junction temperatures, operational window is typically limited by RF electrical properties.



Figure 4. IR microscopy temperature profiles for two type of RF-PA at 34 W CDMA output power at 70° C case temperature. a) The standard WCu package, peak die temperature  $T_{jmax}$ = 124°C with an  $R_{jc}$ = 0.52°C/W. b) The Culaminate component,  $T_{jmax}$ = 107°C with an  $R_{jc}$ = 0.37°C/W.



Figure 5. IR images taken with the Cu-laminate RF-PA at different working conditions. a)  $T_{jmax}=160^{\circ}$ C, b)  $T_{jmax}=200^{\circ}$ C and d)  $T_{jmax}=225^{\circ}$ C.

However, due to the excellent quality of the component, the observed limitations occurred only at high temperatures. The WCu type of component at  $T_j=225$ °C, showed noticeable drop in RF performances (RF gain and power) after approximately 1.5 months of severe RF loadings. At  $T_{jmax}=200$ °C, change was almost negligible and at  $T_j=180$ °C there was no change in the linearity. The new Cu-laminate component, even at high junction temperatures such as  $T_{jmax}=225$ °C, after 1.5 months showed very small changes in the RF performances. At  $T_{jmax}=200$ °C there were no changes in the electrical performances for the Cu-laminate component. These results indicated that maximum operating temperatures should be set as high

as  $T_{jmax}$ =180°C and 200°C for the WCu and Cu-laminate RF-PA components, respectively. These values reflect factors involved in the present design of the RF-PAs, its constellation of the thermal resistances and usual mounting practices.



Figure 6. RF parameters of Cu-laminate components for a set of conditions as:  $T_{jmax}$  = 160-225°C monitored over long continuous loading time.

#### SIMULATIONS

A full 3D, half symmetry, model was developed and implemented in the software code Ansys80. A parametric FE-model for the RF-PA component was constructed in the ANSYS APDL language. The FE-simulations were carried by using a sequential coupled-field analysis.



Figure 7. Half-symmetry FE model developed by using ANSYS software. a) The model mesh and corresponding temperature distribution of the fully assembled component at b) the die and c) flange surfaces. d) Corresponding stress analysis results expressed in (MPa).

The mesh model is shown in Fig 7a. As a first step, the thermal distribution in the component is calculated and compared to the results of IR measurements to validate the model. As a second step, the thermal distribution is used as the load in the stress calculations. In both types of FE-analysis, temperature dependent properties are used and structural non-linearity is not included. To reduce the number of simulations, a surface response model was constructed for calculating the maximum temperature and stress of the component. The surface response model was constructed by running 27 FE-simulations and by using a design of experiment technique [2]. In the model, the component flange bending phenomena were also included because of its influence on the silicon die. The simulation results are given in Fig 7.

#### **DISUSION AND CONCLUSION**

The quality and reliability of the RF-PA with novel materials and manufacturing technology were examined under elevated junction temperatures. Both temperature field and RF electrical performances were measured for the two types of RF-PAs over longer period of time and a set of loading conditions. Covered temperature ranges were  $T_{imax}=160-225^{\circ}$ C and  $T_c=70-110^{\circ}$ C for the junction and case temperatures, respectively. The most sensitive limiting factors observed at elevated temperatures were RF electrical properties (power, gain, linearity). For the Cu-laminate components, at junction temperatures of  $T_{imax}$ =160–180°C, the RF gain was stable over 1.5 months of continuous RF loading and has not indicated potential risks. At  $T_{imax}$ =200°C, a small drop of about 0,5 dB was observed after 1.5 months of continuous severe loadings. In the harsh temperature case (continuous at  $T_{imax}=225^{\circ}$ C), the drop in the RF gain was significant. When the WCu components were tested in a similar way, changes of the RF properties were slightly larger. At the most severe temperature conditions (continuous  $T_{jmax}=225^{\circ}$ C) observed drop in the RF gain was noticeable, drop was more than 1 dB after 1.5 months of continuous loadings. In the development of Cu-laminate flange structures, a trade-off existed between achieving higher  $K_{th}$  and still preserving desired mechanical properties. Optimized mechanical properties of the flange provided desired flatness for the Cu-laminate flange; this enabled further lowering of the interfacial thermal resistance between the RF-PA transistor flange and the next level heat-sink. Such coordinated improvements that include careful device layout, Si die thinning to 100  $\mu$ m, high  $K_{th}$  Cu-laminate flange material, robust AuSi die-attach, and the flange's flatness resulted in nearly 18%-35% reduction in  $R_{ic}$  compared to components manufactured with the conventional high thermal conductivity WCu flanges. The Culaminate flange based RF-PA device offers the possibility of 10-15% higher P1dB (RF output power) compared to the standard device.

The validated FE simulations and corresponding stress analysis showed that the thermomechanical stresses experienced even in the most severe loading conditions ( $T_{jmax}=225^{\circ}$ C) are within safe margins for both types of the RF-PAs [3]. However, upper limits are imposed by RF-PA properties suggesting that maximal operating temperature should not exceed  $T_{jmax}=200^{\circ}$ C. This value reflects the limiting factors involved by the present design of the RF-PA, its constellation of the thermal resistances and usual mounting practices. As a conclusion, we would like to emphasize that usage of novel materials in combination with cost effective manufacturing technology yielded in extended operational window and larger functional capacity for the new Cu-laminate RF-PA components. These features provide good opportunity for applications in base station environment.

References:

[1] Nick Strobel, Chapter 12 "The Sun and Stellar Structure", http://www.astronomynotes.com

[2] Eriksson L., Design of experiments principles and applications. Sweden: Umetrics/Umea; 2001.

[3] Fischer E., Upper yield point of large diameter silicon, Microelectron Eng 2001;56:117.