

STEL-1173

Data Sheet

STEL-1173
(50 MHz)
48-Bit Resolution
CMOS Numerically
Controlled Oscillator

FEATURES

- **48-BIT FREQUENCY RESOLUTION**
- **50 MHz CLOCK FREQUENCY (0 TO 70°C)**
- **SINE OR COSINE OUTPUT AVAILABLE**
- **12-BIT AMPLITUDE RESOLUTION AND 13-BIT PHASE RESOLUTION GIVES HIGH SPECTRAL PURITY, ALL SPURS <-75 dBc (AT DIGITAL OUTPUT)**
- **MICROPROCESSOR BUS COMPATIBLE CONTROL INPUTS**
- **CASCADABLE ACCUMULATOR FOR HIGHER FREQUENCY RESOLUTION**
- **2's COMPLEMENT OR OFFSET BINARY OUTPUT CODES**
- **LOW POWER CMOS**
- **MILITARY AND COMMERCIAL TEMPERATURE RANGES AVAILABLE**

APPLICATIONS

- **FREQUENCY SYNTHESIZERS**
- **SINGLE SIDEBAND CONVERTERS**
- **BASEBAND RECEIVERS**
- **DIGITAL SIGNAL PROCESSORS**
- **HIGH SPEED HOPPED FREQUENCY SOURCES**

FUNCTIONAL DESCRIPTION

The STEL-1173 Numerically Controlled Oscillator (NCO) uses digital techniques to provide a cost-effective solution for low noise signal sources. The NCO device combines low power 1.5μ CMOS technology with a unique architectural design resulting in a power efficient, high-speed sinusoidal waveform generator able to achieve fine tuning resolution and exceptional spectral purity with clock frequencies up to 50 MHz.

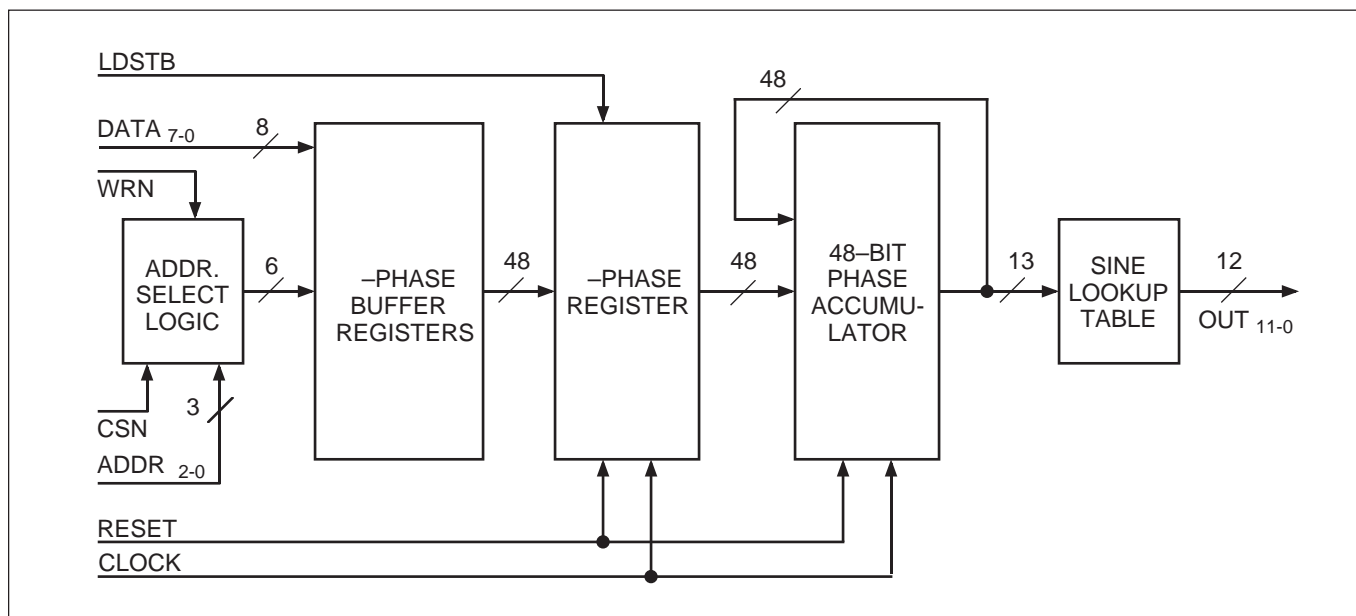
The NCO generates digital sine or cosine functions of very precise frequency to be used directly in digital signal processing applications or, in conjunction with a D/A converter, in analog frequency generation applications. The NCO is designed to interface with and be controlled from an 8-bit microprocessor bus.

The NCO maintains a record of phase which is accurate to 48 bits. At each clock cycle, the number stored in the 48 bit Δ-Phase register is added to the previous value of the phase accumulator. The number in the phase accumulator represents the current phase of the synthesized sine and cosine functions. The number in the Δ-Phase register represents the change of phase for each cycle of the clock. This number is directly related to the output frequency by the following:

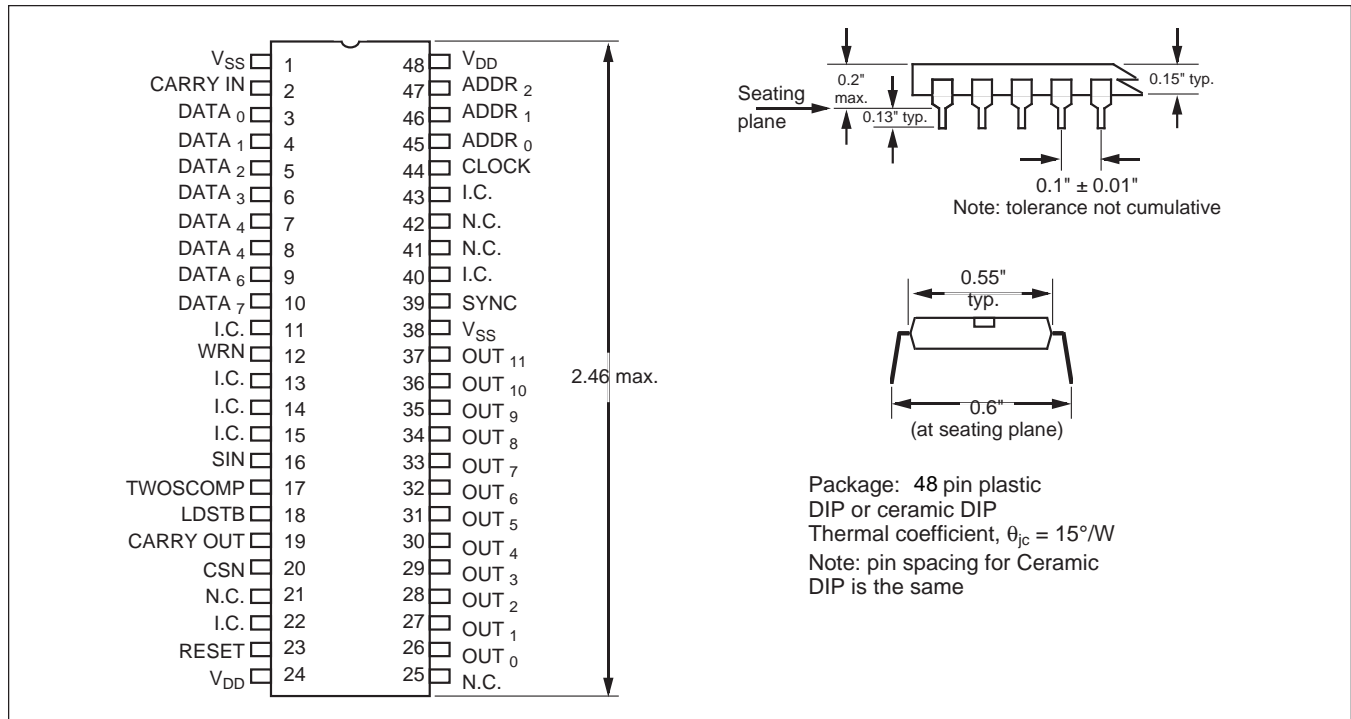
$$f_o = \frac{f_c \times \Delta\text{-Phase}}{2^{48}}$$

where: f_o is the frequency of the output signal
and: f_c is the clock frequency.

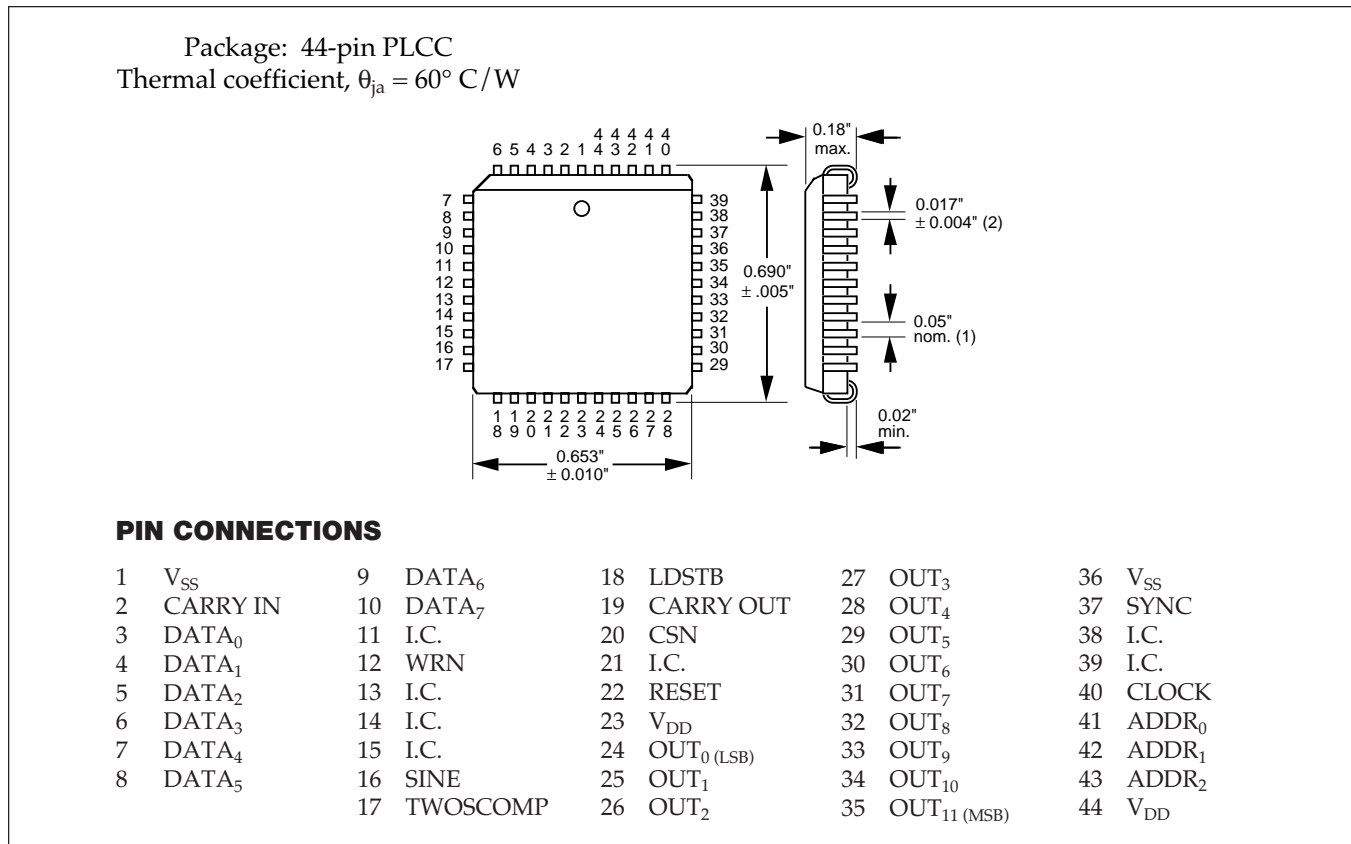
BLOCK DIAGRAM



PIN CONFIGURATION -- STEL-1173/CL



PIN CONFIGURATION -- STEL-1173/CM



- Notes:
1. Tolerances on pin spacing are not cumulative.
 2. I.C. denotes Internal Connection. These pins must be left unconnected. Do not use for vias.
 3. N.C. denotes No Connection. These pins may be used for vias.

CIRCUIT DESCRIPTION

The sine and cosine functions are generated from the 13 most significant bits of the phase accumulator. The frequency of the NCO is determined by the number stored in the Δ -Phase register which may be programmed by an eight-bit microprocessor.

The frequency programming capability of the NCO is analogous to sampling a sine wave where the sampling function is the clock. If the output frequency is very low with respect to the clock ($< f_c / 8096$), then the NCO output will sequence through each of the 8096 states of the sine function. As the output frequency is increased with respect to the clock the sine function will appear to be more discontinuous since there will be fewer samples in each cycle. At the Nyquist limit, when the output frequency is exactly half the clock, the output waveform reduces to a square wave. The practical upper limit of the NCO output frequency is about 40% of the clock frequency because spurious components created by sampling, which are at a frequency greater than half the clock frequency, become difficult to remove by filtering.

The phase noise of the NCO output signal may be determined by knowing the phase noise of the clock signal input, and the ratio of the output frequency to the clock frequency. This ratio squared times the phase noise power of the clock specified in a given bandwidth is the phase noise power that may be expected in that same bandwidth relative to the output frequency.

The NCO achieves its high operating frequency by making extensive use of pipelining in its architecture. The pipeline delays within the NCO represent 20 clock cycles. This effectively limits the minimum possible frequency switching period of the NCO. After new frequency data is entered, the load command is given. After the 20 cycle pipeline delay, the output will instantaneously switch frequency while maintaining phase coherence. After this, the next new frequency may be entered. If a 50 MHz clock were utilized, the NCO could be continuously switched between programmed frequencies with a minimum practical average switching time of about 0.4 μ sec.

FUNCTION BLOCK DESCRIPTION

ADDRESS SELECT LOGIC BLOCK

This block controls the writing of data into the device via the **DATA₇₋₀** inputs. The data is written into the device on the rising edge of the **WRN** input, and the register into which the data is written is selected by the **ADDR₂₋₀** inputs. The writing of data is also controlled with the **CSN** input; this input must be low to enable writing.

BUFFER REGISTER BLOCK

The Buffer Register is used to temporarily store the Δ -Phase data written into the device. This allows the data to be written asynchronously as six bytes per 48-bit Δ -Phase word. The data is transferred from this register into the Δ -Phase Register after a falling edge on the **LDSTB** input.

Δ -PHASE REGISTER BLOCK

This block controls the updating of the Δ -Phase word used in the Accumulator. The frequency data from the Buffer Register Block is loaded into this block after a falling edge on the **LDSTB** input. The **SYNC** output, which indicates the instant of frequency change at the output at the end of the pipeline delay, is generated in this block.

PHASE ACCUMULATOR BLOCK

This block forms the core of the NCO function. It is a high-speed, pipelined, 48-bit parallel accumulator, generating a new sum in every clock cycle. A carry input (**CARRY IN**) allows the resolution of the accumulator to be expanded by means of an auxiliary NCO or phase accumulator. The overflow signal is discarded (and is available at the **CARRY OUT** pin), since the required output is the modulo (2^{48}) sum only. This represents the modulo (2π) phase angle.

SINE LOOKUP TABLE BLOCK

This block is the sine memory. The 13 most significant bits from the Phase Accumulator are used to address this memory to generate the 12-bit **OUT₁₁₋₀** outputs.

INPUT SIGNALS

RESET

The **RESET** input is asynchronous and active low. When **RESET** goes low, all registers including the 48-bit input buffer are cleared within 30 nsecs. The data on the **OUT₁₁₋₀** bus will then be invalid for 6 clock cycles, and thereafter will remain at the value corresponding to zero phase, i.e., 2049 (801H), until a new frequency is loaded into the Δ -Phase register with a **LDSTB** command after the **RESET** returns to a logic one.

CLOCK

All synchronous functions performed within the NCO are referenced to the rising edge of the **CLOCK** input. The **CLOCK** signal should be nominally a square wave at a maximum frequency of 50 MHz. A non-repetitive **CLOCK** waveform is permissible as long as the minimum duration positive or negative pulse on the waveform is always greater than 8 nanoseconds. At each positive transition of the **CLOCK** signal, the number stored in the Δ -Phase register is added to the contents of the phase accumulator and the result is placed in the phase accumulator.

WRN

On the rising edge of the **WRN** input, the information on the 8-bit data bus is transferred to the buffer register selected by the **ADDR₂₋₀** bus.

CSN

The **CSN** (Chip Select) input is active low and can be used to control the writing of data into the chip. When this input is high all data writing via the **DATA₇₋₀** bus is inhibited.

ADDR₂ through ADDR₀

The three address lines **ADDR₂₋₀** control the use of the **DATA₇₋₀** bus for writing frequency data to the Δ -Phase buffer registers as shown in the table below:

ADDR ₂	ADDR ₁	ADDR ₀	Δ -Phase Register Field
0	0	0	Bits0 (LSB) –7
0	0	1	Bits 8–15
0	1	0	Bits 16–23
0	1	1	Bits 24–31
1	0	0	Bits 32–39
1	0	1	Bits 40–47 (MSB)

To write to all 48 bits of the phase write registers, the **DATA₇₋₀** bus must be used 6 times. Note that it is not necessary to reload unchanged bytes, and that the byte loading sequence may be random.

DATA₇ through DATA₀

The eight bit **DATA₇₋₀** bus is used to program the 48-bit Δ -Phase register. **DATA₀** is the least significant bit of the bus.

LDSTB

On the rising edge of the clock following the falling edge of the **LDSTB** input, the information in the 48-bit buffer register is transferred to the Δ -Phase register. The frequency of the NCO output will change 20 clock cycles after the **LDSTB** command due to pipelining delays.

CARRY IN

Normal operation of the NCO requires that **CARRY IN** be set at a logic 0. When **CARRY IN** is a logic 1, the effective value of the Δ -Phase register is increased by one. Two NCOs can be cascaded together to obtain 96 bits of frequency resolution by using the **CARRY OUT** of the lower order NCO and the **CARRY IN** of the higher order NCO.

TWOSCOMP

When the **TWOSCOMP** input is set high, the data appearing on the **OUT₁₁₋₀** bus is presented in two's complement code, and when it is set low, the data is presented in offset binary code. The limits of the data values in both codes is shown below:

Code →	Offset binary	2's Complement
Minimum value	+1 (001 _H)	– 2047 (801 _H)
Maximum value	+4095 (FFF _H)	+2047 (7FF _H)
Mean value	+2048 (800 _H)	0 (000 _H)

Both number formats produce sine or cosine waves which are symmetrical about the phase quadrant axis and the mean-value magnitude axis.

SINE

When the **SINE** input signal is set to a logic low level, the output signal appearing on the **OUT₁₁₋₀** bus is the cosine of the 48-bit accumulator's 13 most significant bits (bits 47-35, with 47 being the MSB). Normally set high, this signal allows the NCO to generate either sine or cosine signals. By using two devices, one set in the sine mode and the other set in the cosine mode, quadrature outputs may be obtained. The quadrature phase relationship of the two outputs will be maintained at all times provided the two devices are reset simultaneously and operate from a common clock signal.

A high level on the **SINE** input sets the output to be the sine of the 48-bit accumulator's 13 most significant bits. The value of the output for a given phase value follows the relationship:

$$2's \text{ comp} = 2047 \times \sin(360 \times \text{phase})$$

$$\text{offset bin} = 2047 \times \sin(360 \times \text{phase}) + 2048$$

The result is accurate to within 1 LSB.

When this input is set low the output will be the cosine of the 48-bit accumulator's 13 most significant bits. The value of the output for a given phase value follows the relationship:

$$2's \text{ comp} = 2047 \times \cos(360 \times \text{phase})$$

$$\text{offset bin} = 2047 \times \cos(360 \times \text{phase}) + 2048$$

again, accurate to within 1 LSB.

OUTPUT SIGNALS

OUT₁₁₋₀

The signal appearing on the OUT₁₁₋₀ bus is derived from the 13 most significant bits of the phase accumulator. The 12-bit sine or cosine function is presented in offset binary or two's complement format, depending on the status of the TWOSCOMP input. When the phase accumulator is zero, e.g., after a reset, the decimal value of the output is 2049 in offset binary and 1 in two's complement. The nominal phase (in degrees) of the sine wave output may be determined at any point by multiplying the decimal equivalent of the 13 most significant bits of the phase accumulator by (360/8192) and then adding (360/16384). OUT₁₁ is the MSB, and OUT₀ is the LSB.

CARRY OUT

Each time the contents of the phase accumulator exceeds the maximum value that can be represented by a 48 bit number the CARRY OUT signal goes high for one clock cycle.

SYNC

The normally high SYNC output goes low for one clock cycle, 20 clock cycles after a LDSTB command, to indicate the end of the pipeline delay and the start of the new steady state condition.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Warning: Stresses greater than those shown below may cause permanent damage to the device.

Exposure of the device to these conditions for extended periods may also affect device reliability. All voltages are referenced to V_{SS}

Symbol	Parameter	Range	Units
T _{stg}	Storage Temperature	−40 to +125	°C (Plastic package)
V _{DDmax}	Supply voltage on V _{DD}	−0.3 to +7	volts
V _{I(max)}	Input voltage	−0.3 to V _{DD} + 0.3	volts
I _i	DC input current	± 10	mA

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Range	Units
V _{DD}	Supply Voltage	+5 ± 5%	Volts (Commercial)
T _a	Operating Temperature (Ambient)	0 to +70	°C (Commercial)

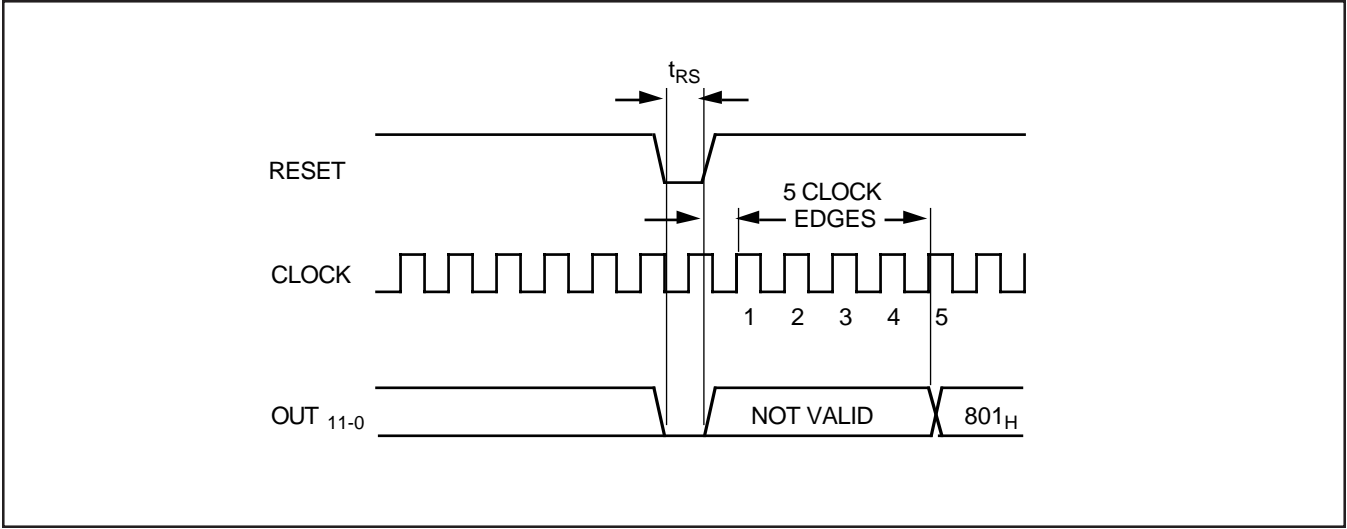
D.C. CHARACTERISTICS (Operating Conditions: $V_{DD} = 5.0\text{ V} \pm 5\%$, $V_{SS} = 0\text{ V}$, $T_a = 0^\circ\text{ to }70^\circ\text{ C}$, Commercial)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_{DD(Q)}$	Supply Current, Quiescent			1.0	mA	Static, no clock
I_{DD}	Supply Current, Operational			3.0	mA/MHz	
$V_{IH(min)}$	High Level Input Voltage					
	Standard Operating Conditions	2.0			volts	Logic '1'
	Extended Operating Conditions	2.25			volts	Logic '1'
$V_{IL(max)}$	Low Level Input Voltage			0.8	volts	Logic '0'
$I_{IH(min)}$	High Level Input Current	10	35	110	μA	CIN and CSEL , $V_{IN} = V_{DD}$
$I_{IH(max)}$	High Level Input Current			10	μA	All other inputs, $V_{IN} = V_{DD}$
$I_{IL(max)}$	Low Level Input Current			-10	μA	CIN and CSEL , $V_{IN} = V_{SS}$
$I_{IL(min)}$	Low Level Input Current	-15	-45	-130	μA	All other inputs, $V_{IN} = V_{SS}$
$V_{OH(min)}$	High Level Output Voltage	2.4	4.5		volts	$I_O = -4.0\text{ mA}$
$V_{OL(max)}$	Low Level Output Voltage		0.2	0.4	volts	$I_O = +4.0\text{ mA}$
I_{OS}	Output Short Circuit Current	20	65	130	mA	$V_{OUT} = V_{DD}$, $V_{DD} = \text{max}$
		-10	-45	-130	mA	$V_{OUT} = V_{SS}$, $V_{DD} = \text{max}$
C_{IN}	Input Capacitance		2		pF	All inputs
C_{OUT}	Output Capacitance		4		pF	All outputs

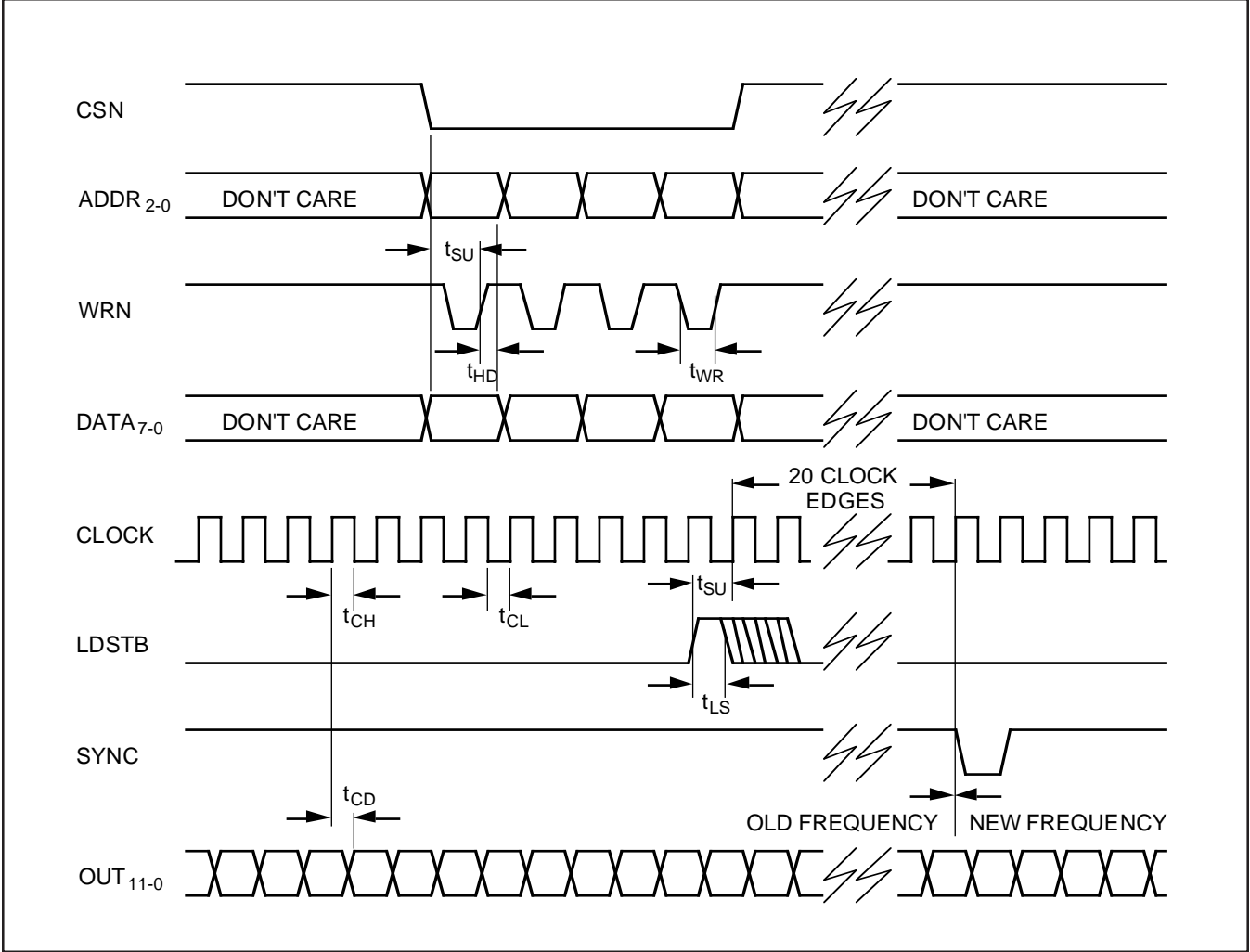
A.C. CHARACTERISTICS (Operating Conditions: $V_{DD} = 5.0\text{ V} \pm 5\%$, $V_{SS} = 0\text{ V}$, $T_a = 0^\circ\text{ to }70^\circ\text{ C}$, Commercial)

		STEL-1173			
		(Commercial)			
Symbol	Parameter	Min.	Max	Units	Conditions
t_{RS}	RESET pulse width	30		nsec.	
t_{SR}	RESET to CLOCK Setup	10		nsec.	
t_{SU}	DATA , ADDR or CSEL to WRN Setup, and LDSTB to CLOCK Setup	18		nsec.	
t_{HD}	DATA , ADDR or CSEL to WRN Hold, and LDSTB to CLOCK Hold	12		nsec.	
t_{CH}	CLOCK high	8		nsec.	$f_{CLK} = \text{max.}$
t_{CL}	CLOCK low	8		nsec.	$f_{CLK} = \text{max.}$
t_W	WRN or FRLD pulse width	20		nsec.	
t_{CD}	CLOCK to output delay	5	10	nsec.	Load = 15 pF

NCO RESET SEQUENCE

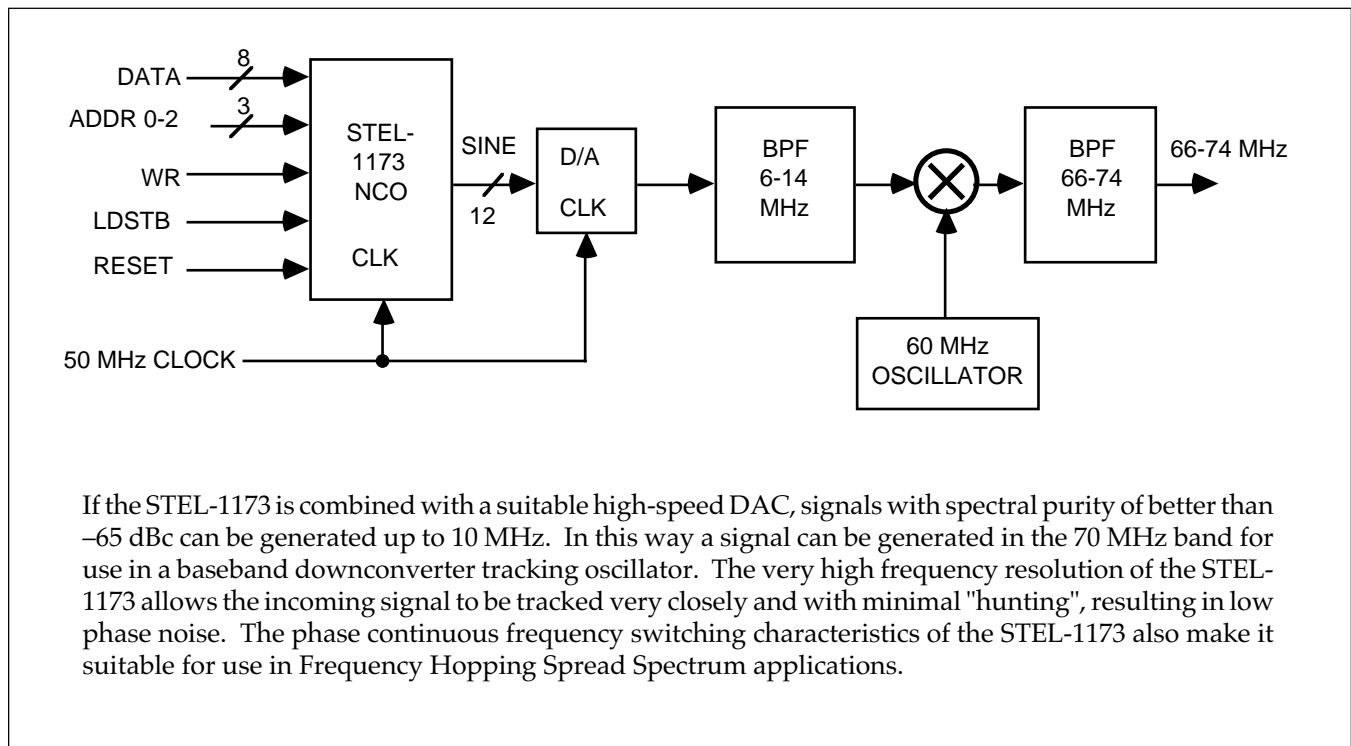


NCO FREQUENCY CHANGE



TYPICAL APPLICATION

HIGH PURITY, HIGH RESOLUTION SYNTHESIZER



SPECTRAL PURITY

In many applications the NCO is used with a Digital to Analog converter (DAC) to generate an analog waveform which approximates an ideal sinewave. The spectral purity of this synthesized waveform is a function of many variables including the phase and amplitude quantization, the ratio of the clock frequency to output frequency, and the dynamic characteristics of the DAC.

The signals generated by the STEL-1173 have 12 bits of amplitude resolution and 13 bits of phase resolution which results in spurious levels which are theoretically

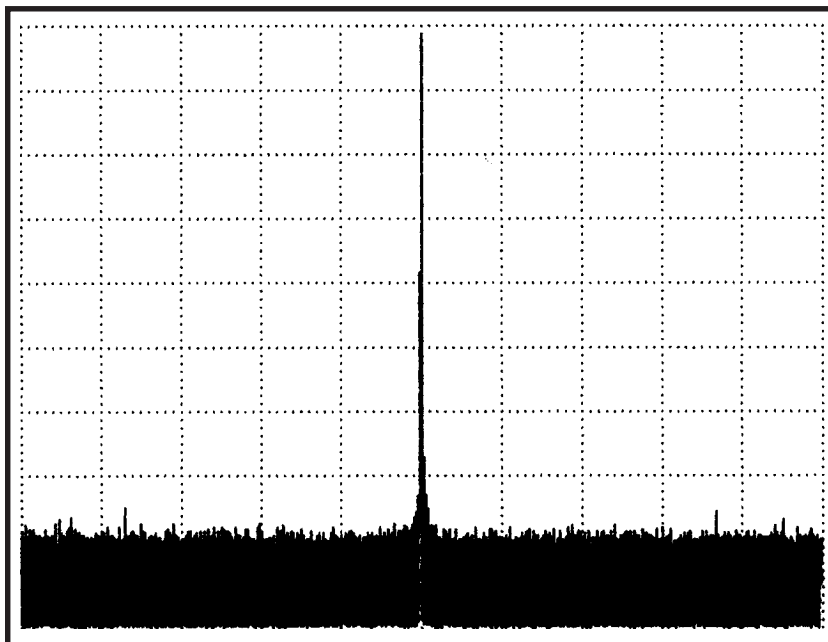
about -75 dBc. The highest output frequency the NCO can generate is half the clock frequency ($f_c/2$), and the spurious components at frequencies greater than $f_c/2$ can be removed by filtering. As the output frequency f_o of the NCO approaches $f_c/2$, the "image" spur at $f_c - f_o$ (created by the sampling process) also approaches $f_c/2$ from above. If the programmed output frequency is very close to $f_c/2$ it will be virtually impossible to remove this image spur by filtering. For this reason, the maximum practical output frequency of the NCO should be limited to about 40% of the clock frequency.

A spectral plot of the NCO output after conversion with a DAC (Sony CX20202A-1) is shown below. In this case, the clock frequency is 50 MHz and the output frequency is programmed to 6.789 MHz. This 10-bit DAC gives better performance than any of the currently available 12-bit DACs at clock frequencies higher than 10 or 20 MHz. The maximum non-harmonic spur level observed over the output frequency range shown in this case is -74 dBc. The spur levels are limited by the dynamic linearity of the DAC. It is important to remember that when the output frequency exceeds 25% of the clock frequency, the second harmonic frequency will be higher than the Nyquist frequency, 50% of the clock frequency. When this happens, the image of the harmonic at the

frequency $f_c - 2f_o$, which is not harmonically related to the output signal, will become intrusive since its frequency falls as the output frequency rises, eventually crossing the fundamental output when its frequency crosses through $f_c/3$. It would be necessary to select a DAC with better dynamic linearity to improve the harmonic spur levels. (The dynamic linearity of a DAC is a function of both its static linearity and its dynamic characteristics, such as settling time and slew rates.) At higher output frequencies the waveform produced by the DAC will have large output changes from sample to sample. For this reason, the settling time of the DAC should be short in comparison to the clock period. As a general rule, the DAC used should have the lowest possible glitch energy as well as the shortest possible settling time.

TYPICAL SPECTRUM

Center Frequency: 6.7 MHz
 Frequency Span: 10.0 MHz
 Reference Level: -5 dBm
 Resolution Bandwidth: 1 KHz
 Video Bandwidth: 3 kHz
 Scale: Log, 10 dB/div
 Output frequency: 6.789 MHz
 Clock frequency: 50 MHz



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For Further Information Call or Write



INTEL CORPORATION

Cable Network Operation

350 E. Plumeria Drive, San Jose, CA 95134

Customer Service Telephone: (408) 545-9700

Technical Support Telephone: (408) 545-9799

FAX: (408) 545-9888