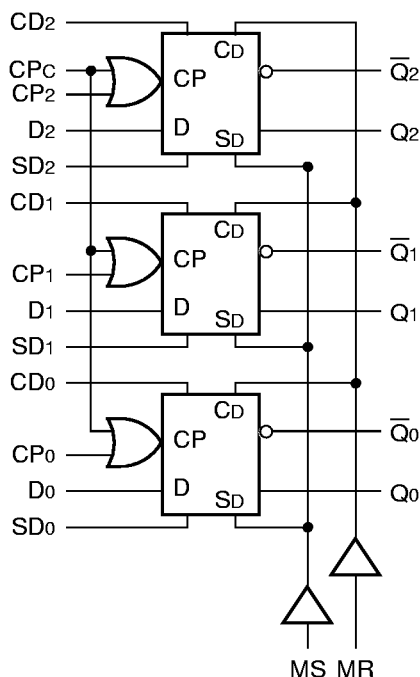


FEATURES

- Max. toggle frequency of 800MHz
- Differential outputs
- IEE min. of -80mA
- Industry standard 100K ECL levels
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75K Ω input pull-down resistors
- 150% faster than National or Signetics
- 40% lower power than National or Signetics
- Function and pinout compatible with National and Signetics F100K
- ESD protection of 2000V
- Available in 24-pin CERPDP, 24-pin CERPAC and 28-pin PLCC packages

BLOCK DIAGRAM

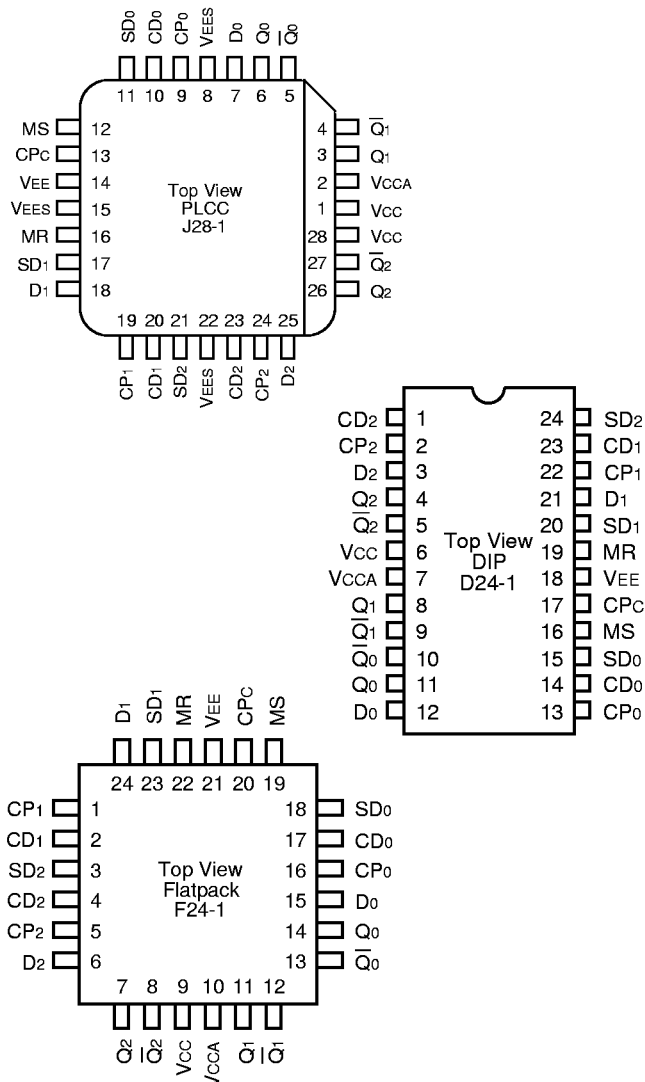


DESCRIPTION

The SY100S331 offers three D-type, edge-triggered master/slave flip-flops with true and complement outputs, designed for use in high-performance ECL systems. Each flip-flop is controlled by a common clock (CP_c), as well as its own clock pulse (CP_n). The resultant clock signal controlling the flip-flop is the logical OR operation of these two clock signals. Data enters the master when both CP_c and CP_n are LOW and enters the slave on the rising edge of either CP_c or CP_n (or both).

Additional control signals include Master Set (MS) and Master Reset (MR) inputs. Each flip-flop also has its own Direct Set (SD_n) and Direct Clear (CD_n) signals. The MR, MS, SD_n and DC_n signals override the clock signals. The inputs on this device have 75K Ω pull-down resistors.

PIN CONFIGURATIONS



PIN NAMES

Pin	Function
CP ₀ – CP ₂	Individual Clock Inputs
CP _c	Common Clock Input
D ₀ – D ₂	Data Inputs
CD ₀ – CD ₂	Individual Direct Clear Inputs
SD _n	Individual Direct Set Inputs
MR	Master Reset Input
MS	Master Set Input
Q ₀ – Q ₂	Data Outputs
$\overline{Q}_0$ – $\overline{Q}_2$	Complementary Data Outputs
VEES	VEE Substrate
VCCA	VCCO for ECL Outputs

TRUTH TABLES

Asynchronous Operation ⁽¹⁾					
Inputs					Outputs
D _n	CP _n	CP _c	MS SD _n	MR DC _n	Q _n (t+1)
X	X	X	H	L	H
X	X	X	L	H	L
X	X	X	H	H	U

NOTE:

1. H = High Voltage Level, L = Low Voltage Level, X = Don't Care, U = Undefined, t = Time before CP Positive Transition, t+1 = Time after CP Positive Transition, u = Low-to-High Transition

Synchronous Operation ⁽¹⁾					
Inputs					Outputs
D _n	CP _n	CP _c	MS SD _n	MR DC _n	Q _n
L	u	L	L	L	L
H	u	L	L	L	H
L	L	u	L	L	L
H	L	u	L	L	H
X	L	L	L	L	Q _n (t)
X	H	X	L	L	Q _n (t)
X	X	H	L	L	Q _n (t)

NOTE:

1. H = High Voltage Level, L = Low Voltage Level, X = Don't Care, U = Undefined, t = Time before CP Positive Transition, t+1 = Time after CP Positive Transition, u = Low-to-High Transition

DC ELECTRICAL CHARACTERISTICS

VEE = –4.2V to –5.5V unless otherwise specified, VCC = VCCA = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I _{IH}	Input HIGH Current, All Inputs	—	—	200	μA	V _{IN} = V _{IH} (Max.)
I _{EE}	Power Supply Current	–80	–65	–35	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERDIP

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = 0^{\circ}C$		$T_A = +25^{\circ}C$		$T_A = +85^{\circ}C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
f_{max}	Toggle Frequency	800	—	800	—	800	—	MHz	
t_{PLH} t_{PHL}	Propagation Delay CP_C to Output	300	900	300	900	300	900	ps	
t_{PLH} t_{PHL}	Propagation Delay CP_n to Output	300	900	300	900	300	900	ps	
t_{PLH} t_{PHL}	Propagation Delay CD_n , SD_n to Output	300	1000	300	1000	300	1000	ps	
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	300	1100	300	1100	300	1100	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
t_s	Set-up Time D_n	400	—	400	—	400	—	ps	
	CD_n , SD_n (Release Time)	500	—	500	—	500	—		
	MS, MR (Release Time)	800	—	800	—	800	—		
t_H	Hold Time D_n	300	—	300	—	300	—	ps	
$t_{pw} (H)$	Pulse Width HIGH CP_n , CP_C , DC_n SD_n , MR, MS	800	—	800	—	800	—	ps	

CERPACK

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = 0^{\circ}C$		$T_A = +25^{\circ}C$		$T_A = +85^{\circ}C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
f_{max}	Toggle Frequency	800	—	800	—	800	—	MHz	
t_{PLH} t_{PHL}	Propagation Delay CP_C to Output	300	800	300	800	300	800	ps	
t_{PLH} t_{PHL}	Propagation Delay CP_n to Output	300	800	300	800	300	800	ps	
t_{PLH} t_{PHL}	Propagation Delay CD_n , SD_n to Output	300	900	300	900	300	900	ps	
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	300	1000	300	1000	300	1000	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
t_s	Set-up Time D_n	400	—	400	—	400	—	ps	
	CD_n , SD_n (Release Time)	500	—	500	—	500	—		
	MS, MR (Release Time)	800	—	800	—	800	—		
t_H	Hold Time D_n	300	—	300	—	300	—	ps	
$t_{pw} (H)$	Pulse Width HIGH CP_n , CP_C , DC_n SD_n , MR, MS	800	—	800	—	800	—	ps	

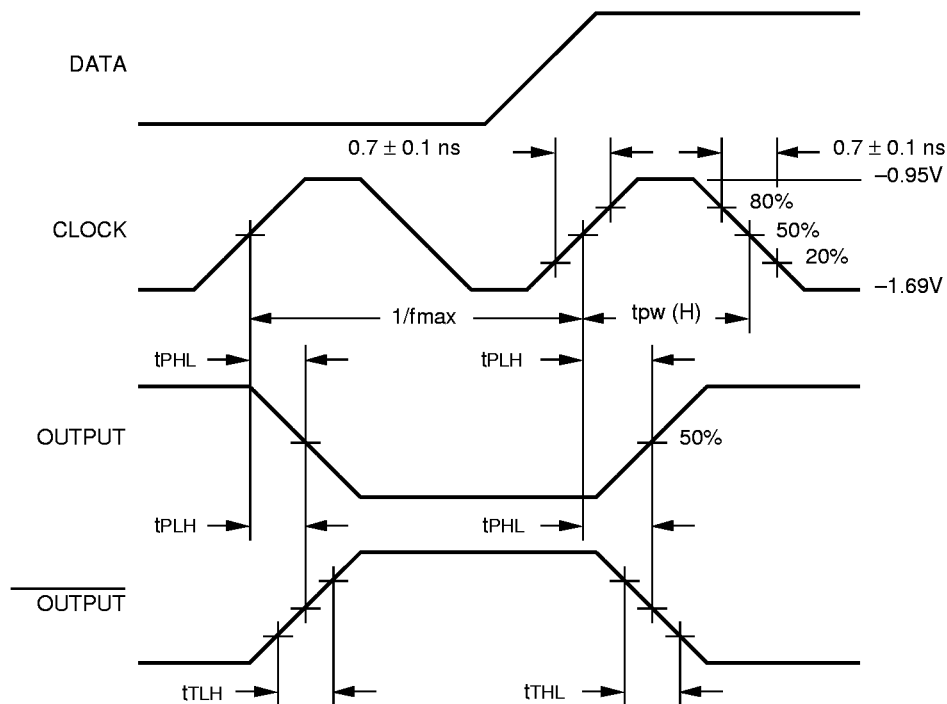
AC ELECTRICAL CHARACTERISTICS (Continued)

PLCC

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = 0^{\circ}C$		$T_A = +25^{\circ}C$		$T_A = +85^{\circ}C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
f_{max}	Toggle Frequency	800	—	800	—	800	—	MHz	
t_{PLH} t_{PHL}	Propagation Delay CP_c to Output	300	700	300	700	300	700	ps	
t_{PLH} t_{PHL}	Propagation Delay CP_n to Output	300	700	300	700	300	700	ps	
t_{PLH} t_{PHL}	Propagation Delay CD_n , SD_n to Output	300	800	300	800	300	800	ps	
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	300	900	300	900	300	900	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
t_s	Set-up Time D_n CD_n , SD_n (Release Time) MS, MR (Release Time)	400 500 800	— — —	400 500 800	— — —	400 500 800	— — —	ps	
t_H	Hold Time D_n	300	—	300	—	300	—	ps	
$t_{pw} (H)$	Pulse Width HIGH CP_n , CP_c , DC_n SD_n , MR, MS	800	—	800	—	800	—	ps	

TIMING DIAGRAMS

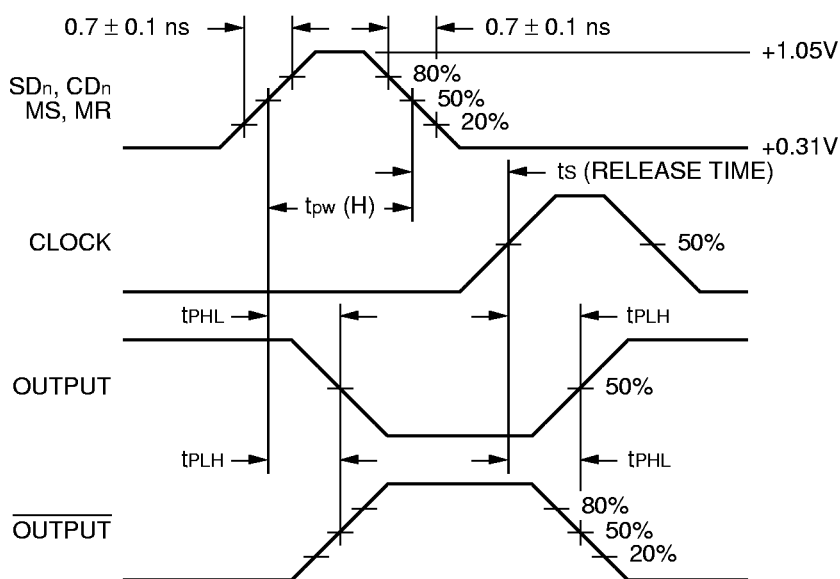


Propagation Delay (Clock) and Transition Times

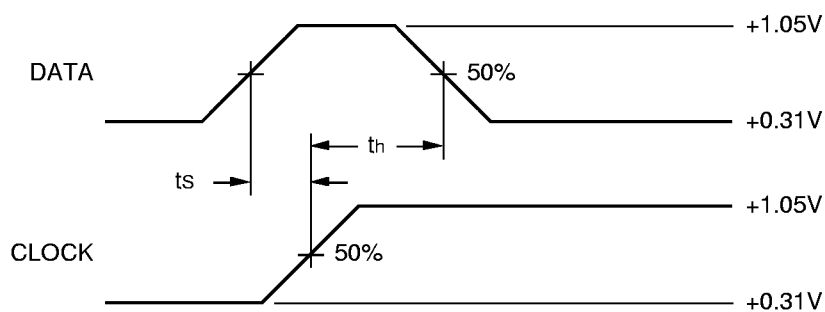
NOTE:

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

TIMING DIAGRAMS (Continued)



Propagation Delay (Sets and Resets)



Data Setup and Hold Time

NOTES:

t_s is the minimum time before the transition of the clock that information must be present at the data input.

t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

PRODUCT ORDERING CODE

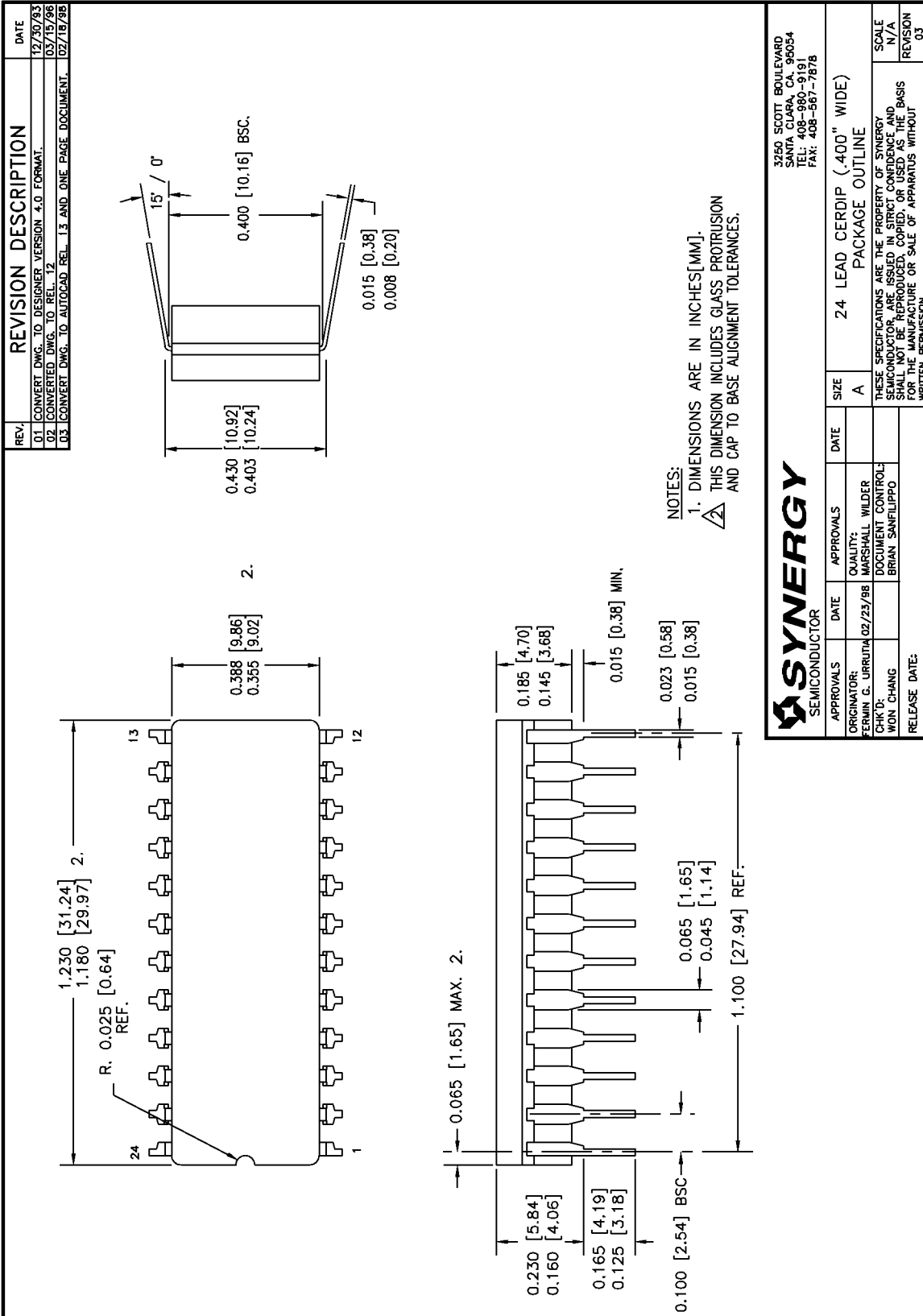
Ordering Code	Package Type	Operating Range
SY100S331DC	D24-1	Commercial
SY100S331FC	F24-1	Commercial
SY100S331JC	J28-1	Commercial
SY100S331JCTR	J28-1	Commercial

24 LEAD Cerdip (D24-1)

FILE/REV #: PD0003A03

PD/0003/ASCORP

PAGE 1 OF 1

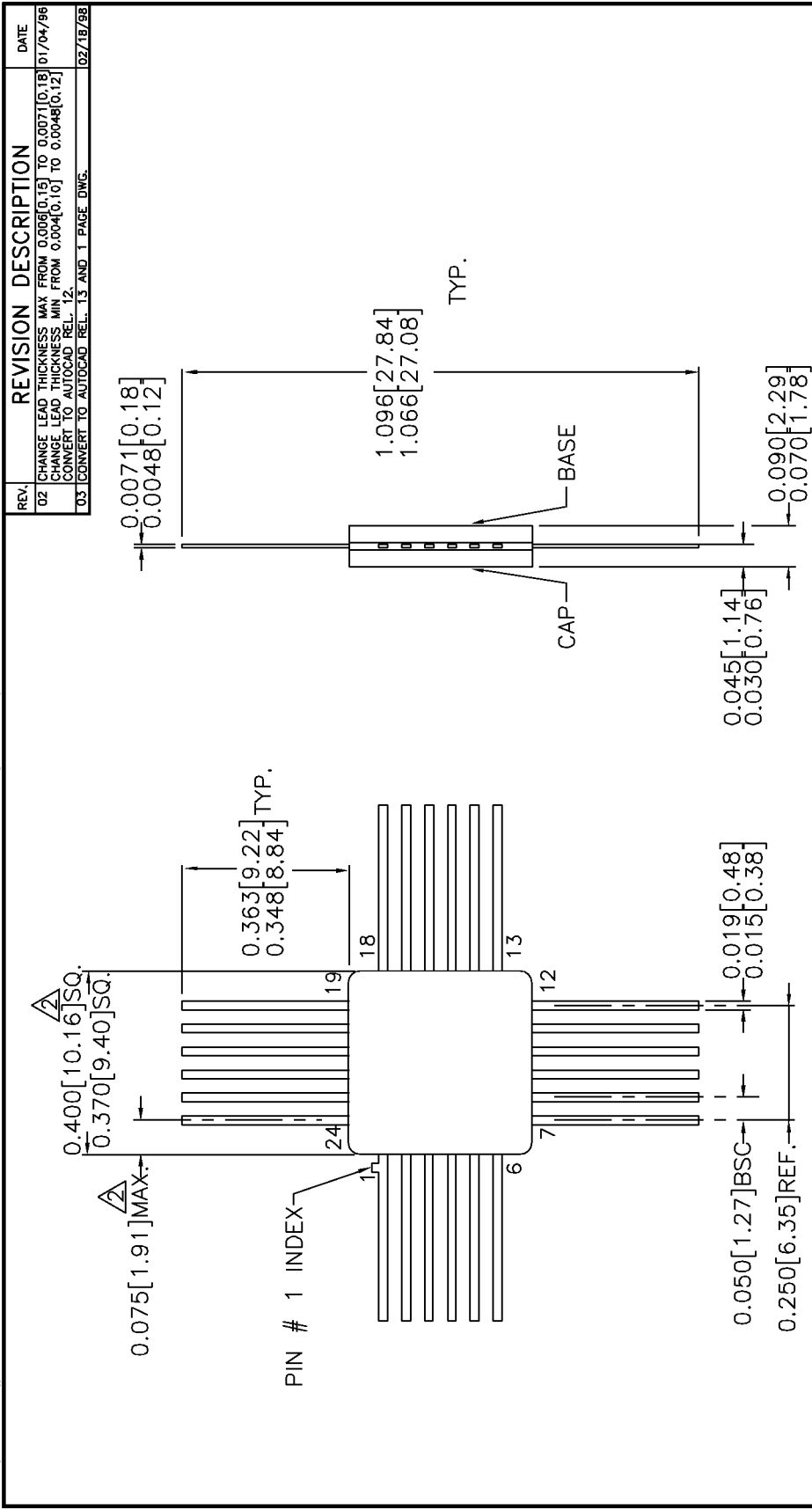


24 LEAD CERPACK (F24-1)

FILE/REV #: PD0006A03

PD/0006/ASCORP

PAGE 1 OF 1



NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.



3250 SCOTT BOULEVARD
SANTA CLARA, CA 95054
TEL: 408-980-9191
FAX: 408-567-7878

APPROVALS	DATE	APPROVALS	DATE	SIZE	24 LEAD CERPACK
ORIGINATOR: FERMIN G. URRUTIA	02/23/98	QUALITY: MARSHALL WILDER		A	PACKAGE OUTLINE
CHK'D: WON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO			
RELEASE DATE:					

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28 LEAD PLASTIC LEADED CHIP CARRIER (J28-1)

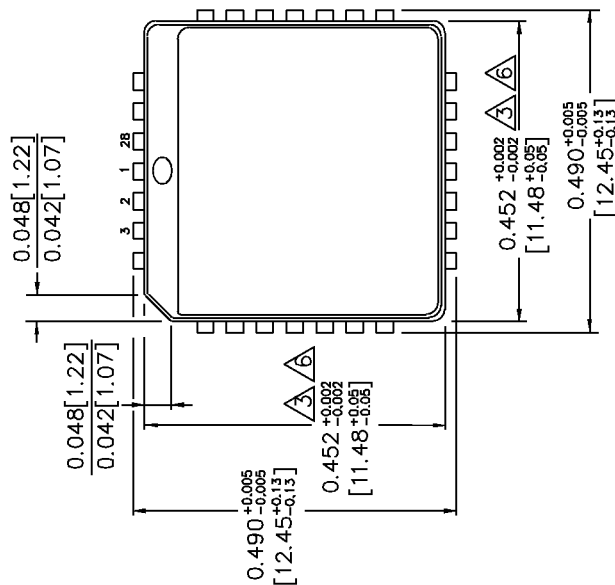
FILE/REV #: PD0008A03

PD/0008/ASCORP

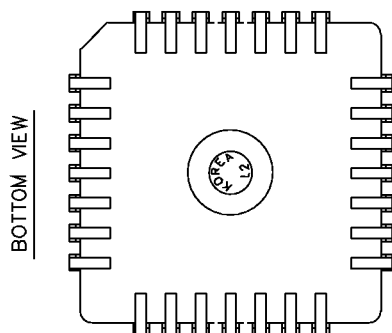
PAGE 1 OF 1

REV.	REVISION DESCRIPTION	DATE
01	CONVERT TO DESIGNER VERSION 4.0 FORMAT. ADD COVER PAGE TO SPEC. CHANGE BODY WIDTH DIMENSION FROM 0.450(11.43) TO 0.443(11.25). TYPOGRAPHICAL ERROR.	08/18/94
02	CONVERT DWG FROM DESIGNER TO AUTOCAD REL. 12. REFERENCE AMKOR DWG. NO. 34856 REV. 00.	02/22/96
03	CONVERT DWG TO REL. 13 AND ONE PAGE DOCUMENT.	02/18/98

TOP VIEW



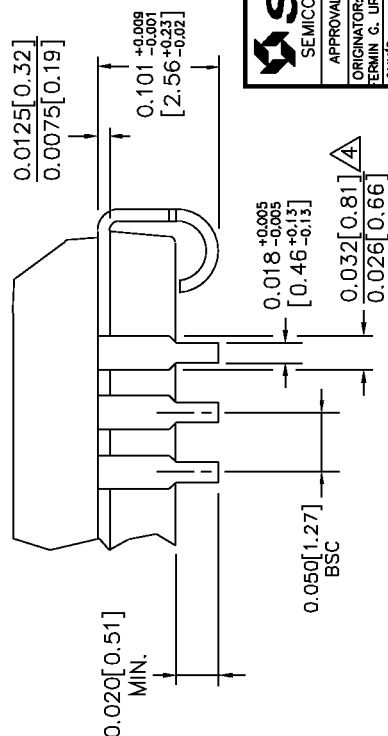
SIDE VIEW



BOTTOM VIEW

NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.



DETAIL "A"

SYNERGY
SEMICONDUCTOR

SEMI CONDUCTOR	APPROVALS	DATE	APPROVALS	DATE	SIZE	28 LEAD PLCC
	ORIGINATOR:	GURRUTIA	MARSHALL		A	PACKAGE OUTLINE
	CHK'D:	WON CHANG	DOCUMENT CONTROL: BRIAN SANFILIPPO			THESE SPECIFICATIONS ARE THE PROPERTY OF SYNERGY SEMICONDUCTOR, ARE ISSUED IN STRICT CONFIDENCE AND SHALL NOT BE REPRODUCED, COPIED, OR USED AS THE BASIS FOR THE MANUFACTURE OR SALE OF APPARATUS WITHOUT
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						REVISION 03

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