

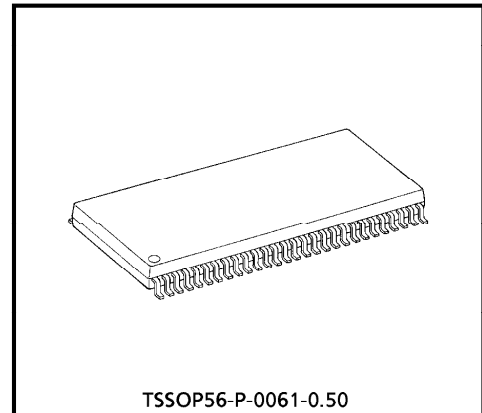
**TC74VCX16841FT****LOW-VOLTAGE 20-BIT D-TYPE LATCH  
WITH 3.6V TOLERANT INPUTS AND OUTPUTS**

The TC74VCX16841FT is a high performance CMOS 20-bit D-TYPE LATCH. Designed for use in 1.8, 2.5 or 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. It is also designed with over voltage tolerant inputs and outputs up to 3.6V.

The TC74VCX16841FT can be used as two 10-bit latches or one 20-bit latch. The 20 latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs. While the latch-enable (1LE or 2LE) input is high, the Q outputs of the corresponding 10-bit latch follow the D inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

When the  $\overline{OE}$  input is high, the outputs are in a high impedance state. This device is designed to be used with 3-state memory address drivers, etc.

All inputs are equipped with protection circuits against static discharge.



TSSOP56-P-0061-0.50

Weight : 0.25g (Typ.)

**FEATURES**

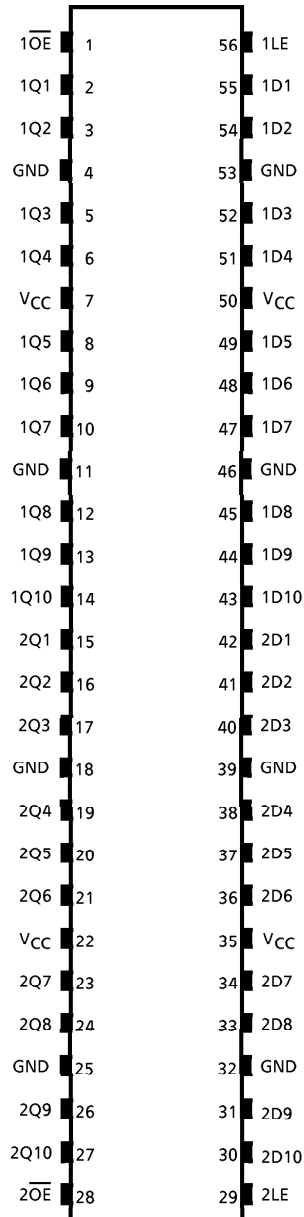
- Low Voltage Operation :  $V_{CC} = 1.8 \sim 3.6V$
- High Speed Operation :  $t_{pd} = TBD$  (max.) at  $V_{CC} = 3.0 \sim 3.6V$   
                                   :  $t_{pd} = TBD$  (max.) at  $V_{CC} = 2.3 \sim 2.7V$   
                                   :  $t_{pd} = TBD$  (max.) at  $V_{CC} = 1.8V$
- 3.6V Tolerant inputs and outputs.
- Output Current :  $I_{OH} / I_{OL} = \pm 24mA$  (min.) at  $V_{CC} = 3.0V$   
                           :  $I_{OH} / I_{OL} = \pm 12mA$  (min.) at  $V_{CC} = 2.3V$   
                           :  $I_{OH} / I_{OL} = \pm 6mA$  (min.) at  $V_{CC} = 1.8V$
- Latch-up Performance :  $\pm 300mA$
- ESD Performance : Human Body Model  $> \pm 2000V$   
                           : Machine Model  $> \pm 200V$
- Package : TSSOP  
                   (Thin Shrink Small Outline Package)
- Power Down Protection is provided on all inputs and outputs.

**PRELIMINARY**

961001EBA1

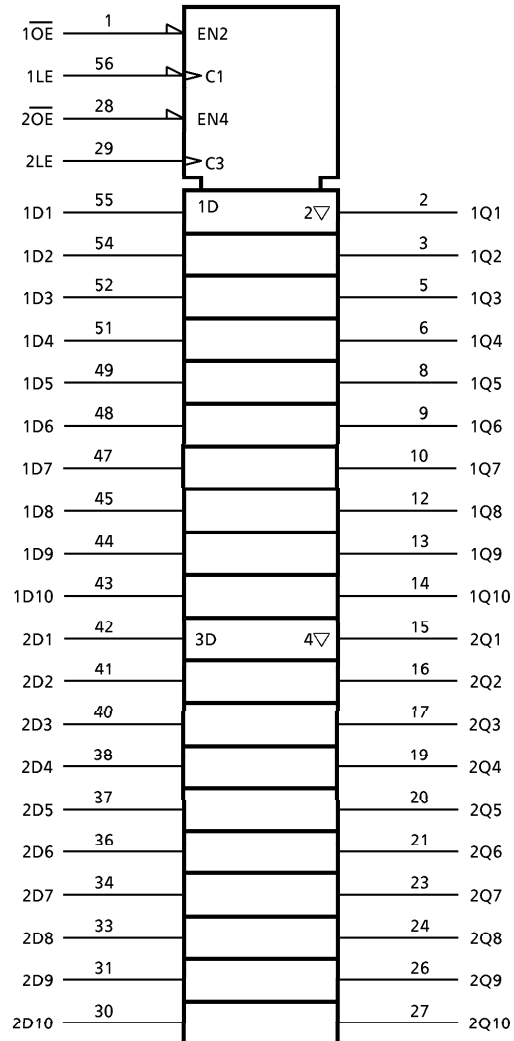
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PIN ASSIGNMENT



(TOP VIEW)

SYMBOL



**PRELIMINARY**

FUNCTION TABLE (each 10-bit latch)

INPUT			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q0
H	X	X	Z

**PRELIMINARY**

SYSTEM DIAGRAM

