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April 1, 2003

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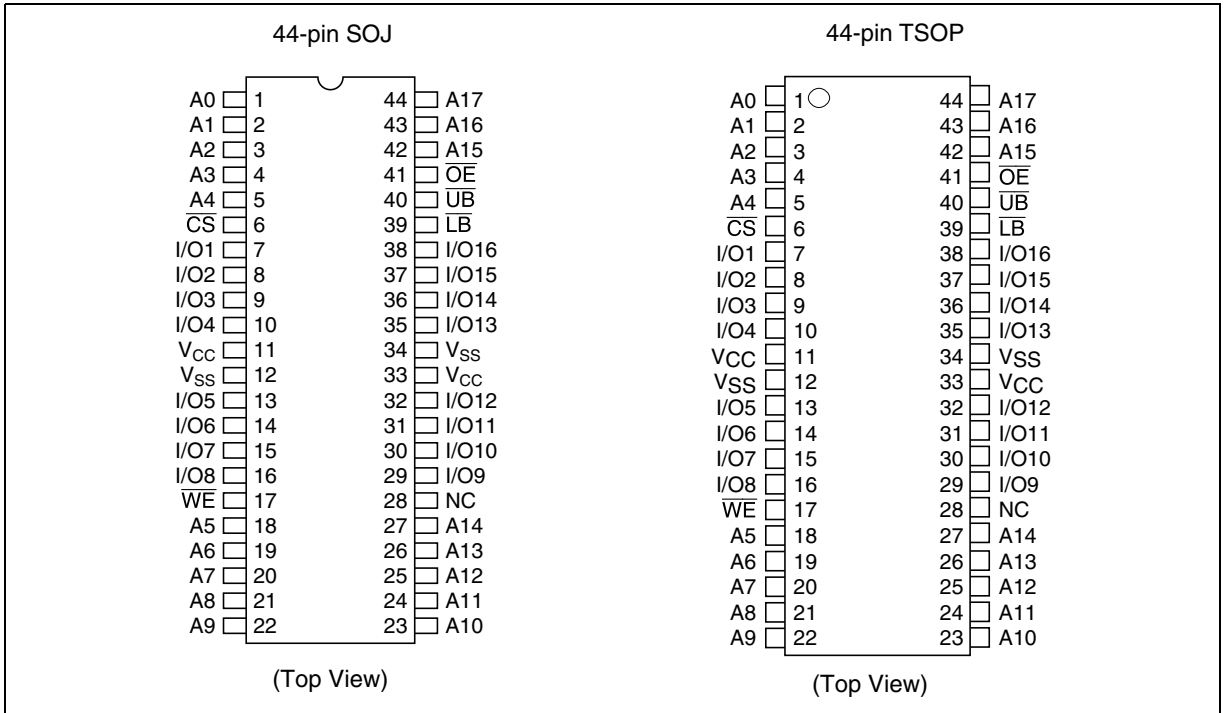
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## Ordering Information

Type No.	Access time	Device marking	Package
HM6216255HCJP-10	10 ns	HM6216255CJP10	400-mil 44-pin plastic SOJ (CP-44D)
HM6216255HCJP-12	12 ns	HM6216255CJP12	
HM6216255HCLJP-10	10 ns	HM6216255CLJP10	
HM6216255HCLJP-12	12 ns	HM6216255CLJP12	
HM6216255HCTT-10	10 ns	HM6216255CTT10	400-mil 44-pin plastic TSOPII (TTP-44DE)
HM6216255HCTT-12	12 ns	HM6216255CTT12	
HM6216255HCLTT-10	10 ns	HM6216255CLTT10	
HM6216255HCLTT-12	12 ns	HM6216255CLTT12	

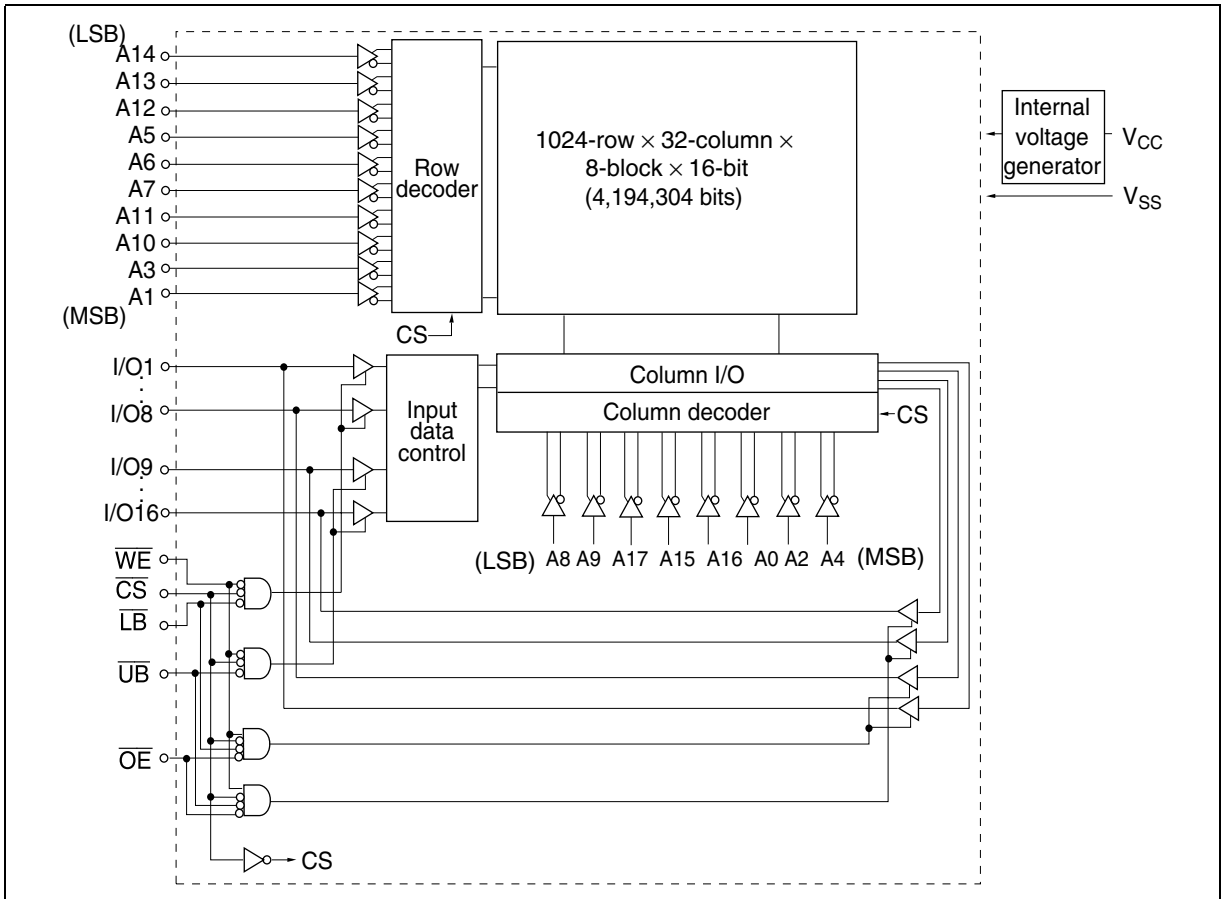
Pin Arrangement



Pin Description

Pin name	Function
A0 to A17	Address input
I/O1 to I/O16	Data input/output
CS	Chip select
OE	Output enable
WE	Write enable
UB	Upper byte select
LB	Lower byte select
V <sub>cc</sub>	Power supply
V <sub>ss</sub>	Ground
NC	No connection

## Block Diagram



## Operation Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	Mode	$V_{CC}$ current	I/O1–I/O8	I/O9–I/O16	Ref. cycle
H	x	x	x	x	Standby	$I_{SB}, I_{SB1}$	High-Z	High-Z	—
L	H	H	x	x	Output disable	$I_{CC}$	High-Z	High-Z	—
L	L	H	L	L	Read	$I_{CC}$	Output	Output	Read cycle
L	L	H	L	H	Lower byte read	$I_{CC}$	Output	High-Z	Read cycle
L	L	H	H	L	Upper byte read	$I_{CC}$	High-Z	Output	Read cycle
L	L	H	H	H	—	$I_{CC}$	High-Z	High-Z	—
L	x	L	L	L	Write	$I_{CC}$	Input	Input	Write cycle
L	x	L	L	H	Lower byte write	$I_{CC}$	Input	High-Z	Write cycle
L	x	L	H	L	Upper byte write	$I_{CC}$	High-Z	Input	Write cycle
L	x	L	H	H	—	$I_{CC}$	High-Z	High-Z	—

Note: H:  $V_{IH}$ , L:  $V_{IL}$ , x:  $V_{IH}$  or  $V_{IL}$

## Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to $V_{SS}$	$V_{CC}$	–0.5 to +7.0	V
Voltage on any pin relative to $V_{SS}$	$V_T$	–0.5* <sup>1</sup> to $V_{CC} + 0.5$ * <sup>2</sup>	V
Power dissipation	$P_T$	1.0	W
Operating temperature	$T_{opr}$	0 to +70	°C
Storage temperature	$T_{stg}$	–55 to +125	°C
Storage temperature under bias	$T_{bias}$	–10 to +85	°C

Notes: 1.  $V_T$  (min) = –2.0 V for pulse width (under shoot)  $\leq 6$  ns.

2.  $V_T$  (max) =  $V_{CC} + 2.0$  V for pulse width (over shoot)  $\leq 6$  ns.

## Recommended DC Operating Conditions

(Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}^{*3}$	4.5	5.0	5.5	V
	$V_{SS}^{*4}$	0	0	0	V
Input voltage	$V_{IH}$	2.2	—	$V_{CC} + 0.5^{*2}$	V
	$V_{IL}$	$-0.5^{*1}$	—	0.8	V

- Notes: 1.  $V_{IL}$  (min) = -2.0 V for pulse width (under shoot) ≤ 6 ns.  
 2.  $V_{IH}$  (max) =  $V_{CC} + 2.0$  V for pulse width (over shoot) ≤ 6 ns.  
 3. The supply voltage with all  $V_{CC}$  pins must be on the same level.  
 4. The supply voltage with all  $V_{SS}$  pins must be on the same level.

## DC Characteristics

(Ta = 0 to +70°C,  $V_{CC} = 5.0$  V ± 10%,  $V_{SS} = 0$  V)

Parameter	Symbol	Min	Typ <sup>*1</sup>	Max	Unit	Test conditions
Input leakage current	$ I_{LI} $	—	—	2	μA	$V_{IN} = V_{SS}$ to $V_{CC}$
Output leakage current	$ I_{LO} $	—	—	2	μA	$V_{IN} = V_{SS}$ to $V_{CC}$
Operation power supply current	10 ns cycle	$I_{CC}$	—	170	mA	Min cycle $\overline{CS} = V_{IL}$ , $I_{OUT} = 0$ mA
	12 ns cycle	$I_{CC}$	—	160	mA	Other inputs = $V_{IH}/V_{IL}$
Standby power supply current	$I_{SB}$	—	—	40	mA	Min cycle, $\overline{CS} = V_{IH}$ , Other inputs = $V_{IH}/V_{IL}$
	$I_{SB1}$	—	2.5	5	mA	$f = 0$ MHz $V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2$ V, (1) $0$ V ≤ $V_{IN} \leq 0.2$ V or (2) $V_{CC} \geq V_{IN} \geq V_{CC} - 0.2$ V
	— <sup>*2</sup>	—	0.6 <sup>*2</sup>	1.2 <sup>*2</sup>	—	—
Output voltage	$V_{OL}$	—	—	0.4	V	$I_{OL} = 8$ mA
	$V_{OH}$	2.4	—	—	V	$I_{OH} = -4$ mA

- Notes: 1. Typical values are at  $V_{CC} = 5.0$  V, Ta = +25°C and not guaranteed.  
 2. This characteristics is guaranteed only for L-version.

## Capacitance

(Ta = +25°C, f = 1.0 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance <sup>*1</sup>	$C_{IN}$	—	—	6	pF	$V_{IN} = 0$ V
Input/output capacitance <sup>*1</sup>	$C_{IO}$	—	—	8	pF	$V_{IO} = 0$ V

- Note: 1. This parameter is sampled and not 100% tested.

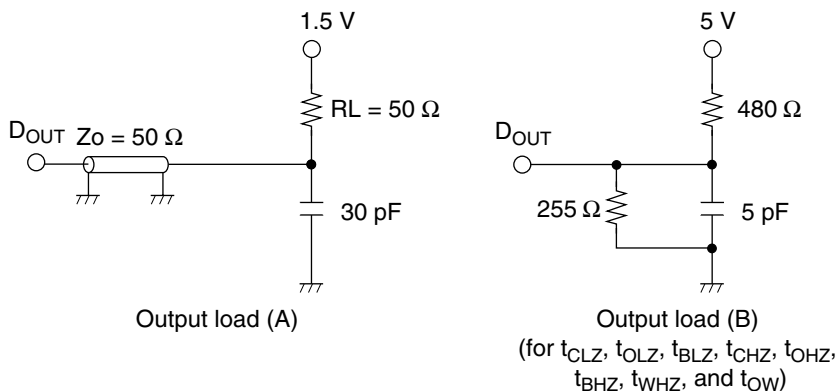


## AC Characteristics

( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ , unless otherwise noted.)

### Test Conditions

- Input pulse levels: 3.0 V/0.0 V
- Input rise and fall time: 3 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures (Including scope and jig)



### Read Cycle

Parameter	Symbol	HM6216255HC				Unit	Notes
		-10		-12			
		Min	Max	Min	Max		
Read cycle time	$t_{RC}$	10	—	12	—	ns	
Address access time	$t_{AA}$	—	10	—	12	ns	
Chip select access time	$t_{ACS}$	—	10	—	12	ns	
Output enable to output valid	$t_{OE}$	—	5	—	6	ns	
Byte select to output valid	$t_{BA}$	—	5	—	6	ns	
Output hold from address change	$t_{OH}$	3	—	3	—	ns	
Chip select to output in low-Z	$t_{CLZ}$	3	—	3	—	ns	1
Output enable to output in low-Z	$t_{OLZ}$	0	—	0	—	ns	1
Byte select to output in low-Z	$t_{BLZ}$	0	—	0	—	ns	1
Chip deselect to output in high-Z	$t_{CHZ}$	—	5	—	6	ns	1
Output disable to output in high-Z	$t_{OHZ}$	—	5	—	6	ns	1
Byte deselect to output in high-Z	$t_{BHZ}$	—	5	—	6	ns	1

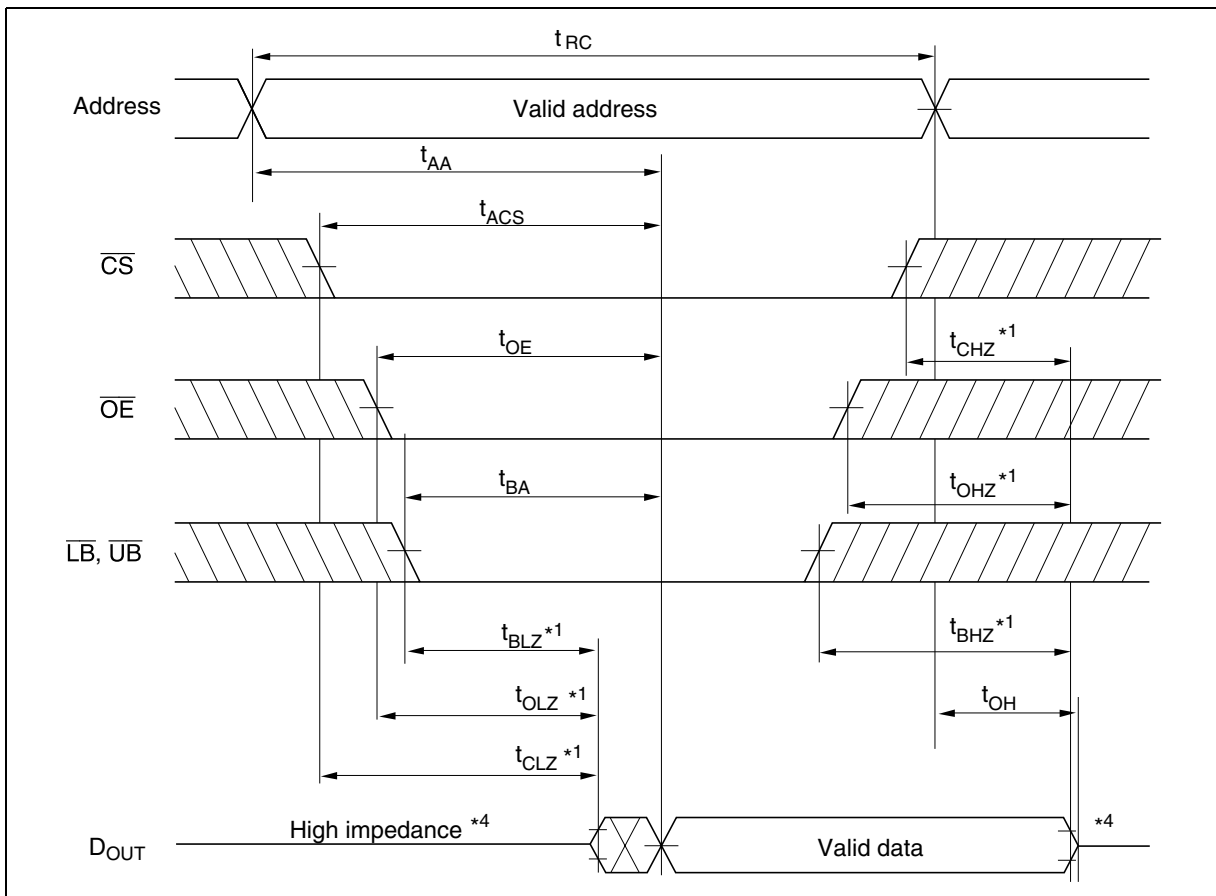
## Write Cycle

Parameter	Symbol	HM6216255HC				Unit	Notes
		-10		-12			
		Min	Max	Min	Max		
Write cycle time	$t_{WC}$	10	—	12	—	ns	
Address valid to end of write	$t_{AW}$	7	—	8	—	ns	
Chip select to end of write	$t_{CW}$	7	—	8	—	ns	8
Write pulse width	$t_{WP}$	7	—	8	—	ns	7
Byte select to end of write	$t_{BW}$	7	—	8	—	ns	
Address setup time	$t_{AS}$	0	—	0	—	ns	5
Write recovery time	$t_{WR}$	0	—	0	—	ns	6
Data to write time overlap	$t_{DW}$	5	—	6	—	ns	
Data hold from write time	$t_{DH}$	0	—	0	—	ns	
Write disable to output in low-Z	$t_{OW}$	3	—	3	—	ns	1
Output disable to output in high-Z	$t_{OHZ}$	—	5	—	6	ns	1
Write enable to output in high-Z	$t_{WHZ}$	—	5	—	6	ns	1

- Notes:
1. Transition is measured  $\pm 200$  mV from steady voltage with output load (B). This parameter is sampled and not 100% tested.
  2. If the  $\overline{CS}$  or  $\overline{LB}$  or  $\overline{UB}$  low transition occurs simultaneously with the  $\overline{WE}$  low transition or after the  $\overline{WE}$  transition, output remains a high impedance state.
  3.  $\overline{WE}$  and/or  $\overline{CS}$  must be high during address transition time.
  4. If  $\overline{CS}$ ,  $\overline{OE}$ ,  $\overline{LB}$  and  $\overline{UB}$  are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
  5.  $t_{AS}$  is measured from the latest address transition to the latest of  $\overline{CS}$ ,  $\overline{WE}$ ,  $\overline{LB}$  or  $\overline{UB}$  going low.
  6.  $t_{WR}$  is measured from the earliest of  $\overline{CS}$ ,  $\overline{WE}$ ,  $\overline{LB}$  or  $\overline{UB}$  going high to the first address transition.
  7. A write occurs during the overlap of a low  $\overline{CS}$ , a low  $\overline{WE}$  and a low  $\overline{LB}$  or a low  $\overline{UB}$  ( $t_{WP}$ ). A write begins at the latest transition among  $\overline{CS}$  going low,  $\overline{WE}$  going low and  $\overline{LB}$  going low or  $\overline{UB}$  going low. A write ends at the earliest transition among  $\overline{CS}$  going high,  $\overline{WE}$  going high and  $\overline{LB}$  going high or  $\overline{UB}$  going high.
  8.  $t_{CW}$  is measured from the later of  $\overline{CS}$  going low to the end of write.

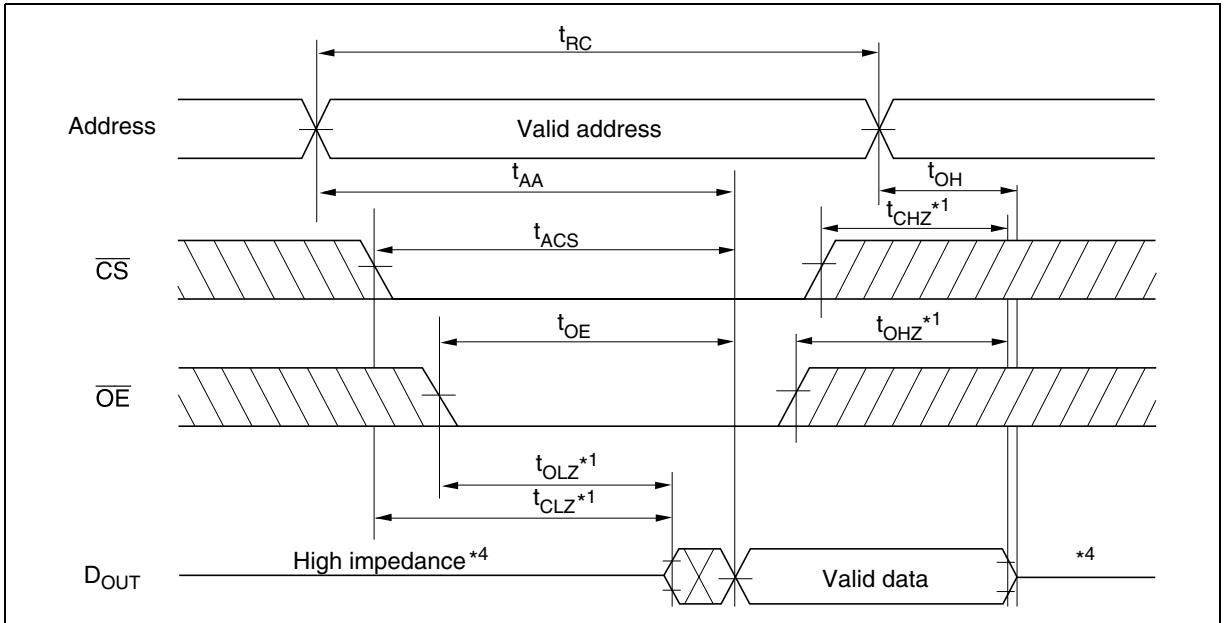
Timing Waveforms

Read Timing Waveform (1) ( $\overline{WE} = V_{IH}$ )

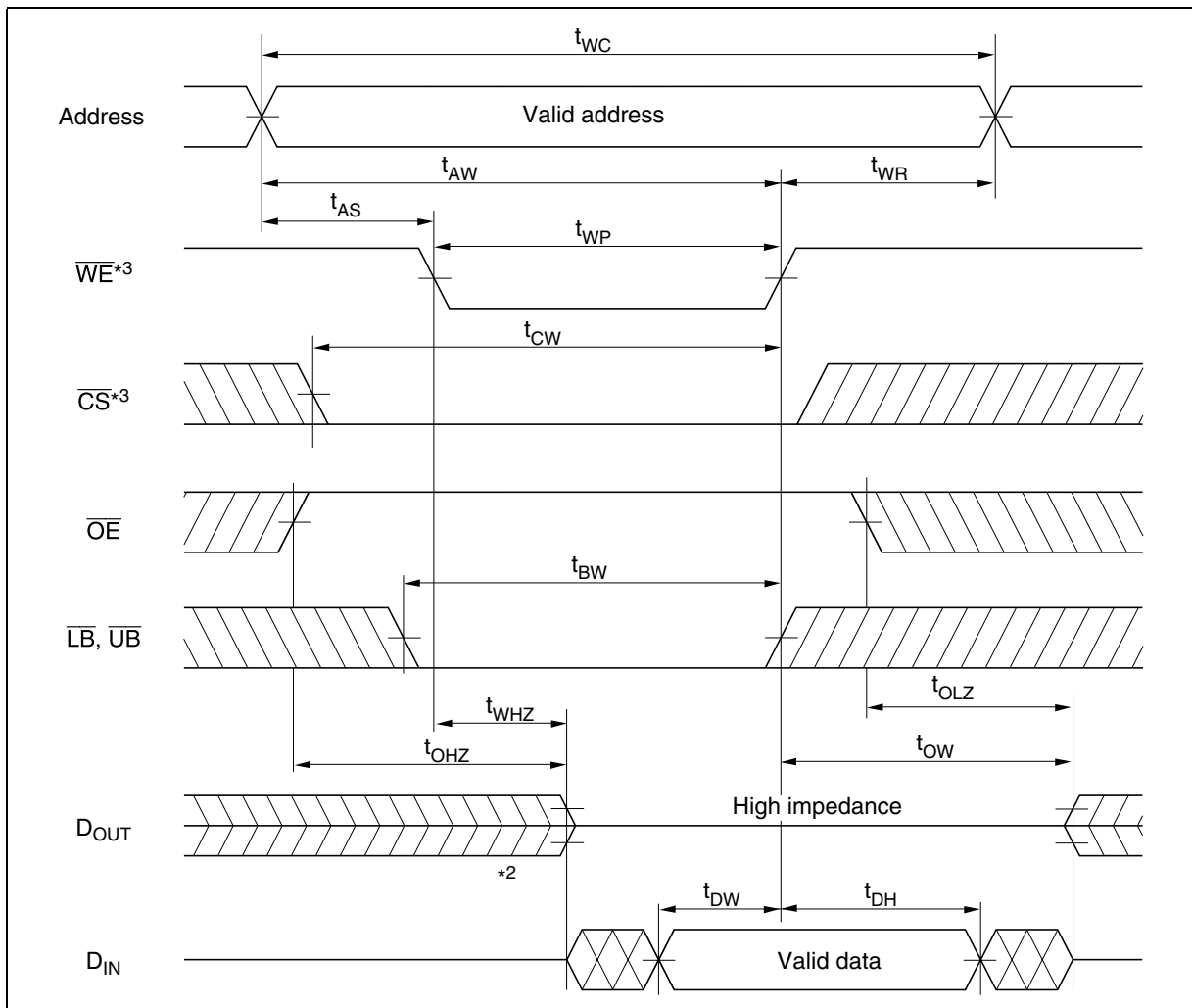


# HM6216255HC Series

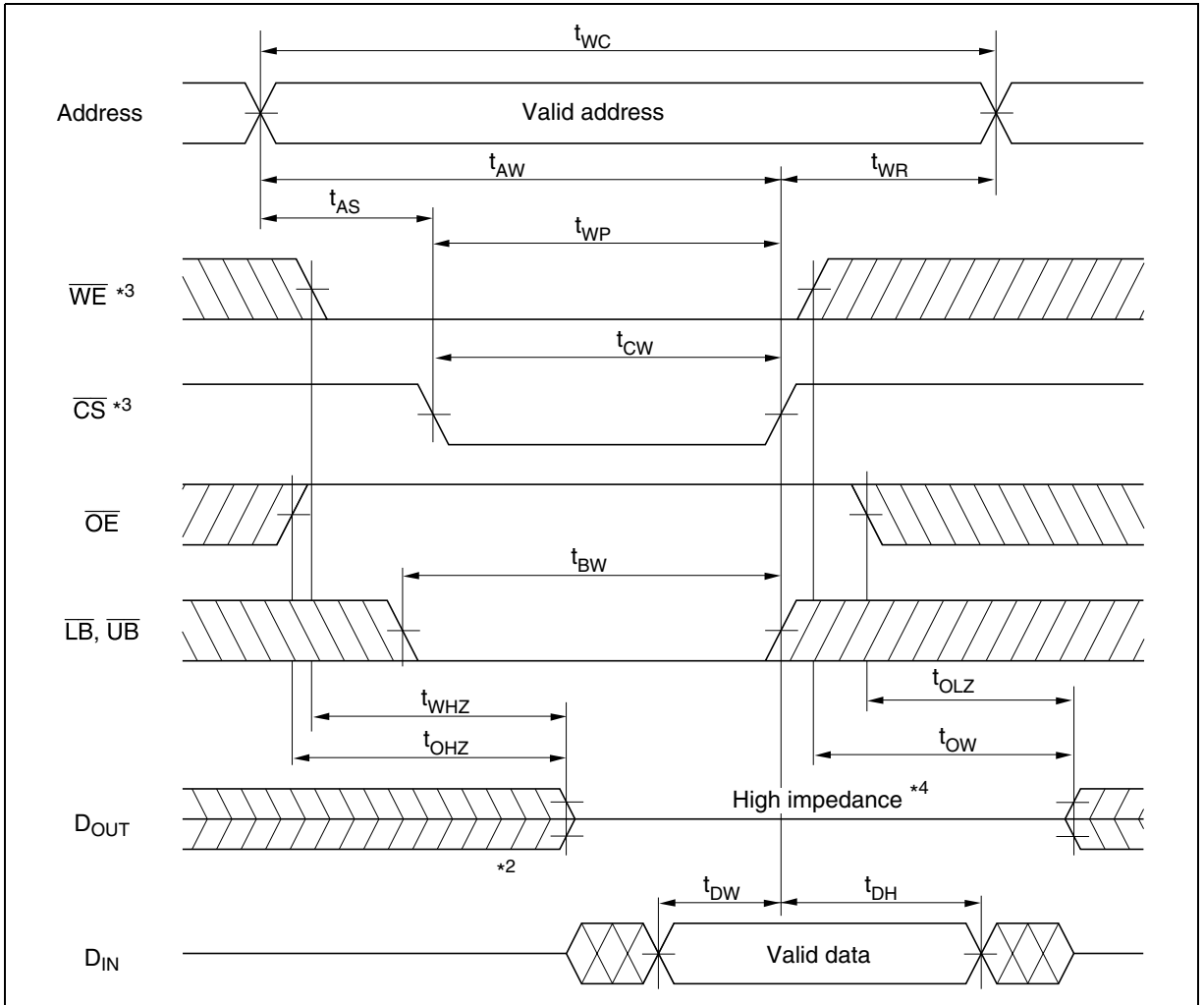
Read Timing Waveform (2) ( $\overline{WE} = V_{IH}$ ,  $\overline{LB} = V_{IL}$ ,  $\overline{UB} = V_{IL}$ )



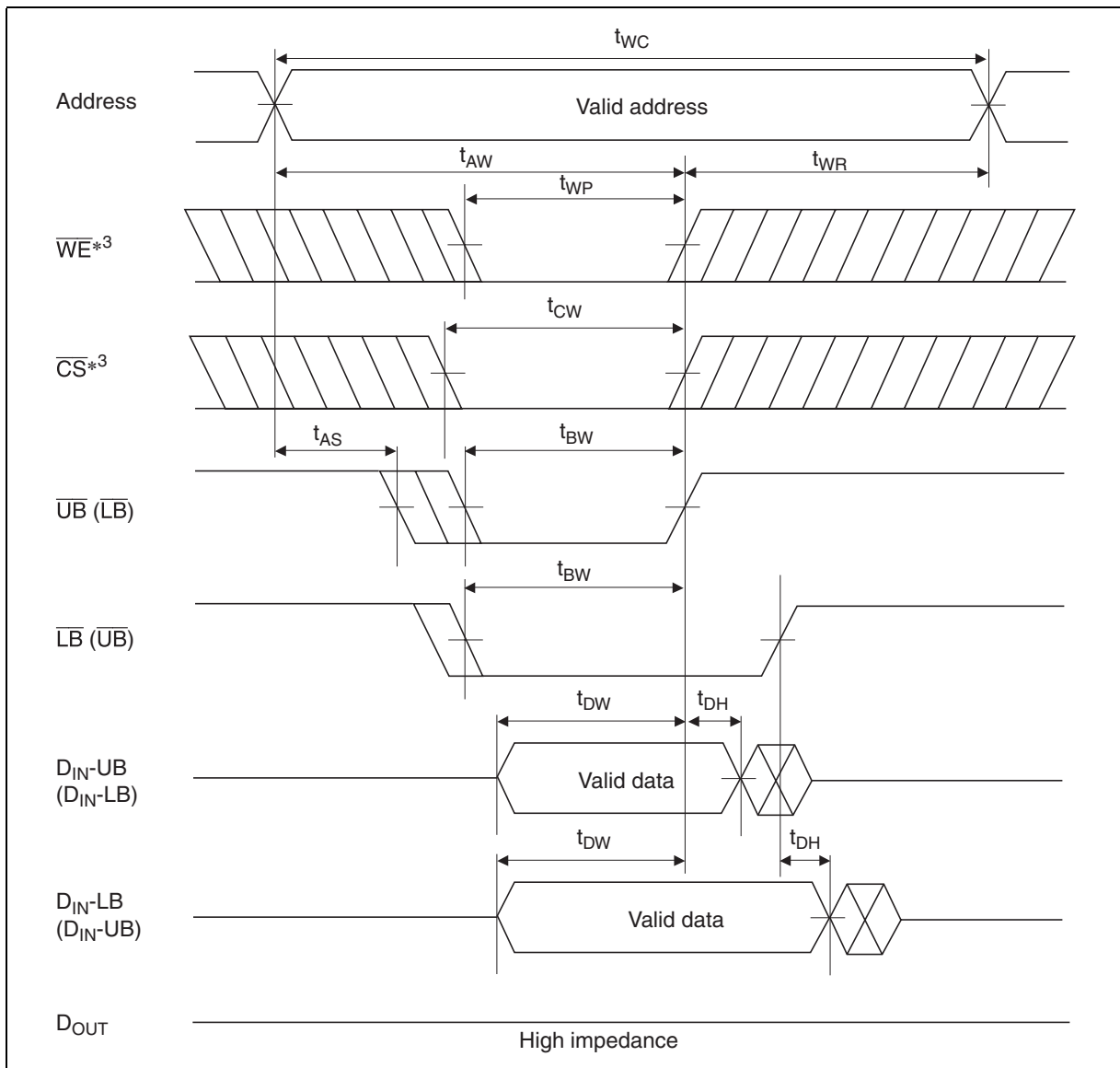
Write Timing Waveform (1) ( $\overline{WE}$  Controlled)



## Write Timing Waveform (2) ( $\overline{CS}$ Controlled)



Write Timing Waveform (3) ( $\overline{LB}$ ,  $\overline{UB}$  Controlled,  $\overline{OE} = V_{IH}$ )



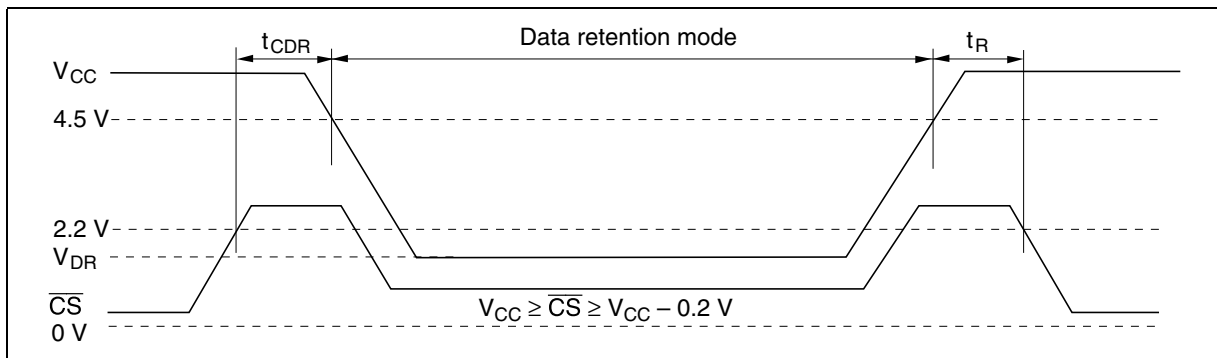
## Low $V_{CC}$ Data Retention Characteristics

( $T_a = 0$  to  $+70^\circ\text{C}$ )

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
$V_{CC}$ for data retention	$V_{DR}$	2.0	—	—	V	$V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2 \text{ V}$ , (1) $0 \text{ V} \leq V_{IN} \leq 0.2 \text{ V}$ or (2) $V_{CC} \geq V_{IN} \geq V_{CC} - 0.2 \text{ V}$
Data retention current	$I_{CCDR}$	—	—	800	$\mu\text{A}$	$V_{CC} = 3 \text{ V}$ $V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2 \text{ V}$ , (1) $0 \text{ V} \leq V_{IN} \leq 0.2 \text{ V}$ or (2) $V_{CC} \geq V_{IN} \geq V_{CC} - 0.2 \text{ V}$
Chip deselect to data retention time	$t_{CDR}$	0	—	—	ns	See retention waveform
Operation recovery time	$t_R$	5	—	—	ms	

## Low $V_{CC}$ Data Retention Timing Waveform



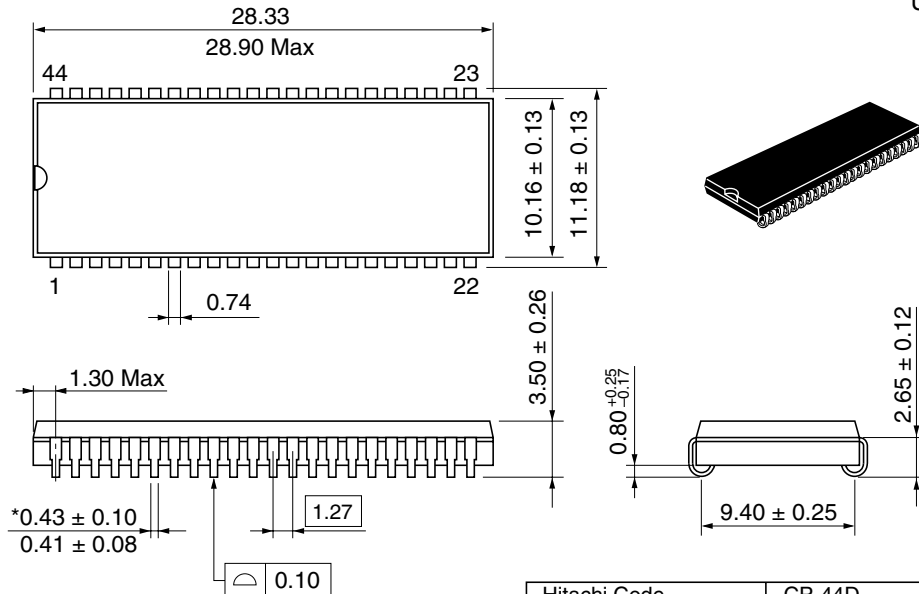


Package Dimensions

HM6216255HCJP/HCLJP Series (CP-44D)

As of July, 2002

Unit: mm



\*Dimension including the plating thickness  
Base material dimension

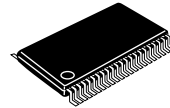
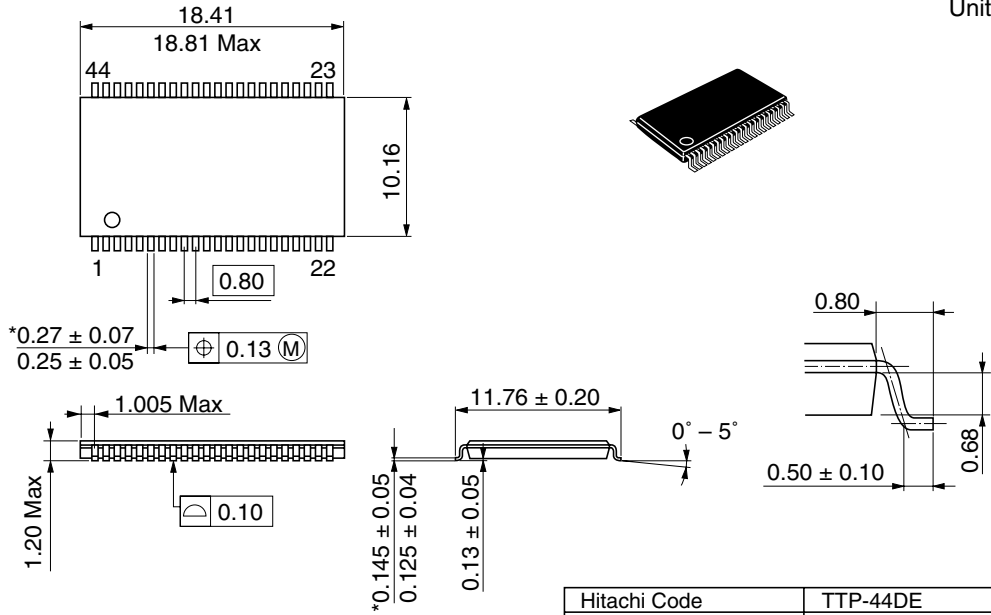
Hitachi Code	CP-44D
JEDEC	Conforms
JEITA	—
Mass (reference value)	1.8 g

# HM6216255HC Series

## HM6216255HCTT/HCLTT Series (TTP-44DE)

As of July, 2002

Unit: mm



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	TTP-44DE
JEDEC	—
JEITA	—
Mass (reference value)	0.43 g

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