T-77-05-05

LC7030

3025B

CMOS LSI

Electronic Tuning Controller

The LC7030 is a controller for direct PLL ICs LM7000, LM7000N and LM7001. It can be used to form a PLL frequency synthesizer for home stereo use.

Features

- Applicable in Japan, U.S. and Europe.
- FLT, LED-used dynamic display.
- Channel selection method (Sawtooth wave mode)

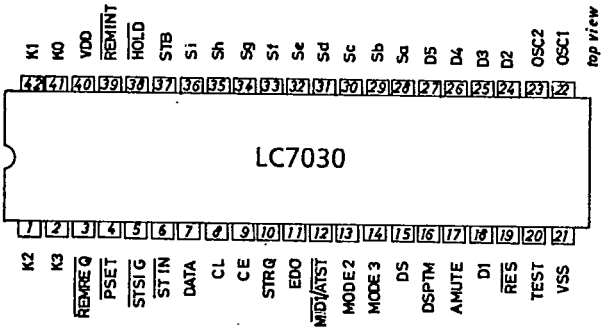
MANUAL (Up/down) : 1 channel/push. Pushing for 500msec. or more causes the channel display to go up/down at a 70msec./channel rate.
AUTO (Up/down) : Received channel hold.
PRESET : Possible to preset 8 channels each of FM/(MW+LW)

- Possible to preset also 3 kinds of information (MD1 to 3) (key entry, output pins available).
- Remote control accept capability : Preset channel up/down, band select.

Receiving Frequency

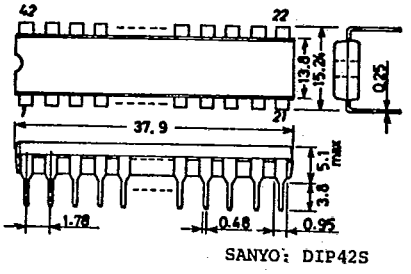
	Band	Receiving Frequency Range	Channel Space	Reference Frequency	Intermediate Frequency
Japan	FM	76.0 to 90.0 MHz	100 kHz	100 kHz	−10.7 MHz
	MW	522 to 1611 kHz	9 kHz	9 kHz	450 kHz
U.S.A.	FM	87.5 to 108.1 MHz	100/200 kHz	100 kHz	10.7 MHz
	MW1	520 to 1610 kHz	10 kHz	10 kHz	450 kHz
	MW2	522 to 1611 kHz	9 kHz	9 kHz	450 kHz
Europe	FM	87.5 to 108.0 MHz	50 kHz	50 kHz	10.7 MHz
	MW	522 to 1611 kHz	9 kHz	9 kHz	450 kHz
	LW	153 to 360 kHz	1 kHz	1 kHz	450 kHz

Pin Assignment



(Note) The pin assignment is subject to change without notice.

Case Outline 3025B-D42SIC
(unit : mm)



SANYO: DIP42S

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0V

				unit
Maximum Supply Voltage	V_{DD} max		−0.3 to +7.0	V
Maximum Input Voltage	V_{IN} max	Input pins other than OSC1	−0.3 to V_{DD}+0.3	V
Maximum Output Voltage	V_{OUT} max1	Pins 7 to 14,OSC2	−0.3 to V_{DD}+0.3	V
	V_{OUT} max2	Pins 15 to 18,24 to 37	V_{DD}−40 to V_{DD}+0.3	V
Peak Output Current	I_O1	Pins 7 to 14,OSC2,per pin	−2.0 to +2.0	mA
	I_O2	Pins 15 to 18,24 to 27,36,37,per pin	−15 to 0	mA
	I_O3	Pins 28 to 35,per pin	−3 to 0	mA
	I_O4	Pins 7 to 18,24 to 37,all pins	−90 to +16	mA
Allowable Power Dissipation	Pd max	Ta = −30 to +70°C	350	mW
Operating Temperature	Topg		−30 to +70	°C
Storage Temperature	Tstg		−55 to +125	°C

(Note) For the OSC1 pin, up to oscillation amplitude generated when internally oscillated under the recommended oscillation conditions in Fig.1 is allowable.

Allowable Operating Conditions at Ta = −30 to +70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V

			min	typ	max	unit
Supply Voltage	V_{DD}1		4.5	5.0	5.5	V
Supply Voltage (Power-down)	V_{DD}2	HOLD mode: $\overline{HOLD}$ = V_{IL}3	2.0		5.5	V
Input 'H'-Level Voltage	V_{IH}1	K0 to K3	0.38V_{DD}		V_{DD}	V
	V_{IH}2	Pins 3 to 14	0.7V_{DD}		V_{DD}	V
	V_{IH}3	$\overline{REMINT}$,$\overline{RES}$,$\overline{HOLD}$,OSC1	0.75V_{DD}		V_{DD}	V
Input 'L'-Level Voltage	V_{IL}1	Pins 3 to 14	V_{SS}		0.3V_{DD}	V
	V_{IL}2	$\overline{REMINT}$,$\overline{RES}$,OSC1	V_{SS}		0.25V_{DD}	V
	V_{IL}3	$\overline{HOLD}$: V_{DD} = 2.0 to 5.5V	V_{SS}		0.3V_{DD}−0.3	V
	V_{IL}4	TEST	V_{SS}		0.4	V
	V_{IL}5	K0 to K3	V_{SS}		0.4	V
Operating Clock Frequency	f_{extosc}	External clock is input to OSC1. OSC2 open. See Fig.2.	300		420	kHz
'H'-Level Clock Pulse	$t_{WØH}$	External clock is input to OSC1. OSC2 open. See Fig.2.	0.5			μs
'L'-Level Clock Pulse	$t_{WØL}$	Same as above	0.5			μs
Clock Input Rise Time	t_{oscR}	Same as above			0.2	μs
Clock Input Fall Time	t_{oscF}	Same as above			0.2	μs
External Capacitance for	C1	Resonator CSB400P,See Fig.1.		100±10%		pF
Ceramic Resonator OSC		Resonator KRB400B,See Fig.1.		100±10%		pF
	C2	Resonator CSB400P,See Fig.1.		100±10%		pF
		Resonator KRB400B,See Fig.1.		100±10%		pF
External Resistance for	R1			1000±5%		kΩ
Ceramic Resonator OSC	R2			4.7±5%		kΩ
Power-down $\overline{HOLD}$ Setup Time	t_{HOLDS}	See Fig.7.	2			ms
Power-down $\overline{HOLD}$ Hold Time	t_{HOLDH}	See Fig.7.	50			μs
Allowable Delay of	t_{DH}1	See Fig.4.			210	μs
Key Matrix Circuit	t_{DL}1	See Fig.4.			210	μs
Allowable Delay of	t_{DH}2	See Fig.5.			5	μs
Diode Matrix Circuit	t_{DL}2	See Fig.5.			5	μs

Electrical Characteristics at Ta = −30 to +70°C, V_{DD} = 5.0V ± 10%, V_{SS} = 0V

			min	typ	max	unit
Input 'H'-Level Current	I_{IH}	All input pins, V_{IN} = V_{DD}			1.0	μA
Input 'L'-Level Current	I_{IL}	All input pins, V_{IN} = V_{SS}	−1.0			μA

Continued on next page.

Continued from preceding page.

			min	typ	max	unit
Output 'H'-Level Voltage	$V_{OH}1$	Pins 7 to 14, $I_{OH}=-1mA$	$V_{DD}-2$			V
	$V_{OH}2$	Pins 7 to 14, $I_{OH}=-100\mu A$	$V_{DD}-0.5$			V
	$V_{OH}3$	Pins 15 to 18,24 to 27,36,37 $I_{OH}=-10mA$	$V_{DD}-2.0$			V
	$V_{OH}4$	Pins 15 to 18,24 to 27,36,37 $I_{OH}=-1mA$	$V_{DD}-0.6$			V
	$V_{OH}5$	Pins 28 to 35, $I_{OH}=-2mA$	$V_{DD}-1.0$			V
	$V_{OH}6$	Pins 28 to 35, $I_{OH}=-1mA$	$V_{DD}-0.6$			V
Output 'L'-Level Voltage	V_{OL}	Pins 7 to 14, $I_{OL}=-1mA$			0.4	V
Output Off Leak Current	$I_{OFF}1$	Pins 7 to 14, $V_{OUT}=V_{DD}$			1.0	μA
	$I_{OFF}2$	Pins 7 to 14, $V_{OUT}=V_{SS}$	−1.0			μA
	$I_{OFF}3$	Pins 15 to 18,24 to 37, $V_{OUT}=V_{DD}$			30	μA
	$I_{OFF}4$	Pins 15 to 18,24 to 37, $V_{OUT}=V_{DD}-35V$	−30			μA
Clock OSC Fequency for Ceramic Resonator OSC	f_{xosc}	Recommended conditions for ceramic resonator OSC in OSC circuit of Fig.1.	384	400	417	kHz
Current Dissipation	$I_{DD}1$	Ceramic resonator OSC, operation mode, recommended conditions for ceramic resonator OSC, output pin open, input pin, $V_{IN}=V_{DD}$		0.5	1.0	mA
	$I_{DD}2$	HOLD mode, test circuit in Fig.3, $V_{DD}=5V\pm10\%$		0.5	10	μA
	$I_{DD}3$	HOLD power-down mode, test circuit in Fig.3, $V_{DD}=2.0V$		0.1	2.0	μA
Input Capacitance	C_{IN}	Pins 1 to 6,41,42, f=1MHz		5		pF
		$\overline{RES}$,$\overline{HOLD}$,$\overline{REMINT}$,OSC1, f=1MHz		5		pF
Output Capacitance	C_{OUT}	OSC2, f=1MHz		10		pF
		Pins 15 to 18,24 to 27,36,37, f=1MHz, output off		20		pF
		Pins 28 to 35, f=1MHz, output off		10		pF
Input/Output Capacitance	C_{IO}	Pins 7 to 14, f=1MHz, output inhibit		10		pF

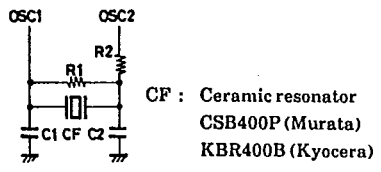


Fig.1 Recommended OSC Circuit for Ceramic Resonator OSC

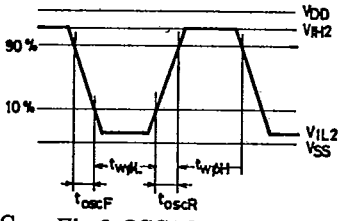


Fig.2 OSC1 Input Waveform

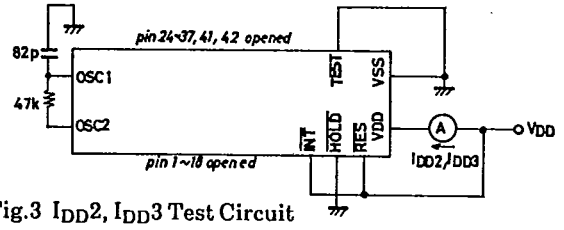
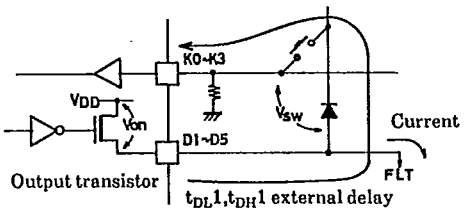


Fig.3 $I_{DD}2$, $I_{DD}3$ Test Circuit



Check to see that sum ($V_{ON}+V_{SW}$) of voltage drop (V_{ON}) in the output transistor and voltage drop (V_{SW}) in the switch circuit meets the V_{IH}/V_{IL} requirement of K0 to K3.

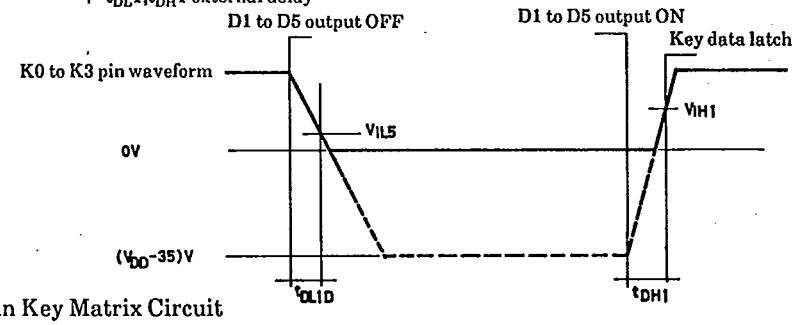
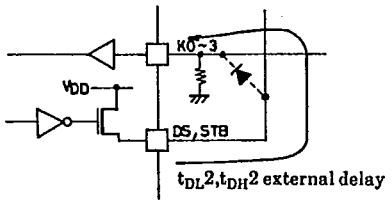


Fig.4 Delay in Key Matrix Circuit



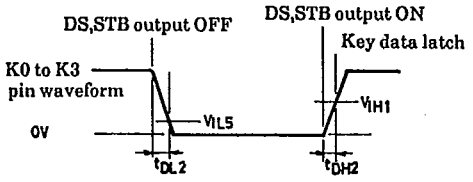
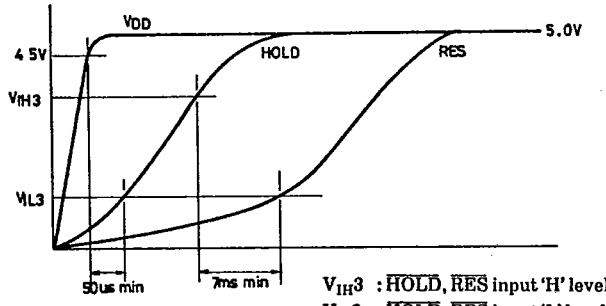


Fig.5 Delay in Diode Matrix Circuit



$V_{IH}3$: $\overline{HOLD}$, $\overline{RES}$ input 'H' level voltage
$V_{IL}3$: $\overline{HOLD}$, $\overline{RES}$ input 'L' level voltage

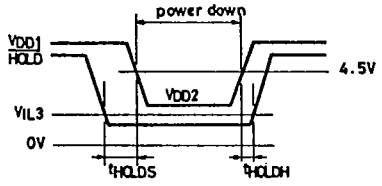


Fig.7 Power-down Mode Timing

Assuming the respective rise times are t_{VDD},$t_{\overline{HOLD}}$,$t_{\overline{RES}}$, the following requirement must be met.

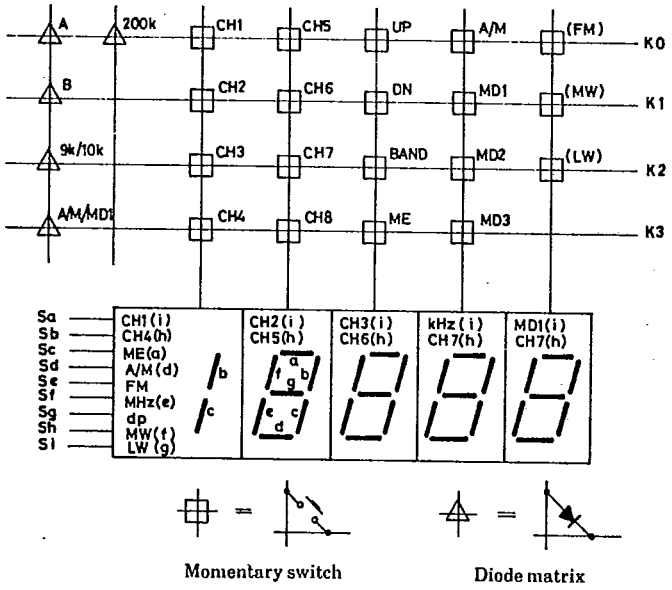
$$t_{VDD} < t_{\overline{HOLD}} < t_{\overline{RES}}$$
$$(CR1) \qquad (CR2)$$

For C,R1,R2 refer to the Sample Application Circuit.

Fig.6 Rise Time of V_{DD}, $\overline{HOLD}$,$\overline{RES}$ Pin Signal

T-77-05-05

Key Matrix Organization and Display



Diode Matrix (Read at power-ON mode : '0' = Without diode, '1' = With diode)

· Area select

		B	
		0	1
A	0	Japan	U.S.A.
	1	Europe (with LW)	Europe (without LW)

· 9/10k select

	9kHz	10kHz
9/10k	1	0

· A/M / MD1 select

	Function
0	The MD1 key is invalid. The output operates as $\overline{\text{AUTO ST}}$ and the A/M mode is stored in the preset memory. The A/M mode is also called at the band select mode, preset contents call mode.
1	The MD1 key is invalid and the MD1 mode is stored in the preset memory. The output operates as $\overline{\text{MD1}}$. The A/M mode is not stored in the preset memory. The MD1 key, A/M key operate independently.

· 100/200kHz step select (effective only when U.S.A. is selected.)

	100kHz	200kHz
100/200k	1	0

Key Description

T-77-05-05

CH1 to CH8

Key for writing/calling a channel, MD1 to 3 modes in/from the preset memory.

ME

Used to write a new channel, MD1 to 3 modes in the preset memory.
When this key is pushed, the 'ME' sign flashes and the write enable mode is entered, and when one of CH1 to CH8 is pushed within 5 seconds, a frequency being displayed and MD1 to 3 modes being set are written. The write enable mode is released automatically in 5 seconds.

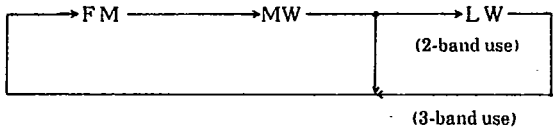
A/M

Key for selecting auto tuning mode/manual tunig mode. Each time this key is pushed, the mode is inverted in such a manner as AUTO→MAN.→AUTO · · · .
When A/M / MD1 = 0 (diode matrix) :
- The 'MD1' key is invalid.
- The A/M mode is stored in the preset memory.
  At the band select mode the A/M mode immediately before this band select is called. This holds true also at the preset contents call mode.
- When the A/M key is operated at the FM mode, the control signal is delivered at the $\overline{\text{MD1}}/\overline{\text{ATST}}$ pin. (The A/M key is operated to be coupled with the auto stereo/forced monaural mode.)
  At the AM mode the $\overline{\text{ATST}}$ ($\overline{\text{MD1}}$) pin is always at 'H' level.

When A/M / MD1 = 1 (diode matrix) :
- The 'A/M' key, 'MD1' key operate independently.
- At the band select mode, preset channel call mode the 'A/M' mode remains unaffected.
- The $\overline{\text{MD1}}$ output is a negative logic output at the FM mode and is fixed at 'H' level at the AM mode.

Band

Band select key. Each time this key is pushed, one band is selected.



FM,MW,LW

Band select key.

UP,DN

- At the manual mode :
  Each time this key is pushed, the channel display goes up/down.
  Pushing this key for 500msec. or more causes the channel display to go up/down at an approximately 70msec/channel rate.
- At the auto mode :
  A broadcasting station is searched automatically in the direction of the key pushed and a receiving frequency is held.
  If this key is kept pushed when the broadcasting station is reached, no auto stop occurs, but a temporary stop (approximately 500msec.) occurs.

MD1,MD2,MD3

· These keys are operated cyclically. The MD1,MD2,MD3 modes can be stored in the preset memory for each channel as shown below.

Diode matrix	A/M / MD1 = "0"					A/M / MD1 = "1"				
Key	Band	Operation	Pin name	Output	Description	Band	Operation	Pin name	Output	Description
A/M	FM	○	ATST	H/L	The A/M mode is stored and the output is turned ON/OFF.	FM	○	–	–	There is no output pin available for the A/M key. The tuning mode only is selected regardless of the band.
	MW LW	×		H	The A/M mode is stored but no output is delivered.	MW LW	○	–	–	
MD1	FM	×	–	–	The MD1 key is invalid.	FM	○	MD1	H/L	The MD1 key turns ON /OFF the output.
	MW LW	×	–	–		MW LW	×		H	The MD1 key is invalid.
MD2	FM	○	MODE2	H/L	The MD2 key turns ON /OFF the output. The MD2 mode is stored.	FM	○	MODE2	H/L	The MD2 key turns ON /OFF the output. The MD2 mode is stored.
	MW LW	×		L	The MD2 key is invalid.	MW LW	×		L	The MD2 key is invalid.
MD3	FM	○	MODE3	H/L	The MD2 key turns ON /OFF the output. The MD3 mode is stored.	FM	○	MODE3	H/L	The MD3 key turns ON /OFF the output. The MD3 mode is stored.
	MW LW	○		H/L	The MD2 key turns ON /OFF the output. The MD3 mode is stored.	MW LW	○		H/L	The MD3 key turns ON /OFF the output. The MD3 mode is stored.

Remote Control Accept Mode

The application of 'L' level to the $\overline{\text{REMINT}}$ pin when the $\overline{\text{REMREQ}}$ pin is at 'L' level causes the remote control accept mode to be entered. When 'H' level is applied to one of the following pins at the remote control accept mode, the operation corresponding to such pin is performed. (For the connection, refer to the Sample Application Circuit.)

K0 pin → CHUP (channel up)
K1 pin → CHDN (channel down)
K2 pin → BAND (band select)

CHUP

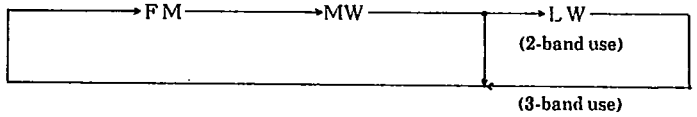
The preset channel number is incremented to call a channel desired.
When the preset channel is in the OFF state, CH1 is called.
When the $\overline{\text{REMREQ}}$ signal continues to be delivered, the preset channel number is incremented each time the $\overline{\text{REMINT}}$ pin is set to 'L' level.

CHDN

The preset channel number is decremented to call a channel desired.
When the preset channel is in the OFF state, CH8 is called.
When the $\overline{\text{REMREQ}}$ signal continues to be delivered, the preset channel number is decremented each time the $\overline{\text{REMINT}}$ pin is set to 'L' level.

BAND

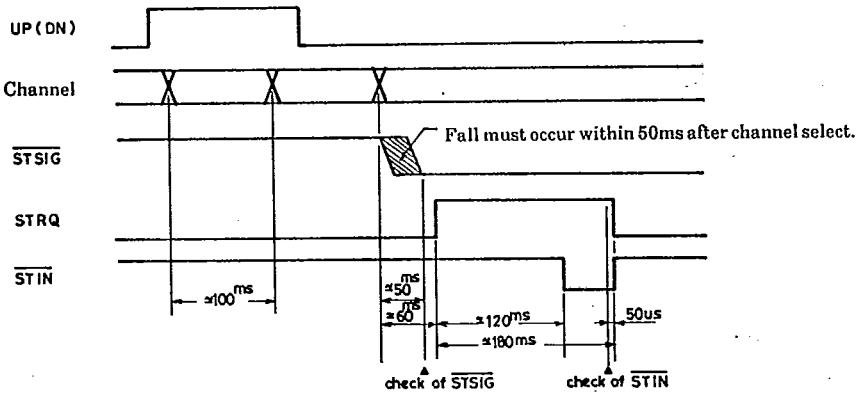
Even when the $\overline{\text{REMINT}}$ signal continues to be delivered, the following operation is not performed unless the $\overline{\text{REMREQ}}$ signal is released once.



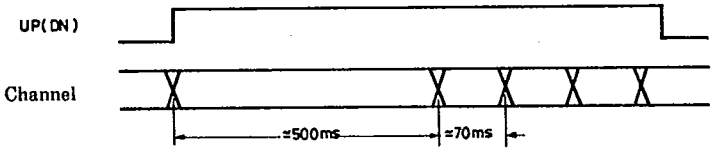
(Note) When the $\overline{\text{REMREQ}}$ signal, $\overline{\text{REMINT}}$ signal are not delivered, 'H' level must not be delivered at the K0 to K2 pins.

Timing Description

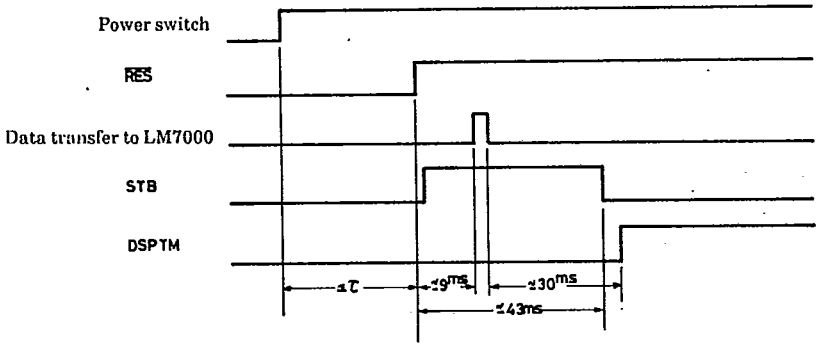
(1) Auto up/down



(2) Manual up/down



(3) Power switch ON

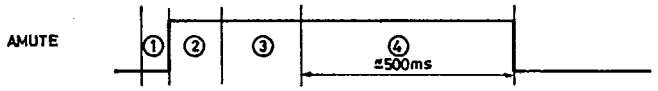


τ depends on C,R at the reset (RES) pin.

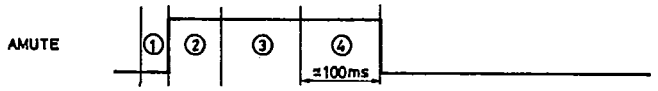
(4) Audio mute (AMUTE)

① Key chattering eliminating time (8msec)
② Audio pre-mute time (15 to 20msec)
③ Data transfer to PLL (15 to 100msec)
④ Audio post-mute time

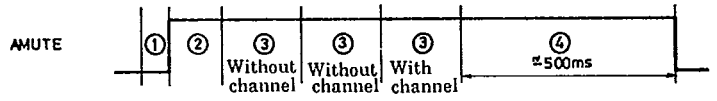
ⓐ Band select mode, preset contents read-out mode



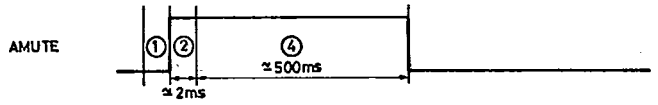
ⓑ Manual up/down mode (When the band edge is reached, the standby mode continues for approximately 500msec.)



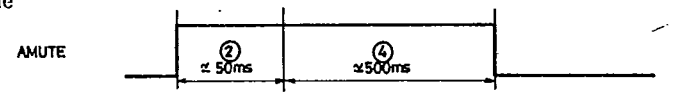
ⓒ Auto up/down mode (When the band edge is reached, the standby mode continues for approximately 500msec.)



ⓓ MD3 key ON/OFF mode

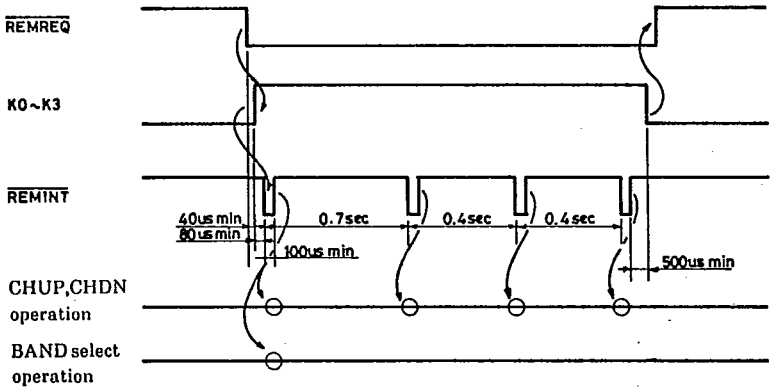


ⓔ Power ON mode

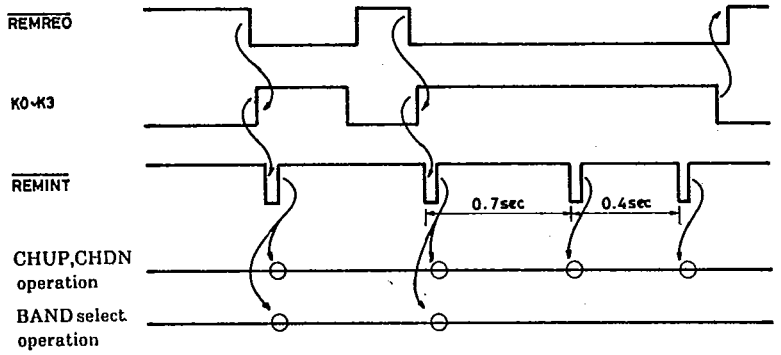


(5) Remote control accept timing

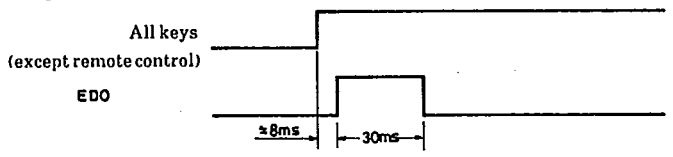
Single input



Consecutive 2 keys



(6) EDO output



Tracking Point

When a pulse of 'L' level is applied to the $\overline{\text{PSET}}$ pin for 100msec. or more, the following frequencies are loaded in the preset memory.

		CH1	CH2	CH3	CH4
Japan	FM	84.0MHz	–	–	–
	MW	630kHz	1080kHz	1440kHz	–
U.S.A	FM	98.1MHz	–	–	–
	MW1	630kHz	1080kHz	1440kHz	–
	MW2	630kHz	1080kHz	1440kHz	–
Europe	FM	98.1MHz	–	–	–
	MW LW	630kHz	1080kHz	1440kHz	245kHz

(Note) FM · · · $\overline{\text{ATST}}$,$\overline{\text{MD1}}$: ON ('L'), MODE2,MODE3 : OFF ('H')
MW,LW · · · MODE1 to 3 : Undefined

Power ON Processing ($\overline{\text{RES}}$ pin 'L' → 'H')

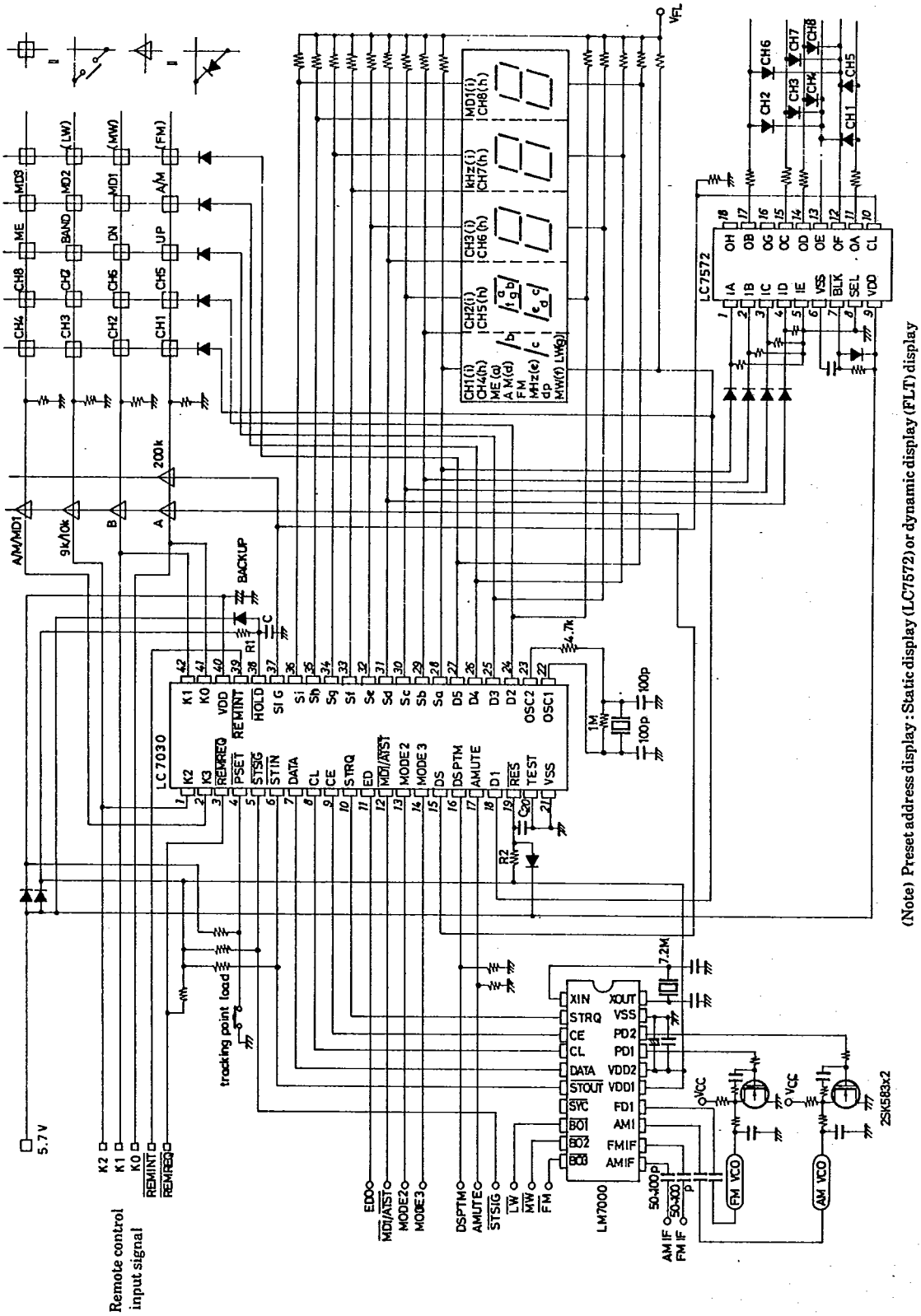
- The last channel data is transferred to the LM7000.
- The last channel number data is transferred to the LC7572.
- The DSPTM signal is delivered.
- The auto tuning mode is entered. (only when the A/M / MD1 diode matrix is '1'.)
- The audio mute signal is delivered.
- The diode matrix data is read.

Pin Description

Pin Name	Pin No.	Description	Active	I/O
Sa to Si	28 to 36	Display segment drive signal. Sa to Sd deliver BCD code for preset address display (using LC7572). Open drain output.	H	O
D1 to D5	18, 24 to 27	Display digit drive signal. Also used as key scan signal. Frame frequency is approximately 100Hz. Open drain output.	H	O
K0 to K3	1,2, 41,42	Key input, diode matrix input, remote control data input signal.	H	I
DS	15	Diode matrix scan signal. Open drain output.	H	O
STB	37	Diode matrix scan signal. Also used as 'CL' signal of the LC7572. Open drain output.	H	O
$\overline{\text{REMREQ}}$	3	Signal for indicating data transfer from remote control.	L	I
$\overline{\text{REMINT}}$	39	CHUP, CHDN timing pulse signal at remote control input mode.	L	I
$\overline{\text{PSET}}$	4	Signal for loading tracking point.	L	I
$\overline{\text{STSIG}}$	5	Signal for giving information that a broadcasting station is nearby during auto tuning.	L	I
$\overline{\text{STIN}}$	6	Auto tuning stop signal.	L	I
DATA	7	Data signal to be transferred to the LM7000 (CMOS output) CMOS output. DATA: Transfer data	–	O
CL	8	CL: Sync clock	∫	O
$\overline{\text{CE}}$	9	CE: Chip enable	H	O
STRQ	10	Signal for instructing the LM7000 to count IF.	H	O
ED0	11	When all keys are pushed, output is delivered. By connecting this pin to the function switch of an amplifier, the functions can be selected. CMOS output.	H	O
$\overline{\text{MD1/ATST}}$	12	Turned ON/OFF by the MD1, A/M key (only at the FM mode). Refer to the description of A/M key. CMOS output.	L	O
MODE2	13	Turned ON/OFF by the MD1 key (only at the FM mode) CMOS output.	H	O
MODE3	14	Turned ON/OFF by the MD2 key (all bands) CMOS output.	H	O
DSPTM	16	Signal for synchronizing an external display with the LC7030 display. Open drain output.	H	O
AMUTE	17	Audio mute signal: Open drain output · Band select mode · Auto, manual up/down mode · Preset contents read-out mode · MODE3 key ON mode · Power ON mode	H	O
$\overline{\text{RES}}$	19	Power On clear signal input.	L	I
TEST	20	Connected to V_{SS}.	–	–
$\overline{\text{HOLD}}$	38	Power-down mode control signal input.	L	I
OSC1	22	A ceramic resonator for system clock is connected.	–	I
OSC2	23		–	O
V_{DD}	40	Supplying of power (+5V).	–	–
V_{SS}	21	Supplying of power (0V).		

(Note) Open drain output : P channel.

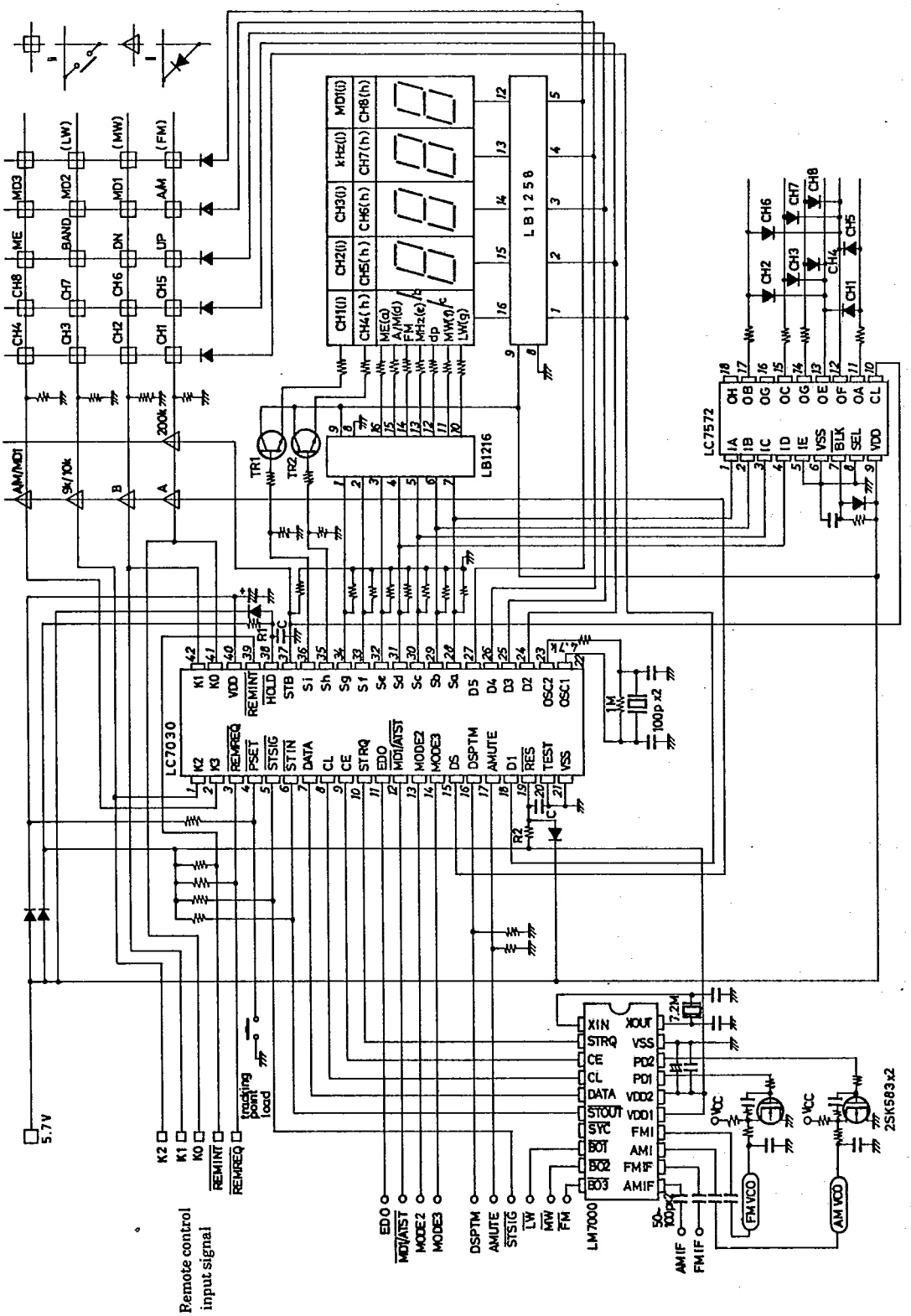
Sample Application Circuit 1 (FLT use)



(Note) Preset address display : Static display (LC7572) or dynamic display (FLT) display

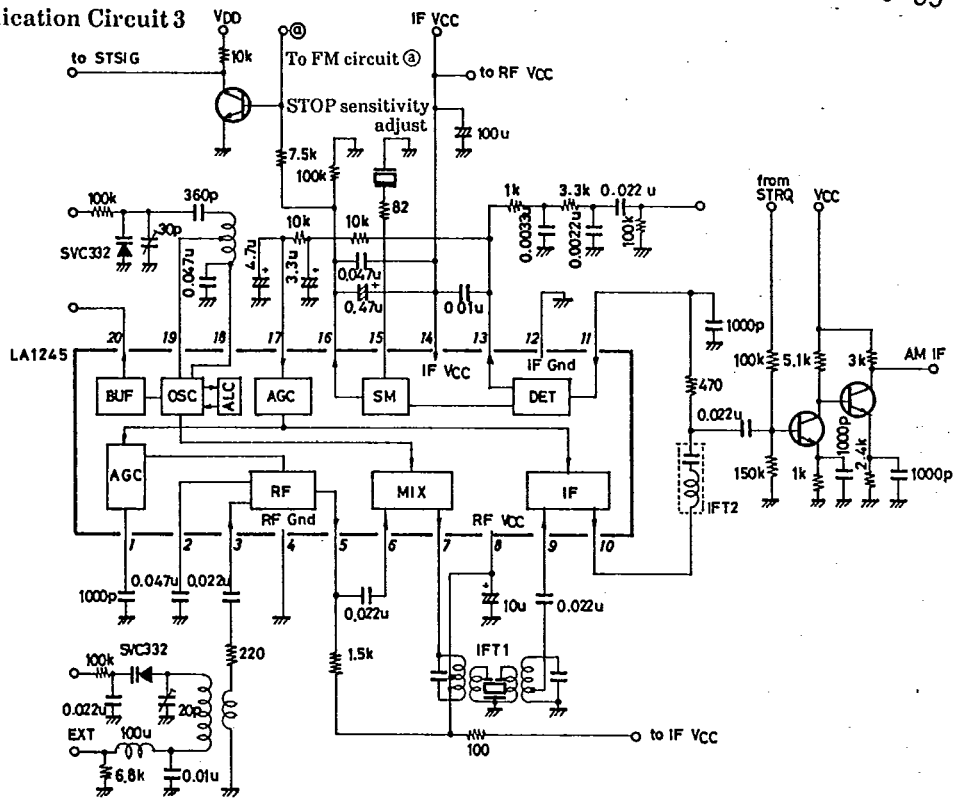
Sample Application Circuit 2 (LED use)

T-77-05-05

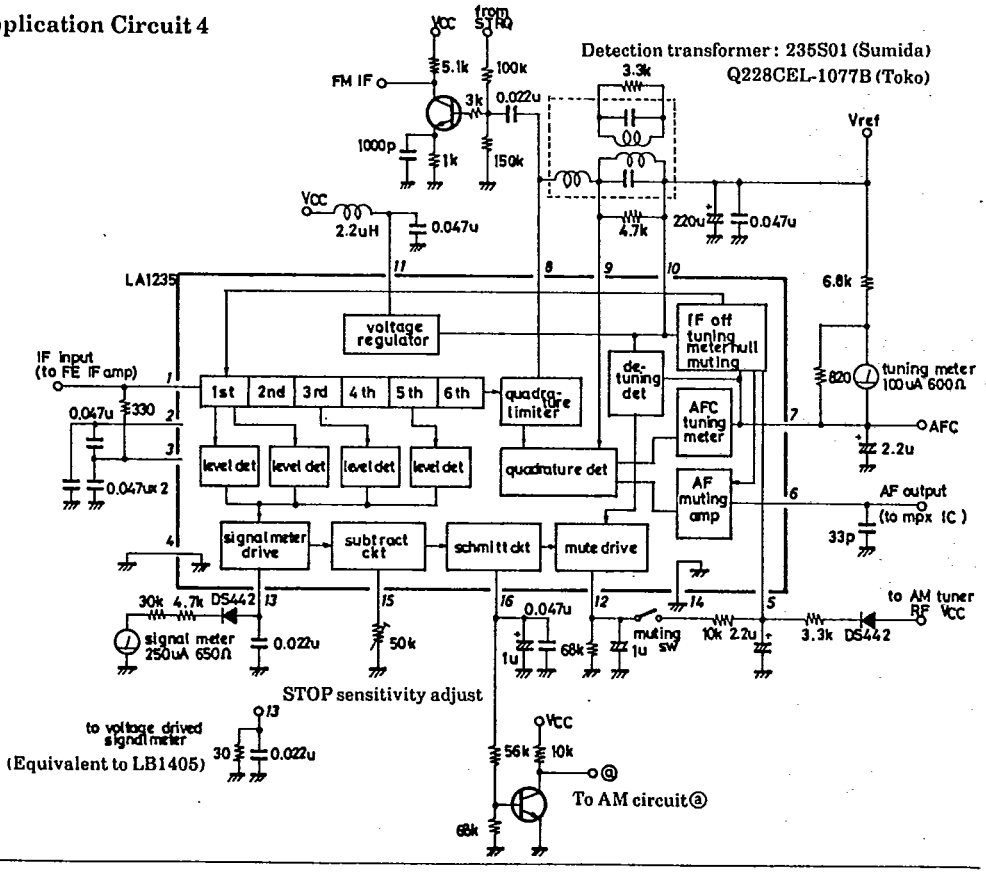


(Note) Preset address display : Static display (LC7572) or dynamic display (TR1, TR2) selectable.

Sample Application Circuit 3

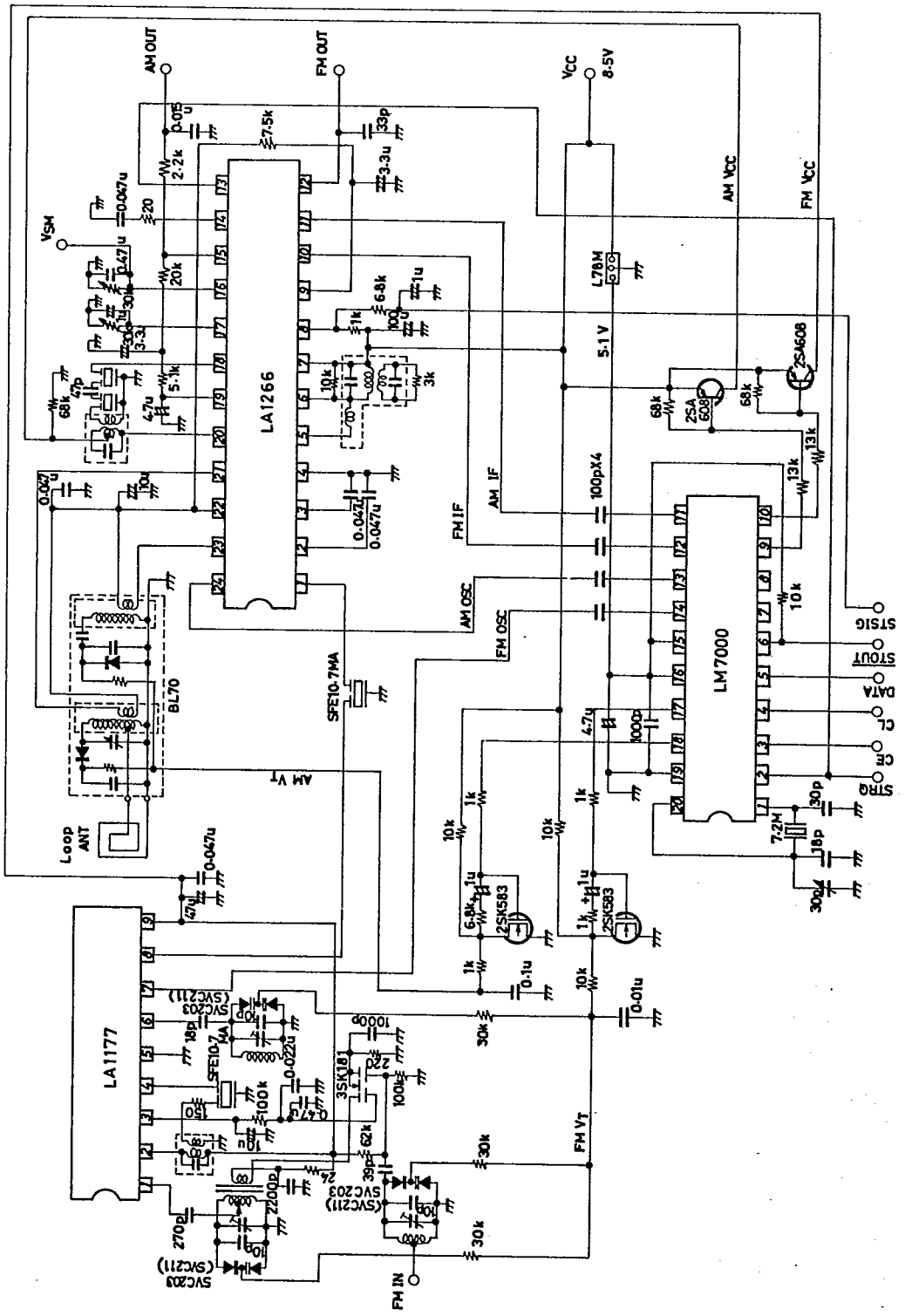


Sample Application Circuit 4



Sample Application Circuit 5

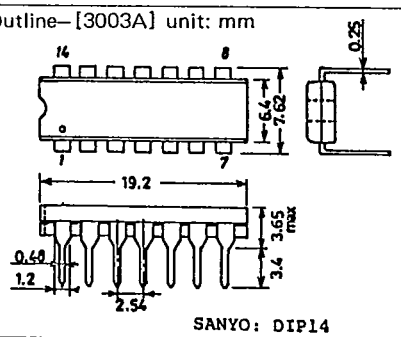
T-77-05-05



AUDIO-USE MOS IC CASE OUTLINES

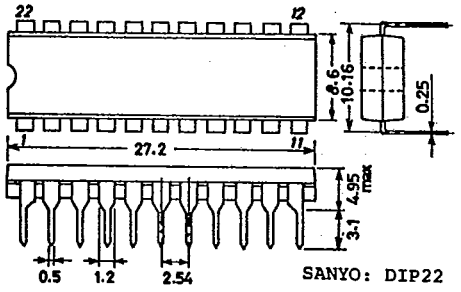
- All of Sanyo audio-use MOS IC case outlines are illustrated below.
- All dimensions are in mm, and dimensions which are not followed by min. or max. are represented by typical values.
- No marking is indicated.

Case Outline—[3003A] unit: mm



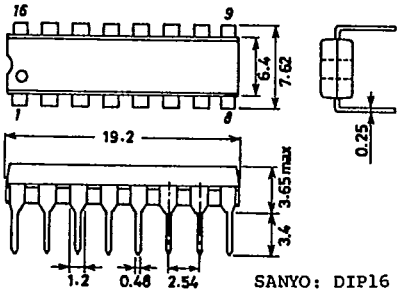
SANYO: DIP14

Case Outline—[3010A] unit: mm



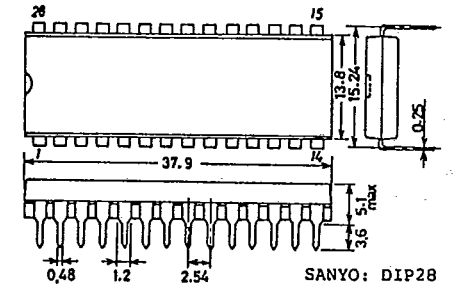
SANYO: DIP22

Case Outline—[3006B] unit: mm



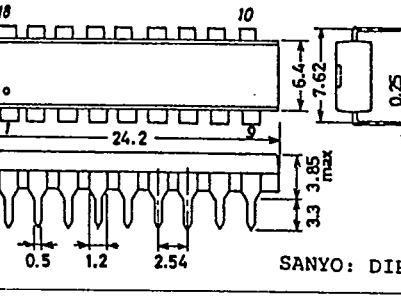
SANYO: DIP16

Case Outline—[3012A] unit: mm



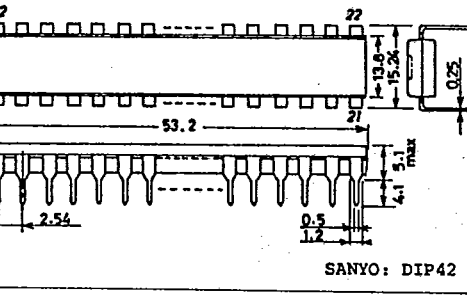
SANYO: DIP28

Case Outline—[3007A] unit: mm



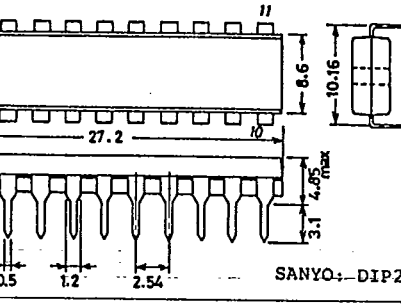
SANYO: DIP18

Case Outline—[3014A] unit: mm



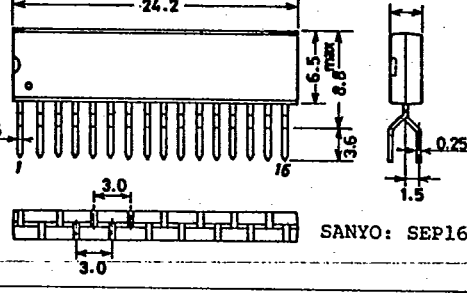
SANYO: DIP42

Case Outline—[3008A] unit: mm



SANYO: DIP20

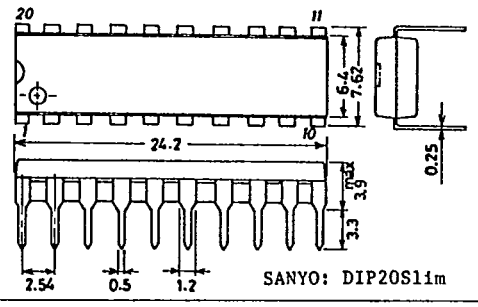
Case Outline—[3020A] unit: mm



SANYO: SEP16

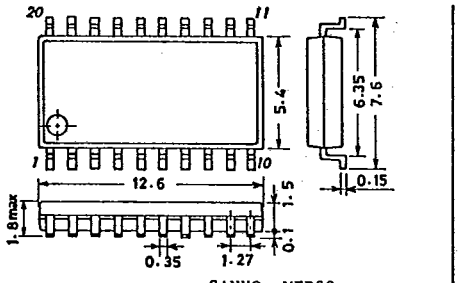
T-90-20

Case Outline—[3021B] unit: mm



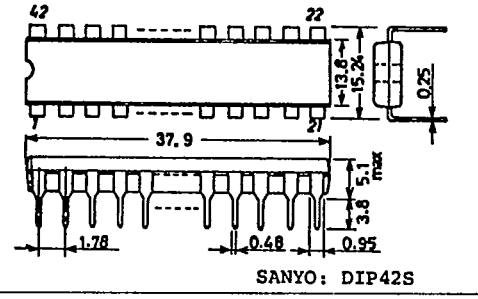
SANYO: DIP20S1im

Case Outline—[3036B] unit: mm



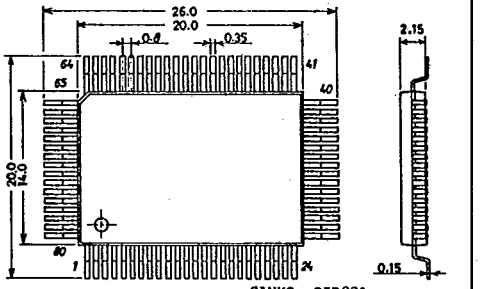
SANYO: MFP20

Case Outline—[3025B] unit: mm



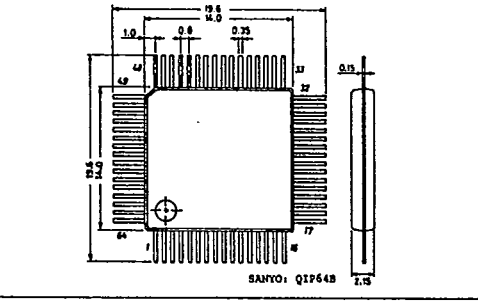
SANYO: DIP42S

Case Outline—[3044B] unit: mm



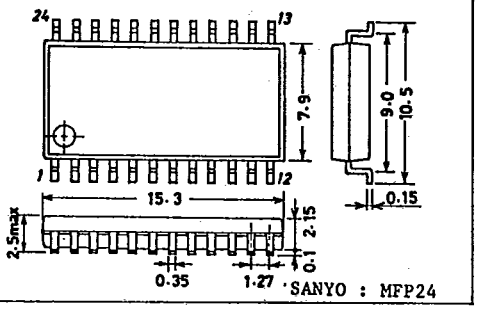
SANYO: QIP80A

Case Outline—[3026B] unit: mm



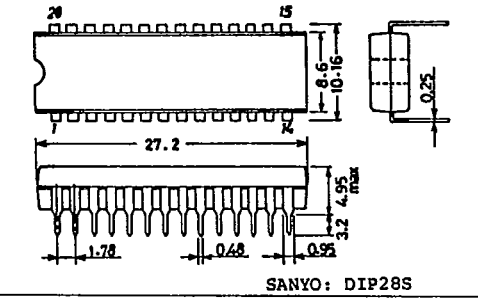
SANYO: QIP64B

Case Outline—[3045B] unit: mm



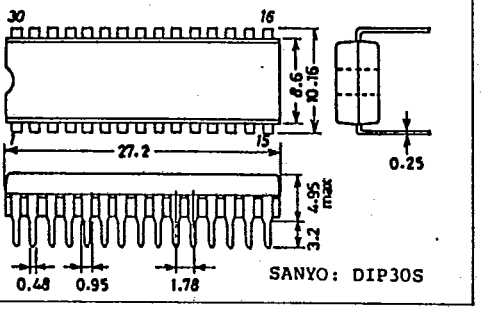
SANYO : MFP24

Case Outline—[3029A] unit: mm



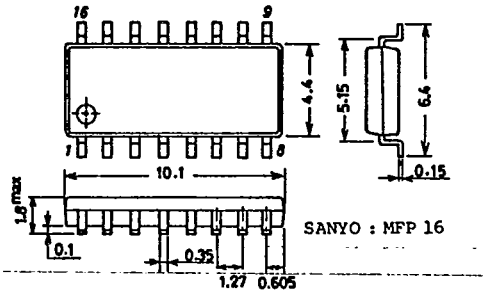
SANYO: DIP28S

Case Outline—[3047A] unit: mm



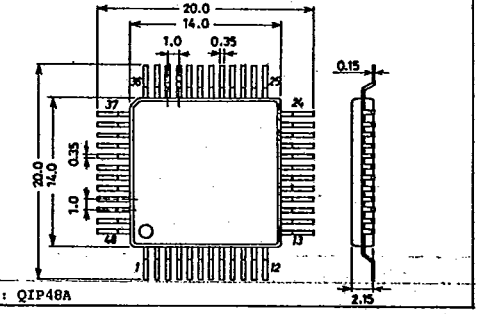
SANYO: DIP30S

Case Outline—[3035A] unit: mm



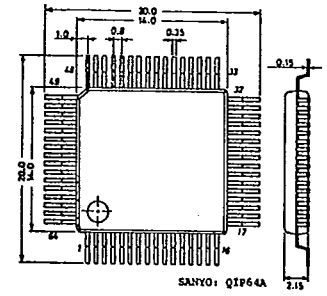
SANYO : MFP 16

Case Outline—[3052A] unit: mm

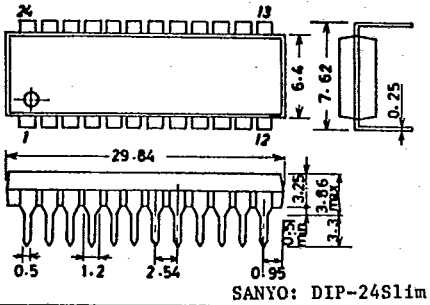


SANYO: QIP48A

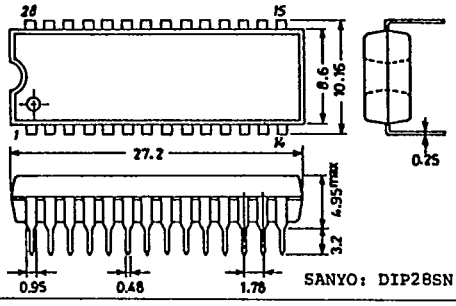
Case Outline—[3057] unit: mm



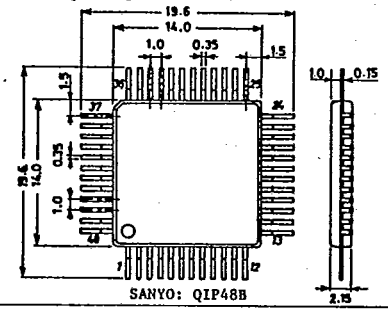
Case Outline—[3084] unit: mm



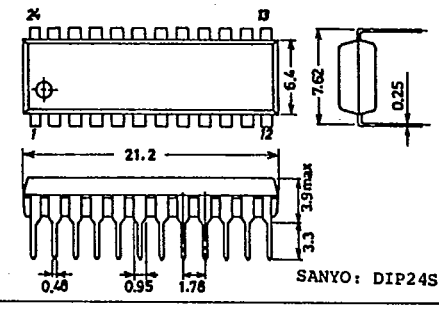
Case Outline—[3063] unit: mm



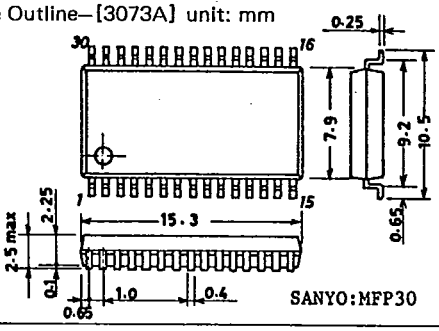
Case Outline—[3118] unit: mm



Case Outline—[3067] unit: mm



Case Outline—[3073A] unit: mm



Case Outline—[3074] unit: mm