

APC**DATA SHEET****System Logic Chip****DESCRIPTION**

The STP2024 System Logic Chip provides additional features for SBus based systems. It has two major logic blocks: an audio DMA controller and a glue logic block. The DMA controller consumes the bulk of the logic, providing 32-bit SBus DVMA and slave ports. It is designed to interface to a CODEC with an 8-bit interface, such as the CS4231 from Crystal Technologies, for system audio functions. The glue logic contains various useful system functions such as power management, SBus control and Boundary SCAN/JTAG capabilities.

The power management portion contains five read/write bits - each associated with output pins. The STP2024 effectively shuts down the system when not in use by putting the processor input a low power, standby mode. Once activity is detected, the system returns to normal operation. In addition, it can be used to control fan speed and power to the AC convenience outlet, CODEC and two general purpose ports.

Features

- Audio DMA Controller
- SBus Master device
- Power Management functions
- SBus Slot Select Decodes
- Dual SBus mastership for STP2000 (Master I/O Controller)
- Scan Chain Splice
- JTAG TAP

Benefits

- Independent Play and Capture pipeline channels, each with 21 bytes of buffering.
- Implementation meets SBus Specification B.0 at 25 MHz operation.
- Reduces overall system power consumption.
- Allows other SBus slaves to coexist in STP2024 address space.
- Return a sense of arbitration fairness to highly integrated I/O devices for a beneficial effect on I/O performance.
- Provides the ability to "splice" in an additional external scan chain into the STP2024's own scan chain.
- Test and diagnostic functionality via IEEE 1149.1 compliant internal and boundary scan controller.

BLOCK AND APPLICATION DIAGRAMS

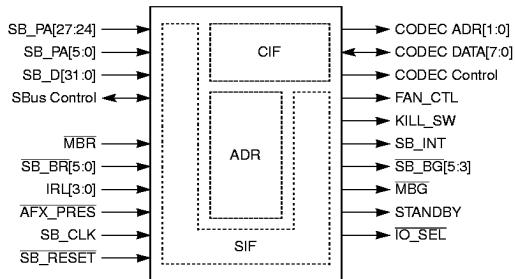


Figure 1. STP2024 Block Diagram

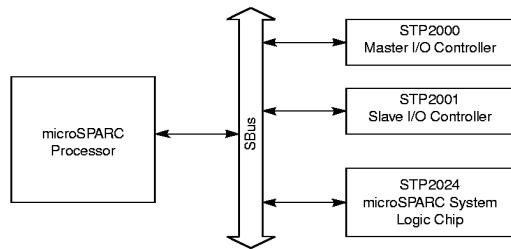


Figure 2. STP2024 Typical Application Diagram

SIGNAL DESCRIPTIONS

Signal	Type	Description
SB_CLK	Input	SBus clock. The main clock to the STP2024. All internal flip-flops are clocked by this one clock.
SB_RESET	Input	SBus reset. The main reset to the STP2024. All internal flip-flops are synchronously reset by this input. The COD_PDWN output is also forced low (active) by this input.
SB_DATA[31:0]	I/O	Bidirectional SBUS data pins. This 32-bit bus provides the PIO and DVMA access path in and out of the STP2024.
SB_PA[27:24, 5:2]	Input	SBus Address input pins. Bits 27-24, in conjunction with SB_AS and SB_SEL provide STP2024 slot decodes. Selecting either Audio, Power Management, microSPARC II local bus functional blocks, or IO_SEL generic select output. Bits 5-2 provide specific register selection.
SB_AS	Input	SBus address strobe input pin. Registered asserted state of this signal along with SB_SEL indicates the STP2024 is selected for PIO operation.
SB_SEL	Output	SBus slave select. When asserted indicates the STP2024 slot has been selected.
SB_READ	I/O	Bidirectional SBus read/write pin. This pin indicates whether the current transfer is a read or a write operation.
SB_SIZ[2:0]	I/O	Bidirectional SBus transfer size description pins. These three bits describe (encoded) the size of the data transfer, of the current SBUS operation.
SB_ACK[2:0]	I/O	Bidirectional SBus transfer acknowledgment pins. These three bits indicate an slave acknowledgment of the current SBUS cycle by returning an encoded status.
SB_BR [4]	Output	SBus Bus Request. The STP2024's Audio DMA engine asserts this output whenever the playback pipeline needs to be filled or whenever the capture pipeline needs to be emptied. Assertion of this bit will cause de-assertion of the STANDBY bit.
SB_BG [4]	Input	SBus Bus Grant. This input pin indicates that the pending bus request has been granted.
SB_INT	Output	SBus interrupt. An open drain output. Asserted when playback or capture DMA engines need attention. Also asserted on STP2024 detected errors.
SB_BR [5, 3]	Output	SBus Bus Request. The STP2000 Master I/O dual bus master logic asserts either one of these bus request outputs whenever the MBR input is asserted. Note that SB_BR [3] is the primary output.
SB_BG [5, 3]	Input	SBus Bus Grant. These input pins indicates that the pending bus request has been granted. The STP2000 Master I/O dual bus master logic muxes through the proper grant to the MBG output.
MBR	Input	Master I/O Bus Request. SBus Bus Request from the STP2000 Master I/O. The STP2000 dual bus master logic asserts either SB_BR[5] or SB_BR[3] outputs whenever this input pin is asserted. Assertion of this bit will cause de-assertion of the STANDBY bit.
MBG	Output	Master I/O Bus Grant. STP2000 Master I/O dual bus master logic selects either SB_BG [5] or SB_BG [3] and muxes it through to this output pin.
SB_BR [2:0]	Input	SBus Bus Request. Assertion of any of these inputs will cause de-assertion of the STANDBY bit.
CPU_IR[3:0]	Input	Encode CPU interrupt lines. Assertion of any of these inputs will cause de-assertion of the STANDBY bit.

SIGNAL DESCRIPTIONS (CONTINUED)

Signal	Type	Description
COD_DATA[7:0]	I/O	Codec Data bus. Byte wide, bidirectional data bus from/to the STP2024 from/to the Codec chip.
COD_PREQ	Input	Codec Play Request. This input indicates that the Codec is requesting data from the playback pipeline.
COD_CREQ	Input	Codec Capture Request. This input indicates that the Codec is requesting to send data to the capture pipeline.
COD_PACK	Output	Codec Playback Acknowledge. In response to a COD_PREQ this output indicates that play data will be written on the COD_DATA bus.
COD_CACK	Output	Codec Capture Acknowledge. In response to a COD_CREQ this output indicates that capture data will be sampled from the COD_DATA bus.
COD_PDWN	Output	Codec Power Down. This output places the Codec in reset/powerdown mode. Asserted by either CSR[5] or SB_RESET.
COD_CS	Output	Codec Chip Select. This output selects the Codec during PIO slave cycles.
COD_IOR	Output	Codec IO Read. This output indicates that the current operation to the Codec is a read.
COD_IOW	Output	Codec IO Write. This output indicates that the current operation to the Codec is a write.
COD_ADR[1:0]	Output	Codec Address. This output selects one of four 8-bit internal registers in the Codec during slave PIO cycles. These bits are directly driven from the SB_PA[3:2] input pins.
BPA	Output	Bit Port A. A generic output sourced from the PIO accessible BPA register.
BPB	Output	Bit Port B. A generic output sourced from the PIO accessible BPB register.
STANDBY	Output	Standby. A Power Management register output pin. Asserted by PIO write operations. De-asserted by any SB_BR or CPU_IR input.
KILL_COUTLET	Output	Kill Convenience Outlet. A Power Management register output pin. Asserted and de-asserted by PIO write operations
FAN_CTL	Output	Fan Control. A Power Management register output pin. Asserted and de-asserted by PIO write operations
TCK	Input	JTAG Clock. Test input clock for JTAG controller and scan registers.
TRSTN	Input	JTAG Reset pin.
TDI	Input	JTAG Data Input pin.
TDO	Output	JTAG Data Output pin.
TMS	Input	JTAG Mode Select input pin.
AFX_TDO	Input	An input pin from capable of receiving a JTAG scannable bit stream which can then be spliced into the STP2024's internal scan chain.
AFX_TDI	Output	An output pin which is either the STP2024's JTAG scan bit stream (if scan chain splice is active) or the generic bit port register, bpc.
AFX_PRESENT	Input	microSPARC-II local bus Present. An input pin which is PIO readable.
PNAND_OUT	Output	A series of serial connections of all STP2024 input and bidirectional pins, through NAND gates. Ends at this output pin. Used for test purposes only.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings^[1]

Symbol	Name	Rating	Units
V _{CC}	Power supply voltage	+7.0	V
V _{IN}	Input voltage (any pin)	GND ≤ V _{IN} ≤ V _{CC}	V
P _D	Power dissipation	500	mW
T _J	Operating junction temperature	0 to +105	°C
T _S	Storage temperature	-40 to +125	°C
	Static Discharge Voltage	2000	V

1. Operation of the device at values in excess of those listed above will result in degradation or destruction of the device. All voltages are defined with respect to ground. Functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Name	Min	Nom	Max	Units
V _{CC}	Supply Voltage	4.75	5.0	5.25	V
V _{IN}	DC input voltage	0	—	V _{CC}	V
P _D	Power dissipation	—	370	500	mW
T _A	Operating Free-Air Temperature	0	—	70	°C

Capacitance

Symbol	Description	PQCL Max	Units
C _{IN}	Input Capacitance	3	pF
C _{OUT}	Output Capacitance	2.7	pF
C _{BI}	Bidirectional Capacitance	3	pF

DC Characteristics ($V_{CC} = 5.0V \pm 5\%$)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Minimum High Level Input Voltage		2.0	—	—	V
V_{IL}	Maximum Low Level Input Voltage		—	—	0.8	V
V_{OH}	Minimum High Level Output Voltage	$I_{OH} = -4.0$ mA, $V_{CC} = \text{min}$, $I_{OH} = -6.0$ mA, $V_{CC} = \text{min}$, [1] $I_{OH} = -8.0$ mA, $V_{CC} = \text{min}$, [2]	2.4	4.5	—	V
V_{OL}	Minimum High Level Output Voltage	$I_{OL} = 4.0$ mA, $V_{CC} = \text{min}$, $I_{OL} = 6.0$ mA, $V_{CC} = \text{min}$, [1] $I_{OL} = 8.0$ mA, $V_{CC} = \text{min}$, [2]	—	0.2	0.4	V
I_{IN}	Minimum Input Current	$V_{IN} = V_{CC}$ or GND	-10	—	+10	μA
I_{OZ}	Maximum Output Leakage Current	$V_{OUT} = V_{CC}$ or GND Output Disabled	-10	—	+10	μA

1. SB_INT_1 output only.

2. SB_DATA[31:0], SB_SIZ[2:0], SB_ACK[2:0], SB_READ outputs only.

AC Characteristics: Input Pins

Signal	Parameter	Conditions	Reference Edge	Min	Max	Unit
SB_CLK	t_{CLK}			16	25	MHz
	t_{CH}			17	—	ns
	t_{CL}			17	—	ns
	t_{CR}			1	3	ns
	t_{CF}			1	3	ns
TCK	t_{CH}	JTAG_CLK $T_{CYC} \geq 100\text{ns}$		25	—	ns
	t_{CL}			25	—	ns
	t_{CR}			—	10	ns
	t_{CF}			—	10	ns
SB_RESET	t_{SI}		SB_CLK+ SB_CLK+	15	—	ns
	t_{HI}			—	1	ns
TRSTN	t_{SI}	2 cycles	TCK+ TCK+	10	—	ns
	t_{HI}			0	—	ns
TDI	t_{SI}		TCK+ TCK+	10	—	ns
	t_{HI}			0	—	ns
TMS	t_{SI}		TCK+ TCK+	10	—	ns
	t_{HI}			0	—	ns
AFX_TDO	t_{SI}		TCK+ TCK+	10	—	ns
	t_{HI}			0	—	ns
AFX_PRESENT		DC level		N/A	N/A	ns
SB_PA[27:24, 5:2]	t_{SI}		SB_CLK+ SB_CLK+	15	—	ns
	t_{HI}			—	1	ns
SB_AS	t_{SI}		SB_CLK+ SB_CLK+	15	—	ns
	t_{HI}			—	1	ns
SB_SEL	t_{SI}		SB_CLK+ SB_CLK+	15	—	ns
	t_{HI}			—	1	ns
SB_BR [2:0]	t_{SI}		SB_CLK+ SB_CLK+	15	—	ns
	t_{HI}			—	1	ns
SB_BG [5:3]	t_{SI}		SB_CLK+ SB_CLK+	15	—	ns
	t_{HI}			—	1	ns
CPU_IR[3:0]	t_{SI}		SB_CLK+ SB_CLK+	15	—	ns
	t_{HI}			—	1	ns
MBR	t_{SI}		SB_CLK+ SB_CLK+	15	—	ns
	t_{HI}			—	1	ns
COD_REQ	t_{SI}		SB_CLK+ SB_CLK+	N/A	N/A	ns
	t_{HI}			N/A	N/A	ns
COD_CREQ	t_{SI}		SB_CLK+ SB_CLK+	N/A	N/A	ns ns

AC Characteristics: Bidirectional Pins

Signal	Parameter	Conditions	Reference Edge	Min	Max	Unit
SB_DATA[31:0]	t_{DO}	70C, 4.75V, 100pf	SB_CLK+	—	22.5	ns
	t_{HO}	0C, 5.25V, 100pf	SB_CLK+	5.4	—	ns
	t_{SI}		SB_CLK+	15	—	ns
	t_{HI}		SB_CLK+	—	1	ns
SB_SIZ[2:0]	t_{DO}	70C, 4.75V, 100pf	SB_CLK+	—	20.9	ns
	t_{HO}	0C, 5.25V, 100pf	SB_CLK+	5.6	—	ns
	t_{SI}		SB_CLK+	15	—	ns
	t_{HI}		SB_CLK+	—	1	ns
SB_READ	t_{DO}	70C, 4.75V, 100pf	SB_CLK+	—	20.6	ns
	t_{HO}	0C, 5.25V, 100pf	SB_CLK+	4.7	—	ns
	t_{SI}		SB_CLK+	15	—1	ns
	t_{HI}		SB_CLK+	—	ns	ns
SB_ACK[2:0]	t_{DO}	70C, 4.75V, 100pf	SB_CLK+	—	20	ns
	t_{HO}	0C, 5.25V, 100pf	SB_CLK+	5.0	—	ns
	t_{SI}		SB_CLK+	15	—	ns
	t_{HI}		SB_CLK+	—	1	ns
COD_DATA[7:0]	t_{DO}	70C, 4.75V, 15pf	SB_CLK+	—	10.7	ns
	t_{HO}	0C, 5.25V, 15pf	SB_CLK+	—	—	ns
	t_{SI}		COD_IOW	22	—	ns
	t_{HI}		COD_IOW	—	0	ns

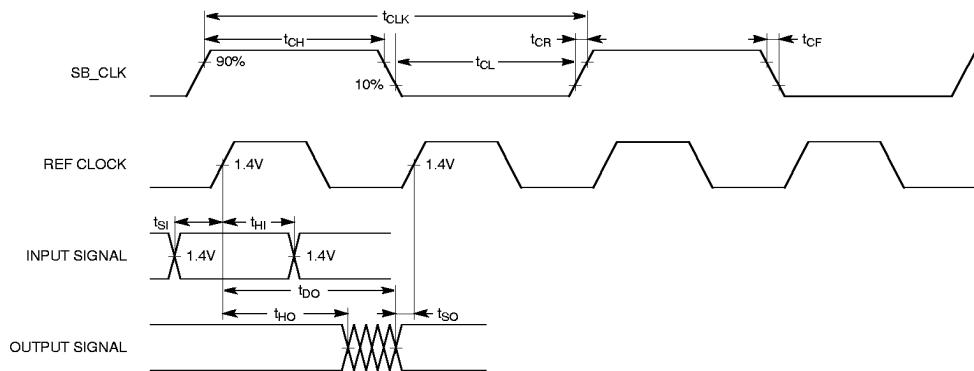
AC Characteristics: Output Pins

Signal	Parameter	Conditions	Reference Edge	Min	Max	Unit
SB_BR[4]	t_{DO}	70C, 4.75V, 60pf	SB_CLK+	—	21	ns
	t_{HO}	70C, 4.75V, 60pf	SB_CLK+	5.5	—	ns
SB_BR[5, 3]	t_{DO}	70C, 4.75V, 20pf	SB_CLK+	—	20.7	ns
	t_{HO}	70C, 4.75V, 20pf	SB_CLK+	2.5	—	ns
	t_{DO}	70C, 5.0V, 20pf	MBR	—	7.6	ns
MBG	t_{DO}	70C, 4.75V, 20pf	SB_CLK+	—	20	ns
	t_{HO}	70C, 4.75V, 20pf	SB_CLK+	3.4	—	ns
	t_{DO}	70C, 5.0V, 20pf	SB_BG [5,3]	—	7.6	ns
SB_INT	t_{DO}	70C, 4.75V, 100pf, L-H	SB_CLK+	—	12.3	ns
	t_{HO}	70C, 4.75V, 100pf, H-L	SB_CLK+	—	21.5	ns
BPA	t_{DO}	0C, 5.25V, 100pf, L-H	SB_CLK+	4.0	—	ns
	t_{HO}	0C, 5.25V, 100pf, H-L	SB_CLK+	6.3	—	ns
BPB	t_{DO}	70C, 4.75V, 15pf	SB_CLK+	—	13	ns
	t_{HO}	0C, 5.25V, 15pf	SB_CLK+	4.0	—	ns
STANDBY	t_{DO}	70C, 4.75V, 15pf	SB_CLK+	—	13	ns
	t_{HO}	0C, 5.25V, 15pf	SB_CLK+	4.2	—	ns
KILL_COUTLET	t_{DO}	70C, 4.75V, 30pf	SB_CLK+	—	13	ns
	t_{HO}	0C, 5.25V, 30pf	SB_CLK+	4.0	—	ns
FAN_CTL	t_{DO}	70C, 4.75V, 30pf	SB_CLK+	—	13	ns
	t_{HO}	0C, 5.25V, 30pf	SB_CLK+	4.2	—	ns
IO_SEL	t_{DO}	70C, 4.75V, 15pf	SB_PA[27:25]	—	9.9	ns
	t_{HO}	0C, 5.25V, 15pf	SB_PA[27:25]	3.7	—	ns
AFX_TDI	t_{DO}	70C, 4.75V, 15pf	SB_CLK+	—	13	ns
	t_{HO}	0C, 5.25V, 15pf	SB_CLK+	4.1	—	ns
TDO	t_{DO}	70C, 4.75V, 15pf	TCK+	—	—	ns
	t_{HO}	0C, 5.25V, 15pf	TCK+	8.3	—	ns
PNAND_OUT	t_{DO}	70C, 4.75V, 15pf	SB_READ+	—	200.6	ns
	t_{HO}	0C, 5.25V, 15pf	SB_READ+	—	—	ns
COD_CS	t_{DO}	70C, 4.75V, 15pf	SB_CLK+	—	12.5	ns
	t_{HO}	0C, 5.25V, 15pf	SB_CLK+	4.0	—	ns
COD_ADR[1:0]	t_{DO}	70C, 4.75V, 15pf	SB_PA[3:2]	—	8.4	ns
	t_{HO}	0C, 5.25V, 15pf	SB_PA[3:2]	2.3	—	ns
COD_IOW	t_{DO}	70C, 4.75V, 15pf	SB_CLK+	—	14.8	ns
	t_{HO}	0C, 5.25V, 15pf	SB_CLK+	4.4	—	ns
COD_IOR	t_{DO}	70C, 4.75V, 15pf	SB_CLK+	—	15.1	ns
	t_{HO}	0C, 5.25V, 15pf	SB_CLK+	4.4	—	ns

AC Characteristics: Output Pins (Continued)

Signal	Parameter	Conditions	Reference Edge	Min	Max	Unit
COD_PACK	t_{DO}	70C, 4.75V, 15pf	SB_CLK+	—	13.8	ns
	t_{HO}	0C, 5.25V, 15pf	SB_CLK+	4.0	—	ns
COD_CACK	t_{DO}	70C, 4.75V, 15pf	SB_CLK+	—	13.8	ns
	t_{HO}	0C, 5.25V, 15pf	SB_CLK+	4.0	—	ns
COD_PDWN	t_{DO}	70C, 4.75V, 15pf	SB_CLK+	—	12.7	ns
	t_{HO}	0C, 5.25V, 15pf	SB_CLK+	4.4	—	ns

TIMING DIAGRAMS



Parameter Definitions

- t_{SI} : Required setup time of a chip input referenced to a given (clock) edge.
- t_{HI} : Required hold time of a chip input referenced to a given (clock) edge.
- t_{HO} : Guaranteed hold time of an output referenced to a given (clock) edge.
- t_{SO} : Guaranteed setup time of an output referenced to a next given (clock) edge.
- t_{DO} : Guaranteed propagation time of an output referenced to a given (clock) edge.
- t_{CH} : Required clock high time.
- t_{CL} : Required clock low time.
- t_{CR} : Required clock rise time.
- t_{CF} : Required clock fall time.

Figure 3. Clock & I/O Waveforms

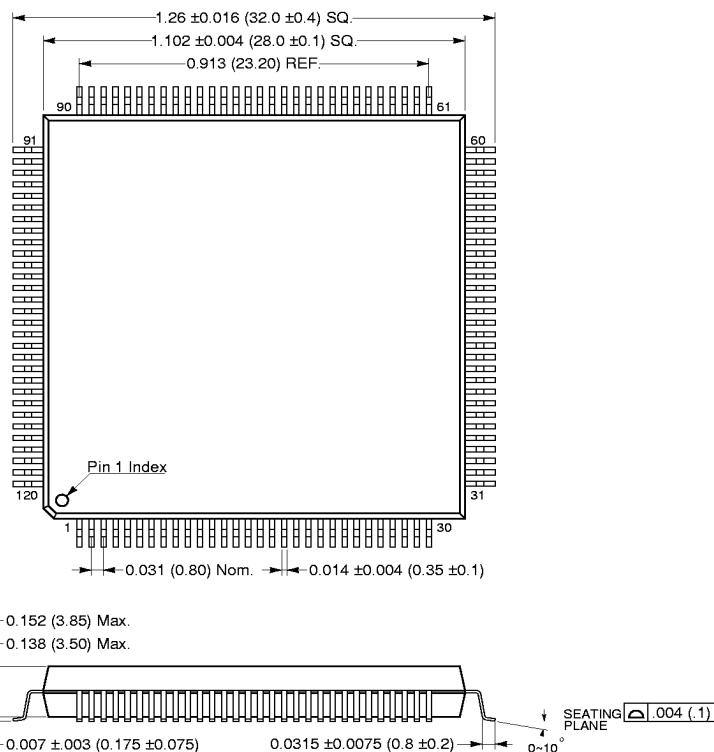
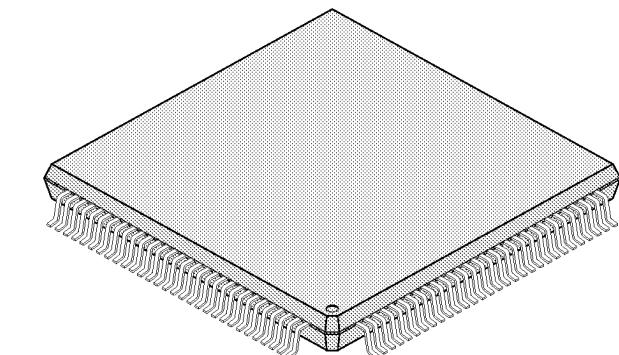
PACKAGING INFORMATION**120-Pin PQFP Pin Assignment**

Pin #	Pin Name						
1	SB_DATA[24]	31	GND	61	V _{CC}	91	SB_DATA[0]
2	SB_DATA[25]	32	SB_AS	62	COD_PDWN	92	SB_DATA[1]
3	SB_DATA[26]	33	SB_SEL	63	COD_PREQ	93	SB_DATA[2]
4	SB_DATA[27]	34	SB_BR[4]	64	COD_CREQ	94	SB_DATA[3]
5	SB_DATA[28]	35	SB_BG[3]	65	COD_IOW	95	SB_DATA[4]
6	SB_DATA[29]	36	SB_BG[5]	66	COD_IOR	96	SB_DATA[5]
7	V _{CC}	37	MBG	67	COD_PACK	97	SB_DATA[6]
8	GND	38	SB_BR[0]	68	COD_CACK	98	SB_DATA[7]
9	SB_DATA[30]	39	SB_BR[1]	69	COD_CS	99	SB_DATA[8]
10	SB_DATA[31]	40	SB_BR[2]	70	MBR	100	SB_DATA[9]
11	SB_ACK[2]	41	SB_BR[3]	71	IO_SEL	101	V _{CC}
12	SB_ACK[1]	42	SB_BR[5]	72	BPA	102	GND
13	SB_ACK[0]	43	SB_INT	73	STANDBY	103	GND
14	GND	44	COD_ADR[0]	74	FAN_CTL	104	SB_DATA[10]
15	SB_SIZ[2]	45	COD_ADR[1]	75	GND	105	SB_DATA[11]
16	SB_SIZ[1]	46	COD_DATA[0]	76	GND	106	SB_DATA[12]
17	SB_SIZ[0]	47	GND	77	V _{CC}	107	SB_DATA[13]
18	SB_PA[27]	48	GND	78	KILL_COUT	108	SB_DATA[14]
19	SB_PA[26]	49	V _{CC}	79	BPB	109	SB_DATA[15]
20	SB_PA[25]	50	COD_DATA[1]	80	TDI	110	SB_DATA[16]
21	SB_PA[24]	51	COD_DATA[2]	81	TCK	111	SB_DATA[17]
22	SB_PA[5]	52	COD_DATA[3]	82	TMS	112	SB_DATA[18]
23	SB_PA[4]	53	COD_DATA[4]	83	TDO	113	SB_DATA[19]
24	SB_PA[3]	54	COD_DATA[5]	84	AFX_TDO	114	V _{CC}
25	SB_PA[2]	55	COD_DATA[6]	85	AFX_TDI	115	GND
26	PNAND_OUT	56	COD_DATA[7]	86	AFX_PRES	116	SB_DATA[20]
27	TRSTN	57	CPU_IR3	87	SB_RESET	117	SB_DATA[21]
28	SB_READ	58	CPU_IR2	88	SB_CLK	118	SB_DATA[22]
29	BS_BG[4]	59	CPU_IR1	89	V _{CC}	119	SB_DATA[23]
30	V _{CC}	60	CPU_IR0	90	V _{CC}	120	V _{CC}

120-Pin PQFP Package Pinout

SB_DATA[24]	1	VCC	90	VCC	89	SB_CLK	88	SB_RESET	87	SB_RESET	86	AFX_PRES	85	AFX_TDI	84	AFX_TDO	83	TDO	82	TMS	81	TCX	80	TDI
SB_DATA[25]	2	GND	91	VCC	88	SB_CLK	87	SB_RESET	86	AFX_PRES	85	AFX_TDI	84	AFX_TDO	83	TDO	82	TMS	81	TCX	80	TDI	79	BPB
SB_DATA[26]	3	GND	92	VCC	89	SB_CLK	87	SB_RESET	86	AFX_PRES	85	AFX_TDI	84	AFX_TDO	83	TDO	82	TMS	81	TCX	80	TDI	78	KILL_COUT
SB_DATA[27]	4	GND	93	VCC	90	SB_CLK	88	SB_RESET	87	AFX_PRES	86	AFX_TDI	85	AFX_TDO	84	TDO	83	TMS	82	TCX	81	TDI	77	VCC
SB_DATA[28]	5	GND	94	VCC	91	SB_CLK	89	SB_RESET	88	AFX_PRES	87	AFX_TDI	86	AFX_TDO	85	TDO	84	TMS	83	TCX	82	TDI	76	GND
SB_DATA[29]	6	GND	95	VCC	92	SB_CLK	90	SB_RESET	89	AFX_PRES	88	AFX_TDI	87	AFX_TDO	86	TDO	85	TMS	84	TCX	83	TDI	75	GND
SB_DATA[30]	7	VCC	96	VCC	93	SB_CLK	91	SB_RESET	90	AFX_PRES	89	AFX_TDI	88	AFX_TDO	87	TDO	86	TMS	85	TCX	84	TDI	74	FAN_CTL
SB_DATA[31]	8	GND	97	VCC	94	SB_CLK	92	SB_RESET	91	AFX_PRES	90	AFX_TDI	89	AFX_TDO	88	TDO	87	TMS	86	TCX	85	TDI	73	STANDBY
SB_DATA[32]	9	VCC	98	VCC	95	SB_CLK	93	SB_RESET	92	AFX_PRES	91	AFX_TDI	90	AFX_TDO	89	TDO	88	TMS	87	TCX	86	TDI	72	BPA
SB_DATA[33]	10	GND	99	VCC	96	SB_CLK	94	SB_RESET	93	AFX_PRES	92	AFX_TDI	91	AFX_TDO	90	TDO	89	TMS	88	TCX	87	TDI	71	IO_SEL
SB_DATA[100]	101	VCC	100	VCC	101	SB_CLK	97	SB_RESET	96	AFX_PRES	95	AFX_TDI	94	AFX_TDO	93	TDO	92	TMS	91	TCX	90	TDI	60	CPU_IR[0]
SB_DATA[101]	102	GND	101	VCC	102	SB_CLK	98	SB_RESET	97	AFX_PRES	96	AFX_TDI	95	AFX_TDO	94	TDO	93	TMS	92	TCX	91	TDI	59	CPU_IR[1]
SB_DATA[102]	103	GND	102	VCC	103	SB_CLK	99	SB_RESET	98	AFX_PRES	97	AFX_TDI	96	AFX_TDO	95	TDO	94	TMS	93	TCX	92	TDI	58	CPU_IR[2]
SB_DATA[104]	104	VCC	101	VCC	104	SB_CLK	100	SB_RESET	99	AFX_PRES	98	AFX_TDI	97	AFX_TDO	96	TDO	95	TMS	94	TCX	93	TDI	57	CPU_IR[3]
SB_DATA[105]	105	GND	102	VCC	105	SB_CLK	101	SB_RESET	100	AFX_PRES	99	AFX_TDI	98	AFX_TDO	97	TDO	96	TMS	95	TCX	94	TDI	56	COD_DATA[7]
SB_DATA[106]	106	GND	103	VCC	106	SB_CLK	102	SB_RESET	101	AFX_PRES	100	AFX_TDI	99	AFX_TDO	98	TDO	97	TMS	96	TCX	95	TDI	55	COD_DATA[6]
SB_DATA[107]	107	VCC	104	VCC	107	SB_CLK	103	SB_RESET	102	AFX_PRES	101	AFX_TDI	100	AFX_TDO	99	TDO	98	TMS	97	TCX	96	TDI	54	COD_DATA[5]
SB_DATA[108]	108	GND	105	VCC	108	SB_CLK	104	SB_RESET	103	AFX_PRES	102	AFX_TDI	101	AFX_TDO	100	TDO	99	TMS	98	TCX	97	TDI	53	COD_DATA[4]
SB_DATA[109]	109	GND	106	VCC	109	SB_CLK	105	SB_RESET	104	AFX_PRES	103	AFX_TDI	102	AFX_TDO	101	TDO	100	TMS	99	TCX	98	TDI	52	COD_DATA[3]
SB_DATA[110]	110	VCC	107	VCC	110	SB_CLK	106	SB_RESET	105	AFX_PRES	104	AFX_TDI	103	AFX_TDO	102	TDO	101	TMS	100	TCX	99	TDI	51	COD_DATA[2]
SB_DATA[111]	111	GND	108	VCC	111	SB_CLK	107	SB_RESET	106	AFX_PRES	105	AFX_TDI	104	AFX_TDO	103	TDO	102	TMS	101	TCX	100	TDI	50	COD_DATA[1]
SB_DATA[112]	112	GND	109	VCC	112	SB_CLK	108	SB_RESET	107	AFX_PRES	106	AFX_TDI	105	AFX_TDO	104	TDO	103	TMS	102	TCX	101	TDI	49	VCC
SB_DATA[113]	113	VCC	114	GND	113	SB_CLK	109	SB_RESET	108	AFX_PRES	107	AFX_TDI	106	AFX_TDO	105	TDO	104	TMS	103	TCX	102	TDI	48	GND
SB_DATA[20]	114	GND	115	VCC	114	SB_CLK	110	SB_RESET	109	AFX_PRES	108	AFX_TDI	107	AFX_TDO	106	TDO	105	TMS	104	TCX	103	TDI	47	GND
SB_DATA[21]	115	GND	116	VCC	115	SB_CLK	111	SB_RESET	110	AFX_PRES	109	AFX_TDI	108	AFX_TDO	107	TDO	106	TMS	105	TCX	104	TDI	46	COD_ADR[2]
SB_DATA[22]	116	VCC	116	GND	117	SB_CLK	112	SB_RESET	111	AFX_PRES	110	AFX_TDI	109	AFX_TDO	108	TDO	107	TMS	106	TCX	105	TDI	45	COD_ADR[1]
SB_DATA[23]	117	VCC	117	GND	117	SB_CLK	113	SB_RESET	112	AFX_PRES	111	AFX_TDI	110	AFX_TDO	109	TDO	108	TMS	107	TCX	106	TDI	44	COD_ADR[0]
SB_DATA[24]	118	GND	118	VCC	118	SB_CLK	114	SB_RESET	113	AFX_PRES	112	AFX_TDI	111	AFX_TDO	110	TDO	109	TMS	108	TCX	107	TDI	43	SB_INT
SB_DATA[25]	119	GND	119	VCC	119	SB_CLK	115	SB_RESET	114	AFX_PRES	113	AFX_TDI	112	AFX_TDO	111	TDO	110	TMS	109	TCX	108	TDI	42	SB_BR[5]
SB_DATA[26]	120	VCC	114	GND	115	SB_CLK	116	SB_RESET	115	AFX_PRES	114	AFX_TDI	113	AFX_TDO	112	TDO	111	TMS	110	TCX	109	TDI	41	SB_BR[3]

120-Pin PQFP Package Dimensions



Dimensions in inches, dimensions in brackets in (millimeters).

ORDERING INFORMATION

Part Number	Description
STP1024PQFP	120-Pin Plastic Quad Flat Pack (PQFP)

Document Part Number: STP2024