SUN MICROELECTRONICS

STP2024

July 1997

APC

DATA SHEET — System Logic Chip

DESCRIPTION

The STP2024 System Logic Chip provides additional features for SBus based systems. It has two major logic blocks: an audio DMA controller and a glue logic block. The DMA controller consumes the bulk of the logic, providing 32-bit SBus DVMA and slave ports. It is designed to interface to a CODEC with an 8-bit interface, such as the CS4231 from Crystal Technologies, for system audio functions. The glue logic contains various useful system functions such as power management, SBus control and Boundary SCAN/JTAG capabilities.

The power management portion contains five read/write bits - each associated with output pins. The STP2024 effectively shuts down the system when not in use by putting the processor input a low power, standby mode. Once activity is detected, the system returns to normal operation. In addition, it can be used to control fan speed and power to the AC convenience outlet, CODEC and two general purpose ports.

Features

- Audio DMA Controller
- SBus Master device
- Power Management functions
- SBus Slot Select Decodes
- Dual SBus mastership for STP2000 (Master I/O Controller)
- Scan Chain Splice
- JTAG TAP

Benefits

- Independent Play and Capture pipeline channels, each with 21 bytes of buffering.
- Implementation meets SBus Specification B.0 at 25 MHz operation.
- Reduces overall system power consumption.
- Allows other SBus slaves to coexist in STP2024 address space.
- Return a sense of arbitration fairness to highly integrated I/O devices for a beneficial effect on I/O performance.
- Provides the ability to “splice” in an additional external scan chain into the STP2024’s own scan chain.
- Test and diagnostic functionality via IEEE 1149.1 compliant internal and boundary scan controller.

BLOCK AND APPLICATION DIAGRAMS

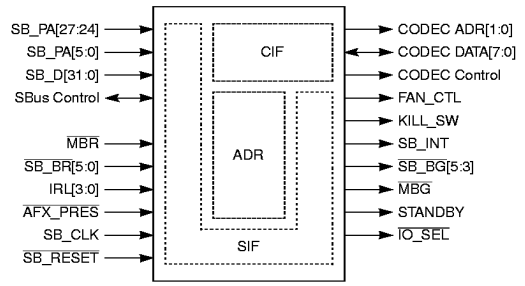


Figure 1. STP2024 Block Diagram

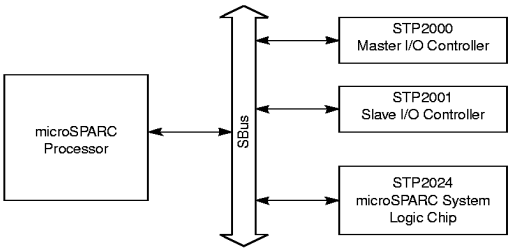


Figure 2. STP2024 Typical Application Diagram

SIGNAL DESCRIPTIONS

Signal	Type	Description
SB_CLK	Input	SBus clock. The main clock to the STP2024. All internal flip-flops are clocked by this one clock.
$\overline{\text{SB\_RESET}}$	Input	SBus reset. The main reset to the STP2024. All internal flip-flops are synchronously reset by this input. The $\overline{\text{COD\_PDWN}}$ output is also forced low (active) by this input.
SB_DATA[31:0]	I/O	Bidirectional SBus data pins. This 32-bit bus provides the PIO and DVMA access path in and out of the STP2024.
SB_PA[27:24, 5:2]	Input	SBus Address input pins. Bits 27-24, in conjunction with $\overline{\text{SB\_AS}}$ and $\overline{\text{SB\_SEL}}$ provide STP2024 slot decodes. Selecting either Audio, Power Management, microSPARC II local bus functional blocks, or $\overline{\text{IO\_SEL}}$ generic select output. Bits 5-2 provide specific register selection.
$\overline{\text{SB\_AS}}$	Input	SBus address strobe input pin. Registered asserted state of this signal along with $\overline{\text{SB\_SEL}}$ indicates the STP2024 is selected for PIO operation.
$\overline{\text{SB\_SEL}}$	Output	SBus slave select. When asserted indicates the STP2024 slot has been selected.
SB_READ	I/O	Bidirectional SBus read/write pin. This pin indicates whether the current transfer is a read or a write operation.
SB_SIZ[2:0]	I/O	Bidirectional SBus transfer size description pins. These three bits describe (encoded) the size of the data transfer, of the current SBus operation.
$\overline{\text{SB\_ACK}}$[2:0]	I/O	Bidirectional SBus transfer acknowledgment pins. These three bits indicate an slave acknowledgment of the current SBus cycle by returning an encoded status.
$\overline{\text{SB\_BR}}$ [4]	Output	SBus Bus Request. The STP2024's Audio DMA engine asserts this output whenever the playback pipeline needs to be filled or whenever the capture pipeline needs to be emptied. Assertion of this bit will cause de-assertion of the STANDBY bit.
$\overline{\text{SB\_BG}}$ [4]	Input	SBus Bus Grant. This input pin indicates that the pending bus request has been granted.
$\overline{\text{SB\_INT}}$	Output	SBus interrupt. An open drain output. Asserted when playback or capture DMA engines need attention. Also asserted on STP2024 detected errors.
$\overline{\text{SB\_BR}}$ [5, 3]	Output	SBus Bus Request. The STP2000 Master I/O dual bus master logic asserts either one of these bus request outputs whenever the $\overline{\text{MBR}}$ input is asserted. Note that $\overline{\text{SB\_BR}}$ [3] is the primary output.
$\overline{\text{SB\_BG}}$ [5, 3]	Input	SBus Bus Grant. These input pins indicates that the pending bus request has been granted. The STP2000 Master I/O dual bus master logic muxes through the proper grant to the $\overline{\text{MBG}}$ output.
$\overline{\text{MBR}}$	Input	Master I/O Bus Request. SBus Bus Request from the STP2000 Master I/O. The STP2000 dual bus master logic asserts either $\overline{\text{SB\_BR}}$[5] or $\overline{\text{SB\_BR}}$[3] outputs whenever this input pin is asserted. Assertion of this bit will cause de-assertion of the STANDBY bit.
$\overline{\text{MBG}}$	Output	Master I/O Bus Grant. STP2000 Master I/O dual bus master logic selects either $\overline{\text{SB\_BG}}$ [5] or $\overline{\text{SB\_BG}}$ [3] and muxes it through to this output pin.
$\overline{\text{SB\_BR}}$ [2:0]	Input	SBus Bus Request. Assertion of any of these inputs will cause de-assertion of the STANDBY bit.
CPU_IR[3:0]	Input	Encode CPU interrupt lines. Assertion of any of these inputs will cause de-assertion of the STANDBY bit.

SIGNAL DESCRIPTIONS (CONTINUED)

Signal	Type	Description
COD_DATA[7:0]	I/O	Codec Data bus. Byte wide, bidirectional data bus from/to the STP2024 from/to the Codec chip.
COD_PREQ	Input	Codec Play Request. This input indicates that the Codec is requesting data from the playback pipeline.
COD_CREQ	Input	Codec Capture Request. This input indicates that the Codec is requesting to send data to the capture pipeline.
$\overline{\text{COD\_PACK}}$	Output	Codec Playback Acknowledge. In response to a COD_PREQ this output indicates that play data will be written on the COD_DATA bus.
$\overline{\text{COD\_CACK}}$	Output	Codec Capture Acknowledge. In response to a COD_CREQ this output indicates that capture data will be sampled from the COD_DATA bus.
$\overline{\text{COD\_PDWN}}$	Output	Codec Power Down. This output places the Codec in reset/powerdown mode. Asserted by either CSR[5] or $\overline{\text{SB\_RESET}}$.
$\overline{\text{COD\_CS}}$	Output	Codec Chip Select. This output selects the Codec during PIO slave cycles.
$\overline{\text{COD\_IOR}}$	Output	Codec IO Read. This output indicates that the current operation to the Codec is a read.
$\overline{\text{COD\_IOW}}$	Output	Codec IO Write. This output indicates that the current operation to the Codec is a write.
COD_ADR[1:0]	Output	Codec Address. This output selects one of four 8-bit internal registers in the Codec during slave PIO cycles. These bits are directly driven from the SB_PA[3:2] input pins.
BPA	Output	Bit Port A. A generic output sourced from the PIO accessible BPA register.
BPB	Output	Bit Port B. A generic output sourced from the PIO accessible BPB register.
STANDBY	Output	Standby. A Power Management register output pin. Asserted by PIO write operations. De-asserted by any $\overline{\text{SB\_BR}}$ or CPU_IR input.
$\overline{\text{KILL\_COUTLET}}$	Output	Kill Convenience Outlet. A Power Management register output pin. Asserted and de-asserted by PIO write operations
FAN_CTL	Output	Fan Control. A Power Management register output pin. Asserted and de-asserted by PIO write operations
TCK	Input	JTAG Clock. Test input clock for JTAG controller and scan registers.
TRSTN	Input	JTAG Reset pin.
TDI	Input	JTAG Data Input pin.
TDO	Output	JTAG Data Output pin.
TMS	Input	JTAG Mode Select input pin.
AFX_TDO	Input	An input pin from capable of receiving a JTAG scannable bit stream which can then be *spliced* into the STP2024's internal scan chain.
AFX_TDI	Output	An output pin which is either the STP2024's JTAG scan bit stream (if scan chain splice is active) or the generic bit port register, bpc.
$\overline{\text{AFX\_PRESENT}}$	Input	microSPARC-II local bus Present. An input pin which is PIO readable.
PNAND_OUT	Output	A series of serial connections of all STP2024 input and bidirectional pins, through NAND gates. Ends at this output pin. Used for test purposes only.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings [1]

Symbol	Name	Rating	Units
V_{CC}	Power supply voltage	+7.0	V
V_{IN}	Input voltage (any pin)	$GND \le V_{IN} \le V_{CC}$	V
P_D	Power dissipation	500	mW
T_J	Operating junction temperature	0 to +105	°C
T_S	Storage temperature	-40 to +125	°C
	Static Discharge Voltage	2000	V

1. Operation of the device at values in excess of those listed above will result in degradation or destruction of the device. All voltages are defined with respect to ground. Functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Name	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
V_{IN}	DC input voltage	0	–	V_{CC}	V
P_D	Power dissipation	–	370	500	mW
T_A	Operating Free-Air Temperature	0	–	70	°C

Capacitance

Symbol	Description	PQCL Max	Units
C_{IN}	Input Capacitance	3	pF
C_{OUT}	Output Capacitance	2.7	pF
C_{BI}	Bidirectional Capacitance	3	pF

DC Characteristics (V_{CC} = 5.0V ±5%)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Minimum High Level Input Voltage		2.0	–	–	V
V_{IL}	Maximum Low Level Input Voltage		–	–	0.8	V
V_{OH}	Minimum High Level Output Voltage	I_{OH} = -4.0 mA, V_{CC}=min, I_{OH} = -6.0 mA, V_{CC} = min, [1] I_{OH} = -8.0 mA, V_{CC} = min, [2]	2.4	4.5	–	V V V
V_{OL}	Minimum High Level Output Voltage	I_{OL} = 4.0 mA, V_{CC} = min, I_{OL} = 6.0 mA, V_{CC} = min, [1] I_{OL} = 8.0 mA, V_{CC} = min, [2]	–	0.2	0.4	V V V
I_{IN}	Minimum Input Current	V_{IN} = V_{CC} or GND	-10	–	+10	µA
I_{OZ}	Maximum Output Leakage Current	V_{OUT} = V_{CC} or GND Output Disabled	-10	–	+10	µA

1. SB_INT_1 output only.
2. SB_DATA[31:0], SB_SIZ[2:0], $\overline{\text{SB\_ACK}}$[2:0], SB_READ outputs only.

AC Characteristics: Input Pins

Signal	Parameter	Conditions	Reference Edge	Min	Max	Unit
SB_CLK	t_{CLK}			16	25	MHz
	t_{CH}			17	–	ns
	t_{CL}			17	–	ns
	t_{CR}			1	3	ns
	t_{CF}			1	3	ns
TCK	t_{CH}	JTAG_CLK		25	–	ns
	t_{CL}	T_{CYC} >=100ns		25	–	ns
	t_{CR}			–	10	ns
	t_{CF}			–	10	ns
$\overline{\text{SB\_RESET}}$	t_{SI}		SB_CLK+	15	–	ns
	t_{HI}		SB_CLK+	–	1	ns
TRSTN	t_{SI}	2 cycles	TCK+	10	–	ns
	t_{HI}		TCK+	0	–	ns
TDI	t_{SI}		TCK+	10	–	ns
	t_{HI}		TCK+	0	–	ns
TMS	t_{SI}		TCK+	10	–	ns
	t_{HI}		TCK+	0	–	ns
AFX_TDO	t_{SI}		TCK+	10	–	ns
	t_{HI}		TCK+	0	–	ns
$\overline{\text{AFX\_PRESENT}}$		DC level		N/A	N/A	ns
SB_PA[27:24, 5:2]	t_{SI}		SB_CLK+	15	–	ns
	t_{HI}		SB_CLK+	–	1	ns
$\overline{\text{SB\_AS}}$	t_{SI}		SB_CLK+	15	–	ns
	t_{HI}		SB_CLK+	–	1	ns
$\overline{\text{SB\_SEL}}$	t_{SI}		SB_CLK+	15	–	ns
	t_{HI}		SB_CLK+	–	1	ns
$\overline{\text{SB\_BR}}$ [2:0]	t_{SI}		SB_CLK+	15	–	ns
	t_{HI}		SB_CLK+	–	1	ns
$\overline{\text{SB\_BG}}$ [5:3]	t_{SI}		SB_CLK+	15	–	ns
	t_{HI}		SB_CLK+	–	1	ns
CPU_IR[3:0]	t_{SI}		SB_CLK+	15	–	ns
	t_{HI}		SB_CLK+	–	1	ns
$\overline{\text{MBR}}$	t_{SI}		SB_CLK+	15	–	ns
	t_{HI}		SB_CLK+	–	1	ns
COD_PREQ	t_{SI}		SB_CLK+	N/A	N/A	ns
	t_{HI}		SB_CLK+			ns
COD_CREQ	t_{SI}		SB_CLK+	N/A	N/A	ns
	t_{HI}		SB_CLK+			ns

AC Characteristics: Bidirectional Pins

Signal	Parameter	Conditions	Reference Edge	Min	Max	Unit
SB_DATA[31:0]	t_{DO}	70C, 4.75V, 100pf	SB_CLK+	–	22.5	ns
	t_{HO}	0C, 5.25V, 100pf	SB_CLK+	5.4	–	ns
	t_{SI}		SB_CLK+	15	–	ns
	t_{HI}		SB_CLK+	–	1	ns
SB_SIZ[2:0]	t_{DO}	70C, 4.75V, 100pf	SB_CLK+	–	20.9	ns
	t_{HO}	0C, 5.25V, 100pf	SB_CLK+	5.6	–	ns
	t_{SI}		SB_CLK+	15	–	ns
	t_{HI}		SB_CLK+	–	1	ns
SB_READ	t_{DO}	70C, 4.75V, 100pf	SB_CLK+	–	20.6	ns
	t_{HO}	0C, 5.25V, 100pf	SB_CLK+	4.7	–	ns
	t_{SI}		SB_CLK+	15	–1	ns
	t_{HI}		SB_CLK+	–		ns
$\overline{\text{SB\_ACK}}$[2:0]	t_{DO}	70C, 4.75V, 100pf	SB_CLK+	–	20	ns
	t_{HO}	0C, 5.25V, 100pf	SB_CLK+	5.0	–	ns
	t_{SI}		SB_CLK+	15	–	ns
	t_{HI}		SB_CLK+	–	1	ns
COD_DATA[7:0]	t_{DO}	70C, 4.75V, 15pf	SB_CLK+	–	10.7	ns
	t_{HO}	0C, 5.25V, 15pf	SB_CLK+	–	–	ns
	t_{SI}		$\overline{\text{COD\_IOW}}$	22	–	ns
	t_{HI}		$\overline{\text{COD\_IOW}}$	–	0	ns

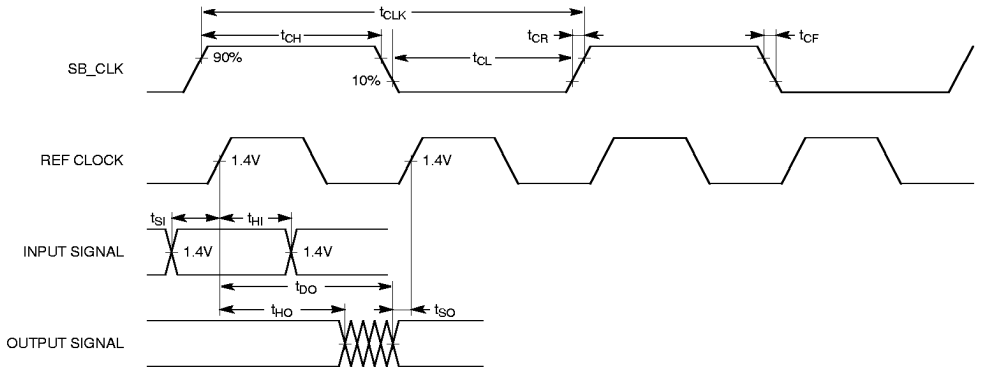
AC Characteristics: Output Pins

Signal	Parameter	Conditions	Reference Edge	Min	Max	Unit
SB_BR[4]	t_{DO}	70C, 4.75V, 60pf	SB_CLK+	–	21	ns
	t_{HO}	70C, 4.75V, 60pf	SB_CLK+	5.5	–	ns
SB_BR[5, 3]	t_{DO}	70C, 4.75V, 20pf	SB_CLK+	–	20.7	ns
	t_{HO}	70C, 4.75V, 20pf	SB_CLK+	2.5	–	ns
	t_{DO}	70C, 5.0V, 20pf	MBR	–	7.6	ns
MBG	t_{DO}	70C, 4.75V, 20pf	SB_CLK+	–	20	ns
	t_{HO}	70C, 4.75V, 20pf	SB_CLK+	3.4	–	ns
	t_{DO}	70C, 5.0V, 20pf	SB_BG [5,3]	–	7.6	ns
SB_INT	t_{DO}	70C, 4.75V, 100pf, L-H	SB_CLK+	–	12.3	ns
		70C, 4.75V, 100pf, H-L	SB_CLK+	–	21.5	ns
	t_{HO}	0C, 5.25V, 100pf, L-H	SB_CLK+	4.0	–	ns
		0C, 5.25V, 100pf, H-L	SB_CLK+	6.3	–	ns
BPA	t_{DO}	70C, 4.75V, 15pf	SB_CLK+	–	13	ns
	t_{HO}	0C, 5.25V, 15pf	SB_CLK+	4.0	–	ns
BPB	t_{DO}	70C, 4.75V, 15pf	SB_CLK+	–	13	ns
	t_{HO}	0C, 5.25V, 15pf	SB_CLK+	4.0	–	ns
STANDBY	t_{DO}	70C, 4.75V, 15pf	SB_CLK+	–	13	ns
	t_{HO}	0C, 5.25V, 15pf	SB_CLK+	4.2	–	ns
KILL_COUTLET	t_{DO}	70C, 4.75V, 30pf	SB_CLK+	–	13	ns
	t_{HO}	0C, 5.25V, 30pf	SB_CLK+	4.0	–	ns
FAN_CTL	t_{DO}	70C, 4.75V, 30pf	SB_CLK+	–	13	ns
	t_{HO}	0C, 5.25V, 30pf	SB_CLK+	4.2	–	ns
IO_SEL	t_{DO}	70C, 4.75V, 15pf	SB_PA[27:25]	–	9.9	ns
	t_{HO}	0C, 5.25V, 15pf	SB_PA[27:25]	3.7	–	ns
AFX_TDI	t_{DO}	70C, 4.75V, 15pf	SB_CLK+	–	13	ns
	t_{HO}	0C, 5.25V, 15pf	SB_CLK+	4.1	–	ns
TDO	t_{DO}	70C, 4.75V, 15pf	TCK+	–	–	ns
	t_{HO}	0C, 5.25V, 15pf	TCK+	8.3	–	ns
PNAND_OUT	t_{DO}	70C, 4.75V, 15pf	SB_READ+	–	200.6	ns
	t_{HO}	0C, 5.25V, 15pf	SB_READ+	–	–	ns
COD_CS	t_{DO}	70C, 4.75V, 15pf	SB_CLK+	–	12.5	ns
	t_{HO}	0C, 5.25V, 15pf	SB_CLK+	4.0	–	ns
COD_ADR[1:0]	t_{DO}	70C, 4.75V, 15pf	SB_PA[3:2]	–	8.4	ns
	t_{HO}	0C, 5.25V, 15pf	SB_PA[3:2]	2.3	–	ns
COD_IOW	t_{DO}	70C, 4.75V, 15pf	SB_CLK+	–	14.8	ns
	t_{HO}	0C, 5.25V, 15pf	SB_CLK+	4.4	–	ns
COD_IOR	t_{DO}	70C, 4.75V, 15pf	SB_CLK+	–	15.1	ns
	t_{HO}	0C, 5.25V, 15pf	SB_CLK+	4.4	–	ns

AC Characteristics: Output Pins (Continued)

Signal	Parameter	Conditions	Reference Edge	Min	Max	Unit
$\overline{\text{COD\_PACK}}$	t_{DO}	70C, 4.75V, 15pf	SB_CLK+	–	13.8	ns
	t_{HO}	0C, 5.25V, 15pf	SB_CLK+	4.0	–	ns
$\overline{\text{COD\_CACK}}$	t_{DO}	70C, 4.75V, 15pf	SB_CLK+	–	13.8	ns
	t_{HO}	0C, 5.25V, 15pf	SB_CLK+	4.0	–	ns
$\overline{\text{COD\_PDWN}}$	t_{DO}	70C, 4.75V, 15pf	SB_CLK+	–	12.7	ns
	t_{HO}	0C, 5.25V, 15pf	SB_CLK+	4.4	–	ns

TIMING DIAGRAMS



Parameter Definitions

t_{SI} : Required setup time of a chip input referenced to a given (clock) edge.
t_{HI} : Required hold time of a chip input referenced to a given (clock) edge.
t_{HO} : Guaranteed hold time of an output referenced to a given (clock) edge.
t_{SO} : Guaranteed setup time of an output referenced to a next given (clock) edge.
t_{DO} : Guaranteed propagation time of an output referenced to a given (clock) edge.
t_{CH} : Required clock high time.
t_{CL} : Required clock low time.
t_{CR} : Required clock rise time.
t_{CF} : Required clock fall time.

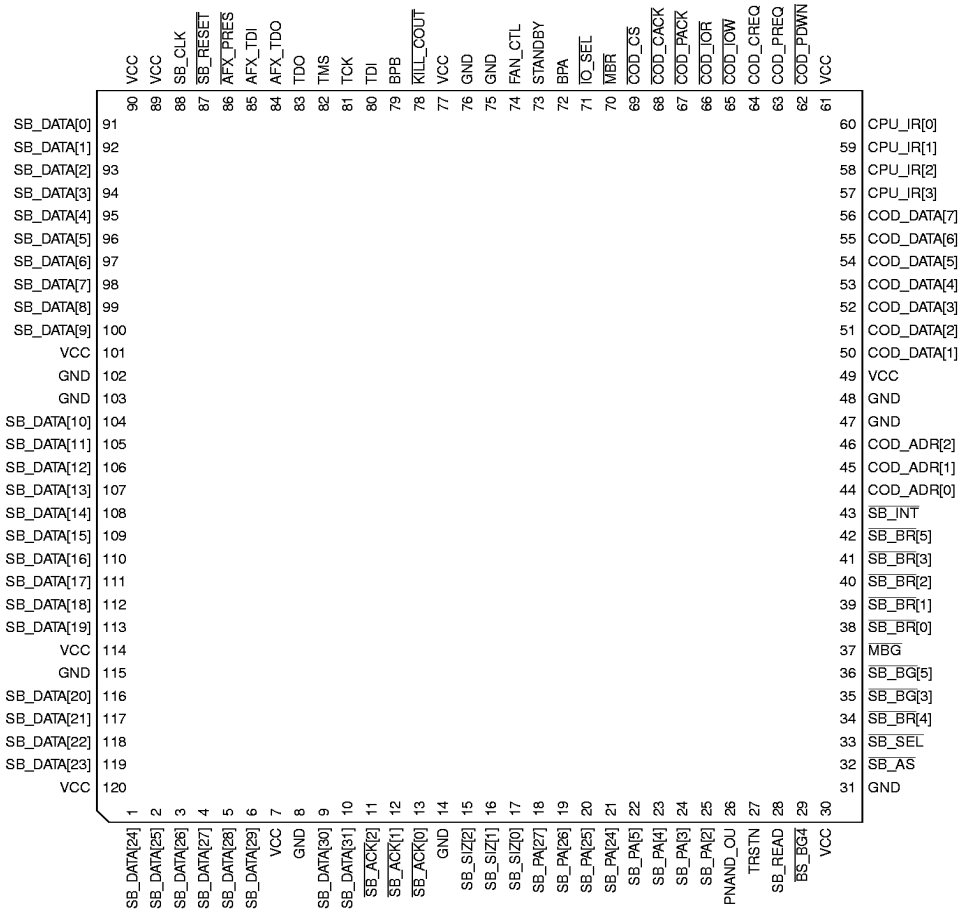
Figure 3. Clock & I/O Waveforms

PACKAGING INFORMATION

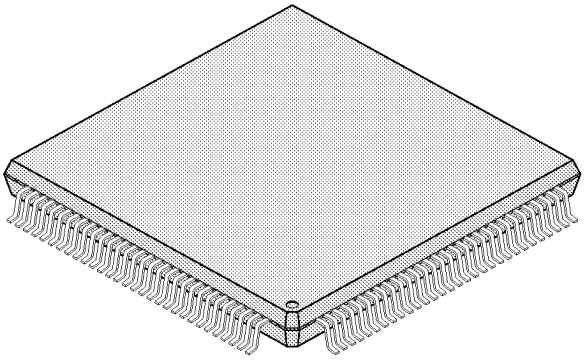
120-Pin PQFP Pin Assignment

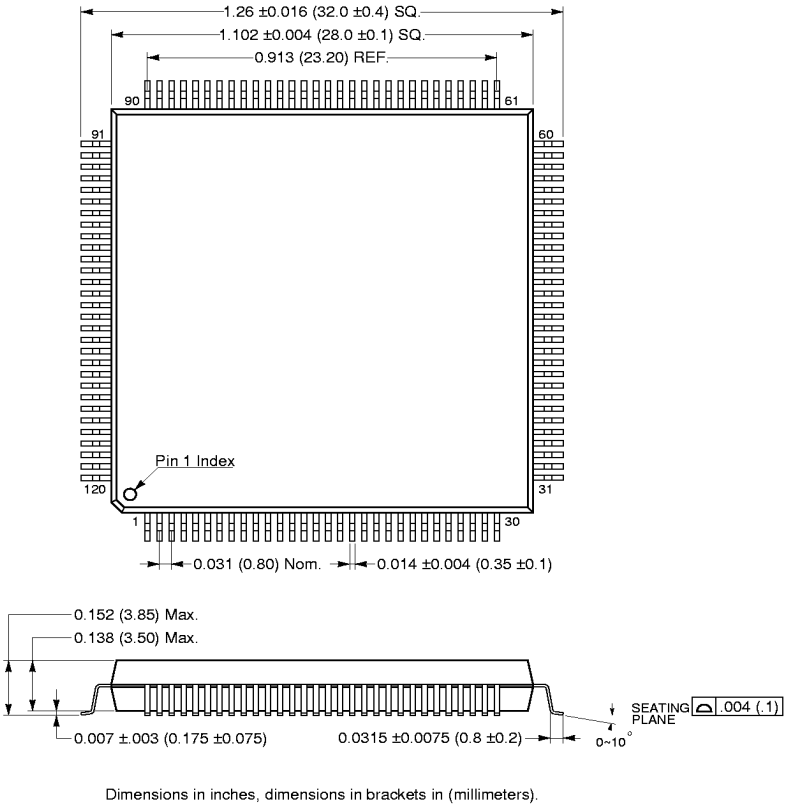
Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	SB_DATA[24]	31	GND	61	V_{CC}	91	SB_DATA[0]
2	SB_DATA[25]	32	$\overline{\text{SB\_AS}}$	62	$\overline{\text{COD\_PDWN}}$	92	SB_DATA[1]
3	SB_DATA[26]	33	$\overline{\text{SB\_SEL}}$	63	COD_PREQ	93	SB_DATA[2]
4	SB_DATA[27]	34	$\overline{\text{SB\_BR}}$[4]	64	COD_CREQ	94	SB_DATA[3]
5	SB_DATA[28]	35	$\overline{\text{SB\_BG}}$[3]	65	$\overline{\text{COD\_IOW}}$	95	SB_DATA[4]
6	SB_DATA[29]	36	$\overline{\text{SB\_BG}}$[5]	66	$\overline{\text{COD\_IOR}}$	96	SB_DATA[5]
7	V_{CC}	37	$\overline{\text{MBG}}$	67	$\overline{\text{COD\_PACK}}$	97	SB_DATA[6]
8	GND	38	$\overline{\text{SB\_BR}}$[0]	68	$\overline{\text{COD\_CACK}}$	98	SB_DATA[7]
9	SB_DATA[30]	39	$\overline{\text{SB\_BR}}$[1]	69	$\overline{\text{COD\_CS}}$	99	SB_DATA[8]
10	SB_DATA[31]	40	$\overline{\text{SB\_BR}}$[2]	70	$\overline{\text{MBR}}$	100	SB_DATA[9]
11	$\overline{\text{SB\_ACK}}$[2]	41	$\overline{\text{SB\_BR}}$[3]	71	$\overline{\text{IO\_SEL}}$	101	V_{CC}
12	$\overline{\text{SB\_ACK}}$[1]	42	$\overline{\text{SB\_BR}}$[5]	72	BPA	102	GND
13	$\overline{\text{SB\_ACK}}$[0]	43	$\overline{\text{SB\_INT}}$	73	STANDBY	103	GND
14	GND	44	COD_ADR[0]	74	FAN_CTL	104	SB_DATA[10]
15	SB_SIZ[2]	45	COD_ADR[1]	75	GND	105	SB_DATA[11]
16	SB_SIZ[1]	46	COD_DATA[0]	76	GND	106	SB_DATA[12]
17	SB_SIZ[0]	47	GND	77	V_{CC}	107	SB_DATA[13]
18	SB_PA[27]	48	GND	78	$\overline{\text{KILL\_COUT}}$	108	SB_DATA[14]
19	SB_PA[26]	49	V_{CC}	79	BPB	109	SB_DATA[15]
20	SB_PA[25]	50	COD_DATA[1]	80	TDI	110	SB_DATA[16]
21	SB_PA[24]	51	COD_DATA[2]	81	TCK	111	SB_DATA[17]
22	SB_PA[5]	52	COD_DATA[3]	82	TMS	112	SB_DATA[18]
23	SB_PA[4]	53	COD_DATA[4]	83	TDO	113	SB_DATA[19]
24	SB_PA[3]	54	COD_DATA[5]	84	AFX_TDO	114	V_{CC}
25	SB_PA[2]	55	COD_DATA[6]	85	AFX_TDI	115	GND
26	PNAND_OUT	56	COD_DATA[7]	86	$\overline{\text{AFX\_PRES}}$	116	SB_DATA[20]
27	TRSTN	57	CPU_IR3	87	$\overline{\text{SB\_RESET}}$	117	SB_DATA[21]
28	SB_READ	58	CPU_IR2	88	SB_CLK	118	SB_DATA[22]
29	$\overline{\text{BS\_BG}}$[4]	59	CPU_IR1	89	V_{CC}	119	SB_DATA[23]
30	V_{CC}	60	CPU_IR0	90	V_{CC}	120	V_{CC}

120-Pin PQFP Package Pinout



120-Pin PQFP Package Dimensions





Dimensions in inches, dimensions in brackets in (millimeters).

ORDERING INFORMATION

Part Number	Description
STP1024PQFP	120-Pin Plastic Quad Flat Pack (PQFP)

Document Part Number: STP2024