

## 8K/16K 1.8V Microwire® Serial EEPROM

### FEATURES

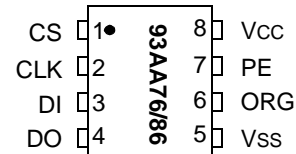
- Single supply operation down to 1.8V
- Low power CMOS technology
  - 1 mA active current typical
  - 5  $\mu$ A standby current (typical) at 3.0V
- ORG pin selectable memory configuration
  - 1024 x 8 or 512 x 16-bit organization (93AA76)
  - 2048 x 8 or 1024 x 16-bit organization (93AA86)
- Self-timed ERASE and WRITE cycles
- Automatic ERAL before WRAL
- Power on/off data protection circuitry
- Industry standard 3-wire serial I/O
- Device status signal during ERASE/WRITE cycles
- Sequential READ function
- 1,000,000 ERASE/WRITE cycles ensured
- Data retention > 200 years
- 8-pin PDIP/SOIC package
- Temperature ranges available:
  - Commercial (C): 0°C to +70°C

### DESCRIPTION

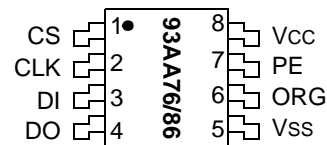
The Microchip Technology Inc. 93AA76/86 are 8K and 16K low voltage serial Electrically Erasable PROMs. The device memory is configured as x8 or x16 bits depending on the ORG pin setup. Advanced CMOS technology makes these devices ideal for low power non-volatile memory applications. These devices also have a Program Enable (PE) pin to allow the user to write protect the entire contents of the memory array. The 93AA76/86 is available in standard 8-pin DIP and 8-pin surface mount SOIC packages.

### PACKAGE TYPES

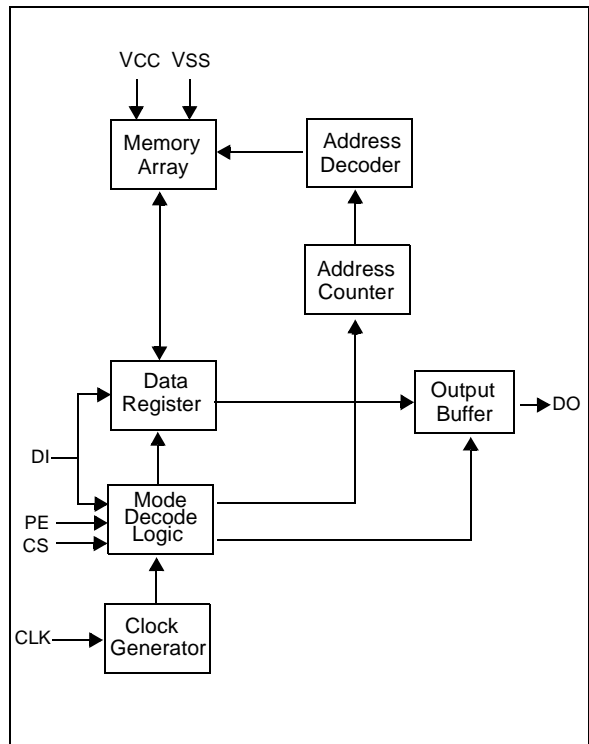
#### DIP Package



#### SOIC Package



### BLOCK DIAGRAM



## 1.0 ELECTRICAL CHARACTERISTICS

### 1.1 Maximum Ratings\*

VCC .....7.0V  
 All inputs and outputs w.r.t. VSS ..... -0.6V to Vcc +1.0V  
 Storage temperature ..... -65°C to +150°C  
 Ambient temp. with power applied ..... -65°C to +125°C  
 Soldering temperature of leads (10 seconds) ..... +300°C  
 ESD protection on all pins ..... 4 kV

**\*Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
Vss	Ground
ORG	Memory Configuration
PE	Program Enable
VCC	Power Supply

### 1.2 AC Test Conditions

AC Waveform:

$$V_{LO} = 2.0V$$

$$V_{HI} = V_{CC} - 0.2V \quad (\text{Note 1})$$

$$V_{HI} = 4.0V \text{ for } \quad (\text{Note 2})$$

Timing Measurement Reference Level

Input 0.5 Vcc

Output 0.5 Vcc

Note 1: For Vcc ≤ 4.0V

2: For Vcc > 4.0V

TABLE 1-2: DC CHARACTERISTICS

Applicable over recommended operating ranges shown below unless otherwise noted: Vcc = +1.8V to +6.0V Commercial (C): TAMB = 0°C to +70°C					
Parameter	Symbol	Min.	Max.	Units	Conditions
High level input voltage	VIH1	2.0	Vcc +1	V	Vcc ≥ 2.7V
	VIH2	0.7 Vcc	Vcc +1	V	Vcc < 2.7V
Low level input voltage	VIL1	-0.3	0.8	V	Vcc ≥ 2.7V
	VIL2	-0.3	0.2 Vcc	V	Vcc < 2.7V
Low level output voltage	VOL1	—	0.4	V	IOL = 2.1 mA; Vcc = 4.5V
	VOL2	—	0.2	V	IOL = 100 µA; Vcc = Vcc Min.
High level output voltage	VOH1	2.4	—	V	IOH = -400 µA; Vcc = 4.5V
	VOH2	Vcc-0.2	—	V	IOH = -100 µA; Vcc = Vcc Min.
Input leakage current	ILI	-10	10	µA	VIN = 0.1V to Vcc
Output leakage current	ILO	-10	10	µA	VOUT = 0.1V to Vcc
Pin capacitance (all inputs/outputs)	CINT	—	7	pF	(Note Note:) TAMB = +25°C, FCLK = 1 MHz
Operating current	Icc write	—	3	mA	Vcc = 5.5V
	Icc read	—	1 500	mA µA	FCLK = 3 MHz; Vcc = 5.5V FCLK = 1 MHz; Vcc = 3.0V
Standby current	Iccs	—	100	µA	CLK = CS = 0V; Vcc = 5.5V
			30	µA	CLK = CS = 0V; Vcc = 3.0V DI = PE = Vss ORG = Vss or Vcc

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-3: AC CHARACTERISTICS

Applicable over recommended operating ranges shown below unless otherwise noted: V <sub>CC</sub> = +1.8V to +6.0V Commercial (C): T <sub>AMB</sub> = 0°C to +70°C					
Parameter	Symbol	Min.	Max.	Units	Conditions
Clock frequency	F <sub>CLK</sub>	—	3 2 1	MHz MHz Mhz	4.5V ≤ V <sub>CC</sub> ≤ 6.0V 2.5V ≤ V <sub>CC</sub> ≤ 4.5V 1.8V ≤ V <sub>CC</sub> < 2.5V
Clock high time	T <sub>CKH</sub>	200 300 500	—	ns ns ns	4.5V ≥ V <sub>CC</sub> ≤ 6.0V 2.5V ≤ V <sub>CC</sub> < 4.5V 1.8V ≤ V <sub>CC</sub> < 2.5V
Clock low time	T <sub>CKL</sub>	100 200 500	—	ns ns ns	4.5V ≤ V <sub>CC</sub> ≤ 6.0V 2.5V ≤ V <sub>CC</sub> < 4.5V 1.8V ≤ V <sub>CC</sub> < 2.5V
Chip select setup time	T <sub>CSS</sub>	50 100 250	—	ns ns ns	4.5V ≤ V <sub>CC</sub> ≤ 6.0V, Relative to CLK 2.5V ≤ V <sub>CC</sub> < 4.5V, Relative to CLK 1.8V ≤ V <sub>CC</sub> < 2.5V, Relative to CLK
Chip select hold time	T <sub>CSH</sub>	0	—	ns	1.8V ≤ V <sub>CC</sub> ≤ 6.0V
Chip select low time	T <sub>CSL</sub>	250	—	ns	1.8V ≤ V <sub>CC</sub> ≤ 6.0V, Relative to CLK
Data input setup time	T <sub>DIS</sub>	50 100 250	—	ns ns ns	4.5V ≤ V <sub>CC</sub> ≤ 6.0V, Relative to CLK 2.5V ≤ V <sub>CC</sub> < 4.5V, Relative to CLK 1.8V ≤ V <sub>CC</sub> < 2.5V, Relative to CLK
Data input hold time	T <sub>DIH</sub>	50 100 250	—	ns ns ns	4.5V ≤ V <sub>CC</sub> ≤ 6.0V, Relative to CLK 2.5V ≤ V <sub>CC</sub> < 4.5V, Relative to CLK 1.8V ≤ V <sub>CC</sub> < 2.5V, Relative to CLK
Data output delay time	T <sub>PD</sub>	—	100 250 500	ns ns ns	4.5V ≤ V <sub>CC</sub> ≤ 6.0V, C <sub>L</sub> = 100 pF 2.5V ≤ V <sub>CC</sub> < 4.5V, C <sub>L</sub> = 100 pF 1.8V ≤ V <sub>CC</sub> < 2.5V, C <sub>L</sub> = 100 pF
Data output disable time	T <sub>CZ</sub>	—	100 500	ns ns	4.5V ≤ V <sub>CC</sub> ≤ 5.5V (Note 1) 1.8V ≤ V <sub>CC</sub> < 4.5V (Note 1)
Status valid time	T <sub>SV</sub>	—	200 300 500	ns ns ns	4.5V ≥ V <sub>CC</sub> ≤ 6.0V, C <sub>L</sub> = 100 pF 2.5V ≤ V <sub>CC</sub> < 4.5V, C <sub>L</sub> = 100 pF 1.8V ≤ V <sub>CC</sub> < 2.5V, C <sub>L</sub> = 100 pF
Program cycle time	T <sub>WC</sub>	—	5	ms	ERASE/WRITE mode
	T <sub>EC</sub>	—	15	ms	ERAL mode
	T <sub>WL</sub>	—	30	ms	WRAL mode
Endurance	—	1M	—	cycles	25°C, V <sub>CC</sub> = 5.0V, Block Mode (Note 2)

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website:  
[www.microchip.com](http://www.microchip.com)

**TABLE 1-4: INSTRUCTION SET FOR 93AA76: ORG=1 (X16 ORGANIZATION)**

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A8 A7 A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	29
EWEN	1	00	1 1 X X X X X X X X	—	High-Z	13
ERASE	1	11	X A8 A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	13
ERAL	1	00	1 0 X X X X X X X X	—	(RDY/BSY)	13
WRITE	1	01	X A8 A7 A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/BSY)	29
WRAL	1	00	0 1 X X X X X X X X	D15 - D0	(RDY/BSY)	29
EWDS	1	00	0 0 X X X X X X X X	—	High-Z	13

**TABLE 1-5: INSTRUCTION SET FOR 93AA76: ORG=0 (X8 ORGANIZATION)**

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	22
EWEN	1	00	1 1 X X X X X X X X	—	High-Z	14
ERASE	1	11	X A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	14
ERAL	1	00	1 0 X X X X X X X X	—	(RDY/BSY)	14
WRITE	1	01	X A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/BSY)	22
WRAL	1	00	0 1 X X X X X X X X	D7 - D0	(RDY/BSY)	22
EWDS	1	00	0 0 X X X X X X X X	—	High-Z	14

**TABLE 1-6: INSTRUCTION SET FOR 93AA86: ORG=1 (X16 ORGANIZATION)**

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	29
EWEN	1	00	1 1 X X X X X X X X	—	High-Z	13
ERASE	1	11	A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	13
ERAL	1	00	1 0 X X X X X X X X	—	(RDY/BSY)	13
WRITE	1	01	A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/BSY)	29
WRAL	1	00	0 1 X X X X X X X X	D15 - D0	(RDY/BSY)	29
EWDS	1	00	0 0 X X X X X X X X	—	High-Z	13

**TABLE 1-7: INSTRUCTION SET FOR 93AA86: ORG=0 (X8 ORGANIZATION)**

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	22
EWEN	1	00	1 1 X X X X X X X X	—	High-Z	14
ERASE	1	11	A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	14
ERAL	1	00	1 0 X X X X X X X X	—	(RDY/BSY)	14
WRITE	1	01	A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/BSY)	22
WRAL	1	00	0 1 X X X X X X X X	D7 - D0	(RDY/BSY)	22
EWDS	1	00	0 0 X X X X X X X X	—	High-Z	14

## 2.0 PRINCIPLES OF OPERATION

When the ORG pin is connected to Vcc, the x16 organization is selected. When it is connected to ground, the x8 organization is selected. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a high-Z state except when reading data from the device, or when checking the READY/BUSY status during a programming operation. The READY/BUSY status can be verified during an Erase/Write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. The DO will enter the high impedance state on the falling edge of the CS.

### 2.1 START Condition

The START bit is detected by the device if CS and DI are both HIGH with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction are clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new start condition is detected.

### 2.2 DI/DO

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic HIGH level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

### 2.3 Erase/Write Enable and Disable (EWEN, EWDS)

The 93AA76/86 powers up in the Erase/Write Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or Vcc is removed from the device. To protect against accidental data disturb, the EWDS instruction can be used to disable all Erase/Write functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

### 2.4 Data Protection

During power-up, all programming modes of operation are inhibited until Vcc has reached a level greater than 1.4V. During power-down, the source data protection circuitry acts to inhibit all programming modes when Vcc has fallen below 1.4V.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed.

## 3.0 DEVICE OPERATION

### 3.1 READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 16 bit (x16 organization) or 8 bit (x8 organization) output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high and clock transitions continue. The memory address pointer will automatically increment and output data sequentially.

### 3.2 ERASE

The ERASE instruction forces all data bits of the specified address to the logical "1" state. The self-timed programming cycle is initiated on the rising edge of CLK as the last address bit (A0) is clocked in. At this point, the CLK, CS, and DI inputs become don't cares.

The DO pin indicates the  $\overline{\text{READY}}/\overline{\text{BUSY}}$  status of the device if the CS is high. The  $\overline{\text{READY}}/\overline{\text{BUSY}}$  status will be displayed on the DO pin until the next start bit is received as long as CS is high. Bringing the CS low will place the device in standby mode and cause the DO pin to enter the high impedance state. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been erased and the device is ready for another instruction.

The ERASE cycle takes 3 ms per word (Typical).

### 3.3 WRITE

The WRITE instruction is followed by 16 bits (or by 8 bits) of data to be written into the specified address. The self-timed programming cycle is initiated on the rising edge of CLK as the last data bit (D0) is clocked in. At this point, the CLK, CS, and DI inputs become don't cares.

The DO pin indicates the  $\overline{\text{READY}}/\overline{\text{BUSY}}$  status of the device if the CS is high. The  $\overline{\text{READY}}/\overline{\text{BUSY}}$  status will be displayed on the DO pin until the next start bit is received as long as CS is high. Bringing the CS low will place the device in standby mode and cause the DO pin to enter the high impedance state. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been written and the device is ready for another instruction.

The WRITE cycle takes 3 ms per word (Typical).

### 3.4 Erase All (ERAL)

The ERAL instruction will erase the entire memory array to the logical "1" state. The ERAL cycle is identical to the ERASE cycle except for the different opcode. The ERAL cycle is completely self-timed and commences on the rising edge of the last address bit (A0). Note that the least significant 8 or 9 address bits are don't care bits, depending on selection of x16 or x8 mode. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ERAL instruction is guaranteed at  $V_{cc} = +4.5V$  to  $+6.0V$ .

The DO pin indicates the  $\overline{\text{READY}}/\overline{\text{BUSY}}$  status of the device if the CS is high. The  $\overline{\text{READY}}/\overline{\text{BUSY}}$  status will be displayed on the DO pin until the next start bit is received as long as CS is high. Bringing the CS low will place the device in standby mode and cause the DO pin to enter the high impedance state. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the entire device has been erased and is ready for another instruction.

The ERAL cycle takes 15 ms maximum (8 ms typical).

### 3.5 Write All (WRAL)

The WRAL instruction will write the entire memory array with the data specified in the command. The WRAL cycle is completely self-timed and commences on the rising edge of the last address bit (A0). Note that the least significant 8 or 9 address bits are don't cares, depending on selection of x16 or x8 mode. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction but the chip must be in the EWEN status. The WRAL instruction is guaranteed at  $V_{cc} = +4.5V$  to  $+6.0V$ .

The DO pin indicates the  $\overline{\text{READY}}/\overline{\text{BUSY}}$  status of the device if the CS is high. The  $\overline{\text{READY}}/\overline{\text{BUSY}}$  status will be displayed on the DO pin until the next start bit is received as long as CS is high. Bringing the CS low will place the device in standby mode and cause the DO pin to enter the high impedance state. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the entire device has been written and is ready for another instruction.

The WRAL cycle takes 30 ms maximum (16 ms typical).

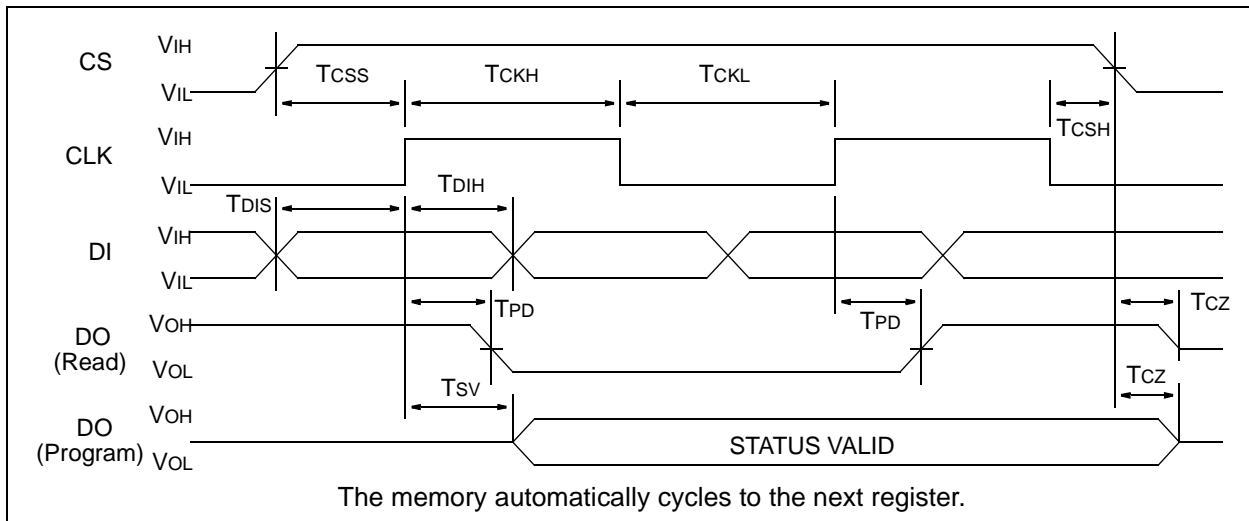
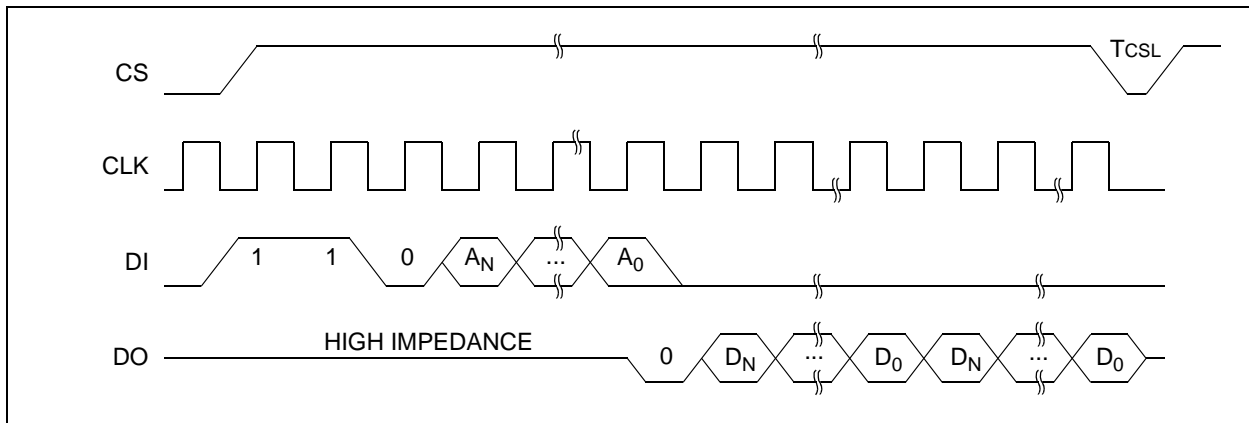
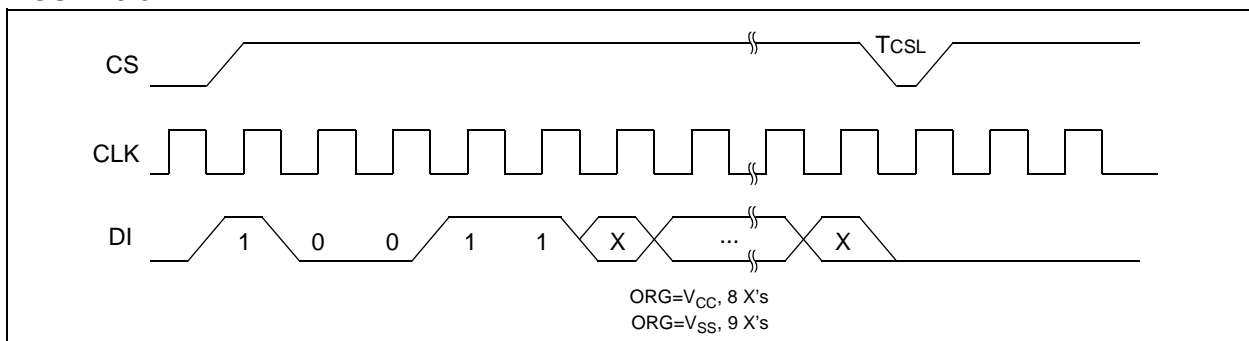
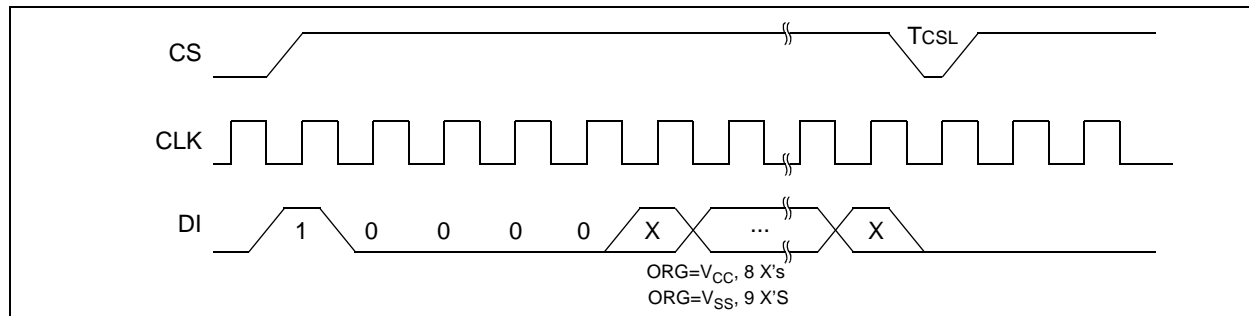
**FIGURE 3-1: SYNCHRONOUS DATA TIMING****FIGURE 3-2: READ****FIGURE 3-3: EWEN****FIGURE 3-4: EWDS**

FIGURE 3-5: WRITE

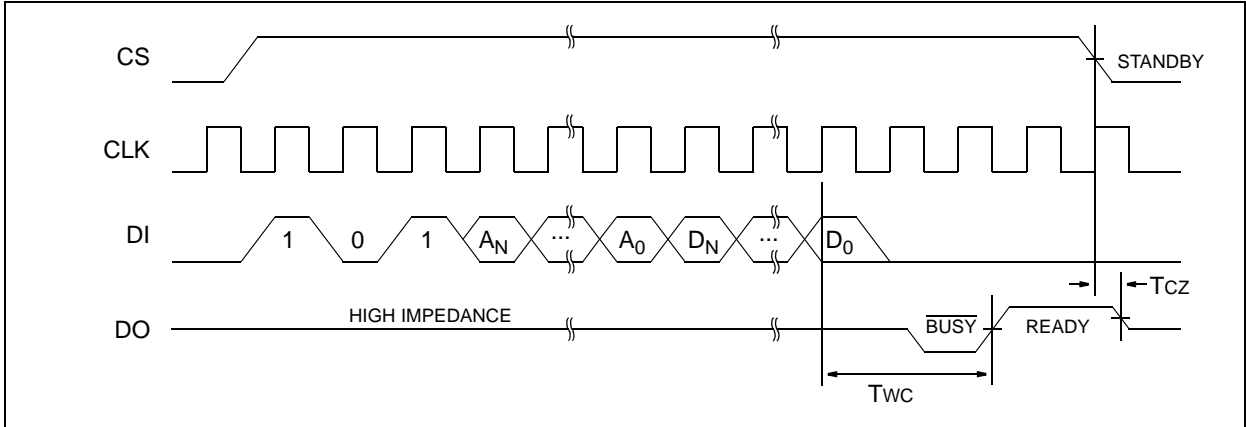


FIGURE 3-6: WRAL

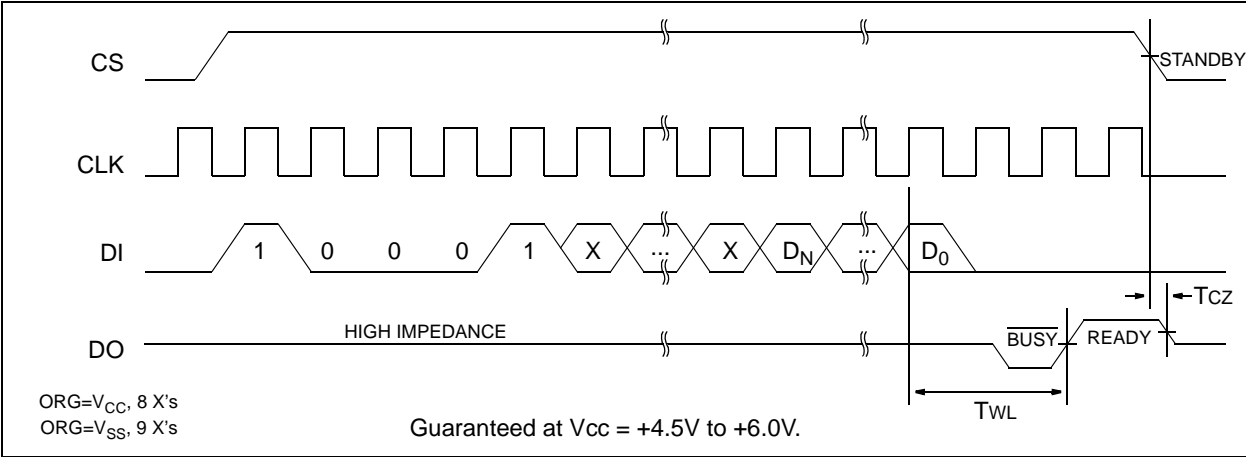


FIGURE 3-7: ERASE

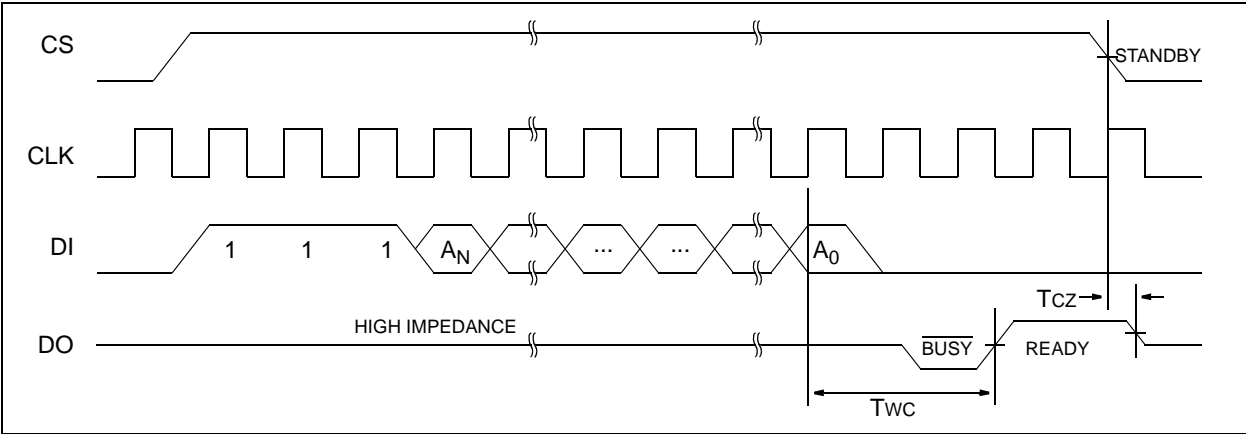
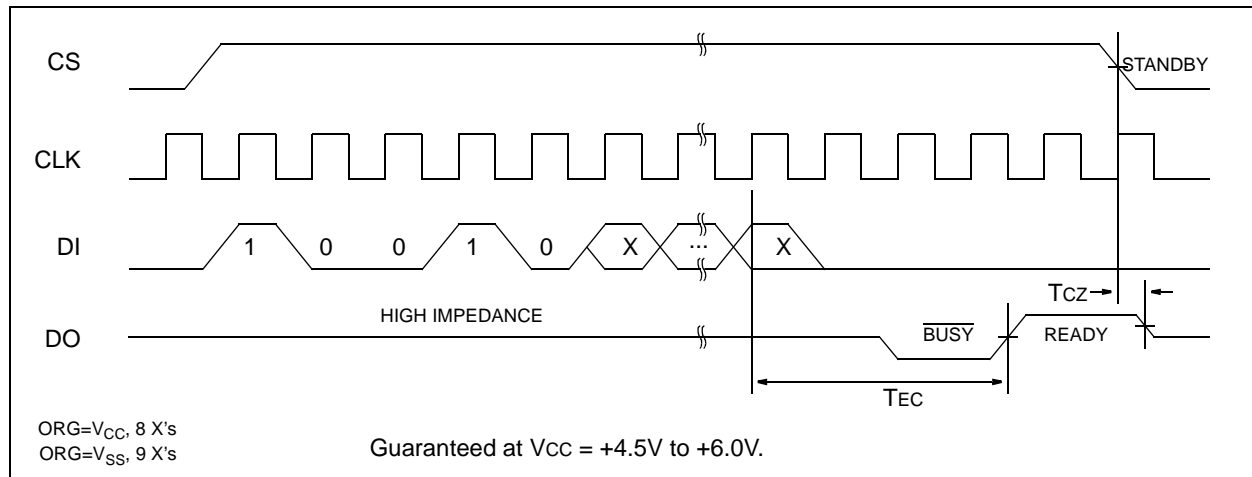


FIGURE 3-8: ERAL



## 4.0 PIN DESCRIPTIONS

### 4.1 Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated will be completed, regardless of the CS input signal. If CS is brought LOW during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be LOW for 250 ns minimum (T<sub>CSL</sub>) between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

### 4.2 Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93AA76/86. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime with respect to clock HIGH time (T<sub>CKH</sub>) and clock LOW time (T<sub>CKL</sub>). This gives the controlling master freedom in preparing opcode, address, and data.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detection of a start condition the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all opcode, address, and data bits before an instruction is executed (see Table 1-4

through Table 1-7 for more details). CLK and DI then become don't care inputs waiting for a new start condition to be detected.

**Note:** CS must go LOW between consecutive instructions, except when performing a sequential read (Refer to Section 3.1 for more detail on sequential reads).

### 4.3 Data In (DI)

Data In is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

### 4.4 Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (T<sub>PD</sub> after the positive edge of CLK).

This pin also provides READY/BUSY status information during ERASE and WRITE cycles. READY/BUSY status information is available when CS is high. It will be displayed until the next start bit occurs as long as CS stays high.

### 4.5 Organization (ORG)

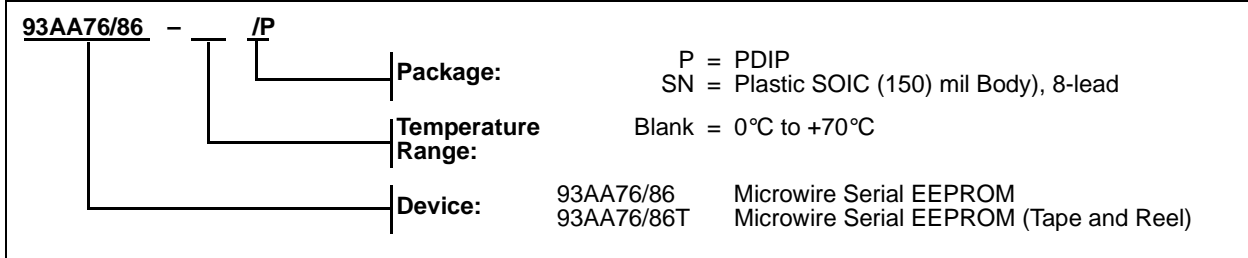
When ORG is connected to V<sub>CC</sub>, the x16 memory organization is selected. When ORG is tied to V<sub>SS</sub>, the x8 memory organization is selected. There is an internal pull-up resistor on the ORG pin that will select x16 organization when left unconnected.

### 4.6 Program Enable (PE)

This pin allows the user to enable or disable the ability to write data to the memory array. If the PE pin is floated or tied to V<sub>CC</sub>, the device can be programmed. If the PE pin is tied to V<sub>SS</sub>, programming will be inhibited. There is an internal pull-up on this device that enables programming if this pin is left floating.

## 93AA76/86 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



## Sales and Support

### Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Web Site ([www.microchip.com](http://www.microchip.com))

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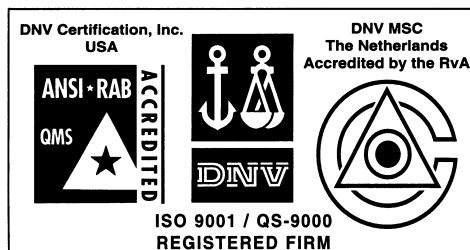
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## WORLDWIDE SALES AND SERVICE

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#### Corporate Office

2355 West Chandler Blvd.  
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Tel: 480-792-7200 Fax: 480-792-7277  
Technical Support: 480-792-7627  
Web Address: <http://www.microchip.com>

#### Rocky Mountain

2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 480-792-7966 Fax: 480-792-7456

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500 Sugar Mill Road, Suite 200B  
Atlanta, GA 30350  
Tel: 770-640-0034 Fax: 770-640-0307

#### Austin

Analog Product Sales  
8303 MoPac Expressway North  
Suite A-201  
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2 Lan Drive, Suite 120  
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#### Boston

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Tel: 972-818-7423 Fax: 972-818-2924

#### Dayton

Two Prestige Place, Suite 130  
Miamisburg, OH 45342  
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#### Detroit

Tri-Atria Office Building  
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Farmington Hills, MI 48334  
Tel: 248-538-2250 Fax: 248-538-2260

#### Los Angeles

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Tel: 949-263-1888 Fax: 949-263-1338

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Analog Product Sales  
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Tel: 650-968-9241 Fax: 650-967-1590

#### New York

150 Motor Parkway, Suite 202  
Hauppauge, NY 11788  
Tel: 631-273-5305 Fax: 631-273-5335

#### San Jose

Microchip Technology Inc.  
2107 North First Street, Suite 590  
San Jose, CA 95131  
Tel: 408-436-7950 Fax: 408-436-7955

#### Toronto

6285 Northam Drive, Suite 108  
Mississauga, Ontario L4V 1X5, Canada  
Tel: 905-673-0699 Fax: 905-673-6509

### ASIA/PACIFIC

#### Australia

Microchip Technology Australia Pty Ltd  
Suite 22, 41 Rawson Street  
Epping 2121, NSW  
Australia  
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

#### China - Beijing

Microchip Technology Beijing Office  
Unit 915  
New China Hong Kong Manhattan Bldg.  
No. 6 Chaoyangmen Beidajie  
Beijing, 100027, No. China  
Tel: 86-10-85282100 Fax: 86-10-85282104

#### China - Shanghai

Microchip Technology Shanghai Office  
Room 701, Bldg. B  
Far East International Plaza  
No. 317 Xian Xia Road  
Shanghai, 200051  
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

#### Hong Kong

Microchip Asia Pacific  
RM 2101, Tower 2, Metroplaza  
223 Hing Fong Road  
Kwai Fong, N.T., Hong Kong  
Tel: 852-2401-1200 Fax: 852-2401-3431

#### India

Microchip Technology Inc.  
India Liaison Office  
Divyasree Chambers  
1 Floor, Wing A (A3/A4)  
No. 11, O'Shaughnessey Road  
Bangalore, 560 025, India  
Tel: 91-80-2290061 Fax: 91-80-2290062

#### Japan

Microchip Technology Intl. Inc.  
Benex S-1 6F  
3-18-20, Shinyokohama  
Kohoku-Ku, Yokohama-shi  
Kanagawa, 222-0033, Japan  
Tel: 81-45-471-6166 Fax: 81-45-471-6122

### ASIA/PACIFIC (continued)

#### Korea

Microchip Technology Korea  
168-1, Youngbo Bldg. 3 Floor  
Samsung-Dong, Kangnam-Ku  
Seoul, Korea  
Tel: 82-2-554-7200 Fax: 82-2-558-5934

#### Singapore

Microchip Technology Singapore Pte Ltd.  
200 Middle Road  
#07-02 Prime Centre  
Singapore, 188980  
Tel: 65-334-8870 Fax: 65-334-8850

#### Taiwan

Microchip Technology Taiwan  
11F-3, No. 207  
Tung Hua North Road  
Taipei, 105, Taiwan  
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

### EUROPE

#### Denmark

Microchip Technology Denmark ApS  
Regus Business Centre  
Lautrup høj 1-3  
Ballerup DK-2750 Denmark  
Tel: 45 4420 9895 Fax: 45 4420 9910

#### France

Arizona Microchip Technology SARL  
Parc d'Activite du Moulin de Massy  
43 Rue du Saule Trapu  
Batiment A - 1er Etage  
91300 Massy, France  
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

#### Germany

Arizona Microchip Technology GmbH  
Gustav-Heinemann Ring 125  
D-81739 Munich, Germany  
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

#### Germany

Analog Product Sales  
Lochhamer Strasse 13  
D-82152 Martinsried, Germany  
Tel: 49-89-895650-0 Fax: 49-89-895650-22

#### Italy

Arizona Microchip Technology SRL  
Centro Direzionale Colleoni  
Palazzo Taurus 1 V. Le Colleoni 1  
20041 Agrate Brianza  
Milan, Italy  
Tel: 39-039-65791-1 Fax: 39-039-6899883

#### United Kingdom

Arizona Microchip Technology Ltd.  
505 Eskdale Road  
Winnersh Triangle  
Wokingham  
Berkshire, England RG41 5TU  
Tel: 44 118 921 5869 Fax: 44-118 921-5820

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