PRELIMINARY

Am28F256A

256 Kilobit (32,768 x 8-Bit) CMOS 12.0 Volt, Bulk Erase Flash Memory with Embedded Algorithms

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - — 70 ns maximum access time
- **CMOS low power consumption**
  - — 30 mA maximum active current
  - — 100 µA maximum standby current
  - — No data retention power consumption
- **Compatible with JEDEC-standard byte-wide 32-Pin EPROM pinouts**
  - — 32-pin DIP
  - — 32-pin PLCC
  - — 32-pin TSOP
  - — 32-pin LCC
- **100,000 write/erase cycles minimum**
- **Write and erase voltage 12.0 V ±5%**
- **Latch-up protected to 100 mA from –1 V to Vcc +1 V**
- **Embedded Erase Electrical Bulk Chip-Erase**
  - — 1.5 seconds typical chip-erase including pre-programming
- **Embedded Program**
  - — 14 µs typical byte-program including time-out
  - — 0.5 second typical chip program
- **Command register architecture for microprocessor/microcontroller compatible write interface**
- **On-chip address and data latches**
- **Advanced CMOS flash memory technology**
  - — Low cost single transistor memory cell
- **Embedded algorithms for completely self-timed write/erase operations**

GENERAL DESCRIPTION

The Am28F256A is a 256K Flash memory organized as 32K bytes of 8 bits each. AMD's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The Am28F256A is packaged in 32-pin PDIP, PLCC, and TSOP versions. The device is also offered in the ceramic LCC package. It is designed to be reprogrammed and erased in-system or in standard EPROM programmers. The Am28F256A is erased when shipped from the factory

The standard Am28F256A offers access times as fast as 70 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the Am28F256A has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

AMD's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The Am28F256A uses a command register to manage this functionality, while maintaining a standard JEDEC Flash Standard 32-pin pinout. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming.

AMD's Flash technology reliably stores memory contents even after 100,000 erase and program cycles. The AMD cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The Am28F256A uses a 12.0 V ± 5% V_{PP} supply to perform the erase and programming functions.

The highest degree of latch-up protection is achieved with AMD's proprietary non-epi process. Latch-up protection is provided for stresses up to 100 milliamps on address and data pins from –1 V to Vcc +1 V.

Embedded Program

The Am28F256A is byte programmable using the Embedded Programming algorithm. The Embedded Programming algorithm does not require the system to time-out or verify the data programmed. The typical room temperature programming time of the Am28F256A is one half second.

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GENERAL DESCRIPTION

Embedded Erase

The entire chip is bulk erased using the Embedded Erase algorithm. The Embedded Erase algorithm automatically programs the entire array prior to electrical erase. The timing and verification of electrical erase are controlled internal to the device. Typical erasure at room temperature is accomplished in one second.

AMD's Am28F256A is entirely pin and software compatible with AMD's Am28F020A, Am28F010A and Am28F512A Flash memories.

Embedded Programming Algorithm vs. Flashrite Programming Algorithm

The Flashrite Programming algorithm requires the user to write a program set-up command, a program command (program data and address), and a program verify command followed by a read and compare operation. The user is required to time the programming pulse width in order to issue the program verify command. An integrated stop timer prevents any possibility of overprogramming. Upon completion of this sequence the data is read back from the device and compared by the user with the data intended to be written; if there is not a match, the sequence is repeated until there is a match or the sequence has been repeated 25 times.

AMD's Embedded Programming algorithm requires the user to only write a program set-up command and a program command (program data and address). The device automatically times the programming pulse width, provides the program verify and counts the number of sequences. A status bit, $\overline{\text{Data}}$ Polling, provides feedback to the user as to the status of the programming operation.

Embedded Erase Algorithm vs. Flasherase Erase Algorithm

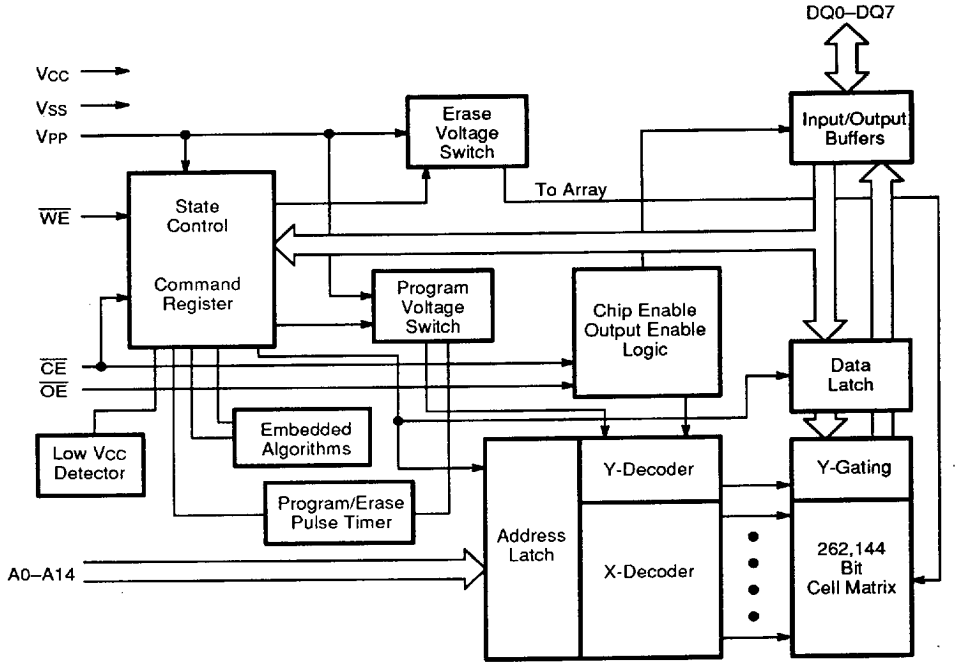
The Flasherase Erase algorithm requires the device to be completely programmed prior to executing an erase command. To invoke the erase operation the user writes an erase set-up command, an erase command, and an erase verify command. The user is required to time the erase pulse width in order to issue the erase verify command. An integrated stop timer prevents any possibility of overerasure. Upon completion of this sequence the data is read back from the device and compared by the user with erased data. If there is not a match, the sequence is repeated until there is a match or the sequence has been repeated 1,000 times.

AMD's Embedded Erase algorithm requires the user to only write an erase set-up command and erase command. The device will automatically pre-program and verify the entire array. Then the device automatically times the erase pulse width, provides the erase verify and counts the number of sequences. A status bit, $\overline{\text{Data}}$ Polling, provides feedback to the user as to the status of the erase operation.

Commands are written to the command register using standard microprocessor write timings. Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. For system design simplification, the Am28F256A is designed to support either $\overline{\text{WE}}$ or $\overline{\text{CE}}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$ whichever occurs last. Data is latched on the rising edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$ whichever occurs first. To simplify the following discussion, the $\overline{\text{WE}}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{\text{WE}}$ signal.

AMD's Flash technology combines years of EPROM and EEPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The Am28F256A electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

BLOCK DIAGRAM



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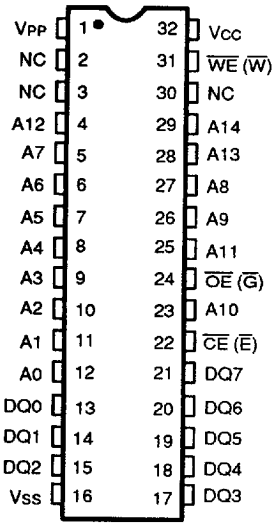
PRODUCT SELECTOR GUIDE

Family Part No.:	Am28F256A				
Ordering Part No.: ±10% Vcc Tolerance		-90	-120	-150	-200
±5% Vcc Tolerance	-75	-95			
Max Access Time (ns)	70	90	120	150	20
$\overline{CE}$ ($\overline{E}$) Access (ns)	70	90	120	150	200
$\overline{OE}$ ($\overline{G}$) Access (ns)	35	35	50	55	55

CONNECTION DIAGRAMS

DIP



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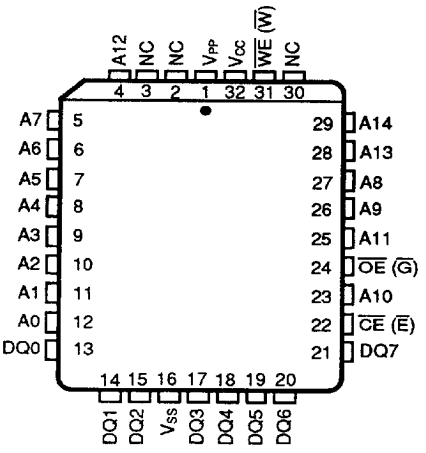
PLCC*



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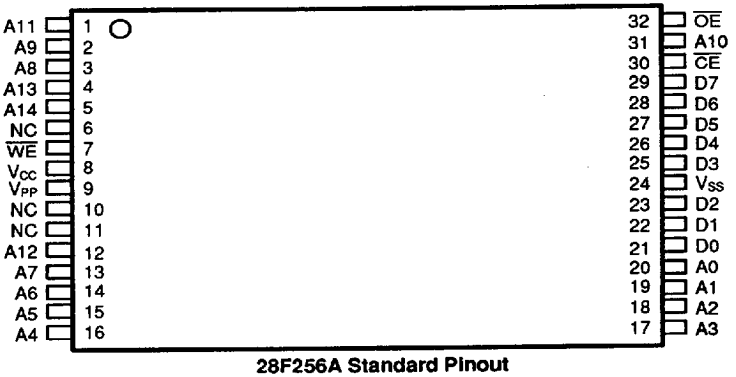
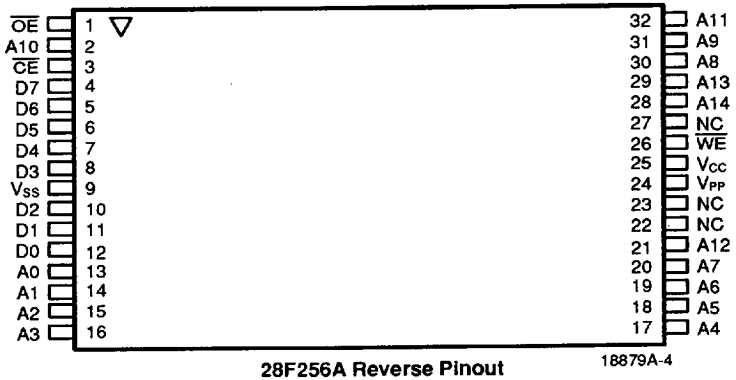
Note: *Pin 1 is marked for orientation.*
**Also available in LCC.*

TSOP PACKAGES



28F256A Standard Pinout



28F256A Reverse Pinout

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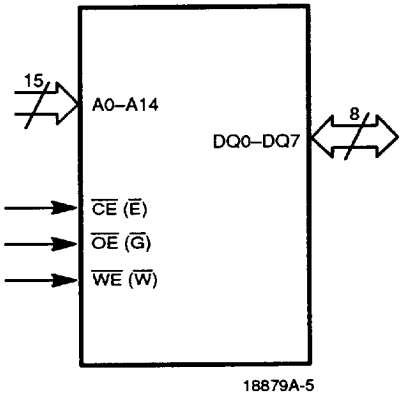
28F256A 32K x 8 Flash Memory in 32-Lead TSOP

LOGIC SYMBOL



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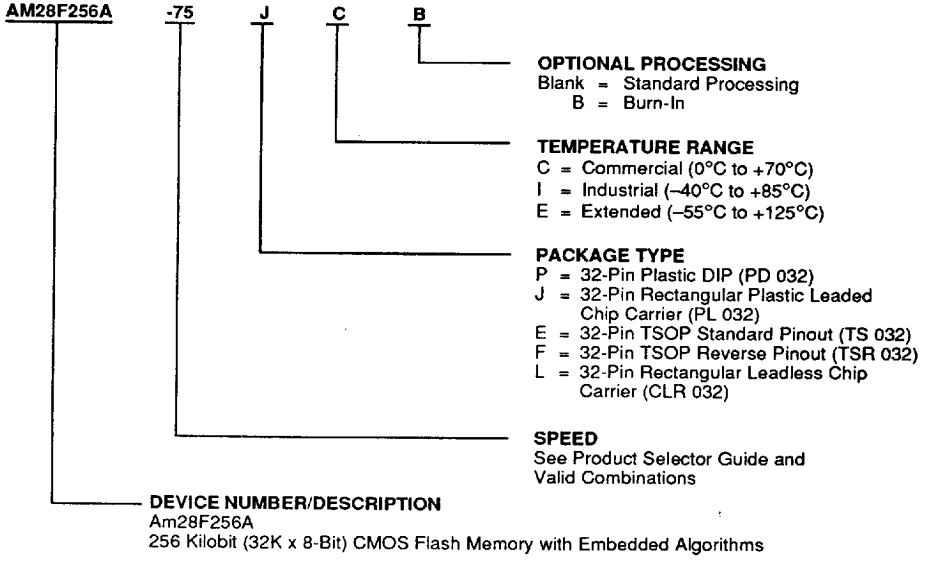
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:



Valid Combinations	
Am28F256A-75 Am28F256A-90 Am28F256A-95	PC, JC, EC, FC, LC
Am28F256A-120 Am28F256A-150 Am28F256A-200	PC, PI, JC, JI, PE, PEB, JE, JEB, EC, FC, EI, FI, EE, FE, EEB, FEB, DI, LC, LI, LE, LEB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PIN DESCRIPTION

A0–A14
Address Inputs for memory locations. Internal latches hold addresses during write cycles.

$\overline{CE}$ ($\overline{E}$)
The Chip Enable active low input activates the chip's control logic and input buffers. Chip Enable high will deselect the device and operates the chip in stand-by mode.

DQ0–DQ7
Data Inputs during memory write cycles. Internal latches hold data during write cycles. Data Outputs during memory read cycles.

NC
No Connect-corresponding pin is not connected internally to the die.

$\overline{OE}$ ($\overline{G}$)
The Output Enable active low input gates the outputs of the device through the data buffers during memory read cycles.

V_{CC}
Power supply for device operation. (5.0 V ± 5% or 10%)

V_{PP}
Power supply for erase and programming. V_{PP} must be at high voltage in order to write to the command register. The command register controls all functions required to alter the memory array contents. Memory contents cannot be altered when $V_{PP} \leq V_{CC} + 2$ V.

V_{SS}
Ground

$\overline{WE}$ ($\overline{W}$)
The Write Enable active low input controls the write function of the command register to the memory array. The target address is latched on the falling edge of the Write Enable pulse and the appropriate data is latched on the rising edge of the pulse.

BASIC PRINCIPLES

The Am28F256A uses 100% TTL-level control inputs to manage the command register. Erase and reprogramming operations use a fixed 12.0 V ± 5% power supply.

Read Only Memory

Without high V_{PP} voltage, the Am28F256A functions as a read only memory and operates like a standard EPROM. The control inputs still manage traditional read, standby, output disable, and Auto select modes.

Command Register

The command register is enabled only when high voltage is applied to the V_{PP} pin. The erase and reprogramming operations are only accessed via the register. In addition, two-cycle commands are required for erase and reprogramming operations. The traditional read, standby, output disable, and Auto select modes are available via the register.

The Am28F256A's command register is written using standard microprocessor write timings. The register controls an internal state machine that manages all device operations. For system design simplification, the Am28F256A is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occur first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

Overview of Erase/Program Operations

Embedded Erase Algorithm

AMD now makes erasure extremely simple and reliable. The Embedded Erase algorithm requires the user to only write an erase set-up command and erase command. The device will automatically pre-program and verify the entire array. The device automatically times the erase pulse width, provides the erase verify and counts the number of sequences. A status bit, $\overline{Data}$ Polling, provides feedback to the user as to the status of the erase operation.

Embedded Programming Algorithm

AMD now makes programming extremely simple and reliable. The Embedded Programming algorithm requires the user to only write a program set-up command and a program command. The device automatically times the programming pulse width, provides the program verify and counts the number of sequences. A status bit, $\overline{Data}$ Polling, provides feedback to the user as to the status of the programming operation.

Data Protection

The Am28F256A is designed to offer protection against accidental erasure or programming, caused by spurious system level signals that may exist during power transitions. The Am28F256A powers up in its read only state. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than 3.2 V (typically 3.7 V). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. The device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above 3.2 V.

Write Pulse "Glitch" Protection

Noise pulses of less than 10 ns (typical) on $\overline{OE}$, $\overline{CE}$ or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IH}$. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

Power-up of the device with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

FUNCTIONAL DESCRIPTION

Description of User Modes

Table 1. Am28F256A User Bus Operations

Operation		$\overline{CE}$ ($\overline{E}$)	$\overline{OE}$ ($\overline{G}$)	$\overline{WE}$ ($\overline{W}$)	V_{PP} (Note 1)	A0	A9	I/O
Read-Only	Read	V_{IL}	V_{IL}	X	V_{PPL}	A0	A9	D_{OUT}
	Standby	V_{IH}	X	X	V_{PPL}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPL}	X	X	HIGH Z
	Auto-select Manufacturer Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IL}	V_{ID} (Note 3)	CODE (01H)
	Auto-select Device Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IH}	V_{ID} (Note 3)	CODE (2FH)
Read/Write	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	A0	A9	D_{OUT} (Note 4)
	Standby (Note 5)	V_{IH}	X	X	V_{PPH}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPH}	X	X	HIGH Z
	Write	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	A0	A9	D_{IN} (Note 6)

Legend:

X = Don't care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} \leq V_{CC} + 2$ V, See DC Characteristics for voltage levels of V_{PPH}, 0 V < An < V_{CC} + 2 V, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. *V_{PPL} may be grounded, connected with a resistor to ground, or $\leq V_{CC}$ +2.0 V. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.*
2. *Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 2.*
3. *$11.5 \leq V_{ID} \leq 13.0$ V*
4. *Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes.*
5. *With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).*
6. *Refer to Table 3 for valid D_{IN} during a write operation.*
7. *All inputs are Don't Care unless otherwise stated, where Don't Care is either V_{IL} or V_{IH} levels. In the Auto select mode all addresses except A9 and A0 must be held at V_{IL}.*

READ ONLY MODE

$V_{PP} < V_{CC} + 2$ V
Command Register Inactive

Read

The Am28F256A functions as a read only memory when $V_{PP} < V_{CC} + 2$ V. The Am28F256A has two control functions. Both must be satisfied in order to output data. $\overline{CE}$ controls power to the device. This pin should be used for specific device selection. $\overline{OE}$ controls the device outputs and should be used to gate data to the output pins if a device is selected.

Address access time t_{ACC} is equal to the delay from stable addresses to valid output data. The chip enable access time t_{CE} is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable at least $t_{ACC} - t_{OE}$).

Standby Mode

The Am28F256A has two standby modes. The CMOS standby mode ($\overline{CE}$ input held at $V_{CC} \pm 0.5$ V), consumes less than 100 µA of current. TTL standby mode ($\overline{CE}$ is held at V_{IH}) reduces the current requirements to less than 1 mA. When in the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure, programming, or program/erase verification, the device will draw active current until the operation is terminated.

Output Disable

Output from the device is disabled when $\overline{OE}$ is at a logic high level. When disabled, output pins are in a high impedance state.

Auto Select

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

The Auto select mode allows the reading out of a binary code from the device that will identify its manufacturer and type. This mode is intended for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

Programming In A PROM Programmer

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 13.0 V) on address A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL}, and V_{PP} must be less than or equal to $V_{CC} + 2.0$ V while using this Auto select mode. Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the Am28F256A these two bytes are given in the table below. All identifiers for manufacturer and device codes will exhibit odd parity with the MSB (DQ7) defined as the parity bit.

(Refer to the AUTO SELECT paragraph in the ERASE, PROGRAM, and READ MODE section for programming the Flash memory device in-system).

Table 2. Am28F256A Auto Select Code

Type	A0	Code (HEX)	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Manufacturer Code	V_{IL}	01	0	0	0	0	0	0	0	1
Device Code	V_{IH}	2F	0	0	1	0	1	1	1	1

ERASE, PROGRAM, AND READ MODE

V_{PP} = 12.0 V ± 5%

Command Register Active

Write Operations

High voltage must be applied to the V_{PP} pin in order to activate the command register. Data written to the register serves as input to the internal state machine. The output of the state machine determines the operational function of the device.

The command register does not occupy an addressable memory location. The register is a latch that stores the command, along with the address and data information needed to execute the command. The register is written by bringing $\overline{WE}$ and $\overline{CE}$ to V_{IL}, while $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$, while data is latched on the rising edge of the $\overline{WE}$ pulse. Standard microprocessor write timings are used.

The device requires the $\overline{OE}$ pin to be V_{IH} for write operations. This condition eliminates the possibility for bus contention during programming operations. In order to write, $\overline{OE}$ must be V_{IH}, and $\overline{CE}$ and $\overline{WE}$ must be V_{IL}. If any pin is not in the correct state a write command will not be executed.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Command Definitions

The contents of the command register default to 00H (Read Mode) in the absence of high voltage applied to the V_{PP} pin. The device operates as a read only memory. High voltage on the V_{PP} pin enables the command register. Device operations are selected by writing specific data codes into the command register. Table 3 defines these register commands.

Read Command

Memory contents can be accessed via the read command when V_{PP} is high. To read from the device, write 00H into the command register. Standard microprocessor read cycles access data from the memory. The device will remain in the read mode until the command register contents are altered.

The command register defaults to 00H (read mode) upon V_{PP} power-up. The 00H (Read Mode) register default helps ensure that inadvertent alteration of the memory contents does not occur during the V_{PP} power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Table 3. Am28F256A Command Definitions

	First Bus Cycle			Second Bus Cycle		
Command	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Note 4)	Write	X	00H/FFH	Read	RA	RD
Read Auto select	Write	X	80H or 90H	Read	00H/01H	01H/2FH
Embedded Erase Set-up/ Embedded Erase	Write	X	30H	Write	X	30H
Embedded Program Set-up/ Embedded Program	Write	X	10H or 50H	Write	PA	PD
Reset (Note 4)	Write	X	FFH	Write	X	FFH

Notes:

1. *Bus operations are defined in Table 1.*
2. *RA = Address of the memory location to be read.*
   PA = Address of the memory location to be programmed.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
   X = Don't care.
3. *RD = Data read from location RA during read operation.*
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$.
4. *Please reference Reset Command section.*

FLASH MEMORY PROGRAM/ERASE OPERATIONS

AMD's Embedded Program and Erase Operations

Embedded Erase Algorithm

The automatic chip erase does not require the device to be entirely pre-programmed prior to executing the Embedded set-up erase command and Embedded erase command. Upon executing the Embedded erase command the device automatically will program and verify the entire memory for an all zero data pattern. The system is not required to provide any controls or timing during these operations.

When the device is automatically verified to contain an all zero pattern, a self-timed chip erase and verify begin. The erase and verify operation are complete when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to Read mode. The system is not required to provide any control or timing during these operations.

When using the Embedded Erase algorithm, the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verify command is required). The margin voltages are internally generated in the same manner as when the standard erase verify command is used.

The Embedded Erase Set-Up command is a command only operation that stages the device for automatic electrical erasure of all bytes in the array. Embedded Erase Set-Up is performed by writing 30H to the command register.

To commence automatic chip erase, the command 30H must be written again to the command register. The automatic erase begins on the rising edge of the $\overline{WE}$ and terminates when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to Read mode.

Figure 5 and Table 4 illustrate the Embedded Erase algorithm, a typical command string and bus operation.

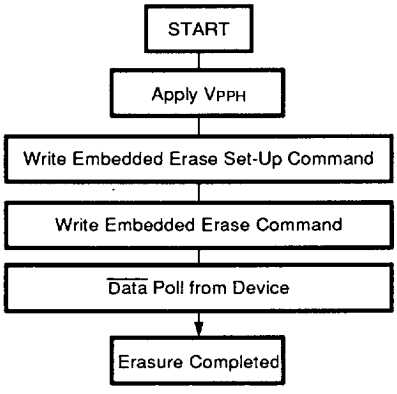


Figure 5. Embedded Erase Algorithm

Table 4. Embedded Erase Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} Ramp to V_{PPH} (1)
Write	Embedded Erase Set-Up Command	Data = 30H
Write	Embedded Erase Command	Data = 30H
Read		$\overline{\text{Data}}$ Polling to Verify Erasure
Standby		Compare Output to FFH
Read		Available for Read Operations

Note:

1. *See DC Characteristics for value of V_{PPL}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V. Refer to Functional Description.*

Embedded Programming Algorithm

The Embedded Program Set-Up is a command only operation that stages the device for automatic programming. Embedded Program Set-Up is performed by writing 10H or 50H to the command register.

Once the Embedded Set-Up Program operation is performed, the next $\overline{WE}$ pulse causes a transition to an active programming operation. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$ pulse, whichever happens later. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. The rising edge of $\overline{WE}$ also begins the programming operation. The system is not required to provide further controls or timings. The device will automatically provide an adequate internally generated program pulse and verify margin. The automatic programming operation is completed when the data on DQ7 is equivalent to data written to this bit (see Write Operation Status section) at which time the device returns to Read mode.

Figure 6 and Table 5 illustrate the Embedded Program algorithm, a typical command string, and bus operation.

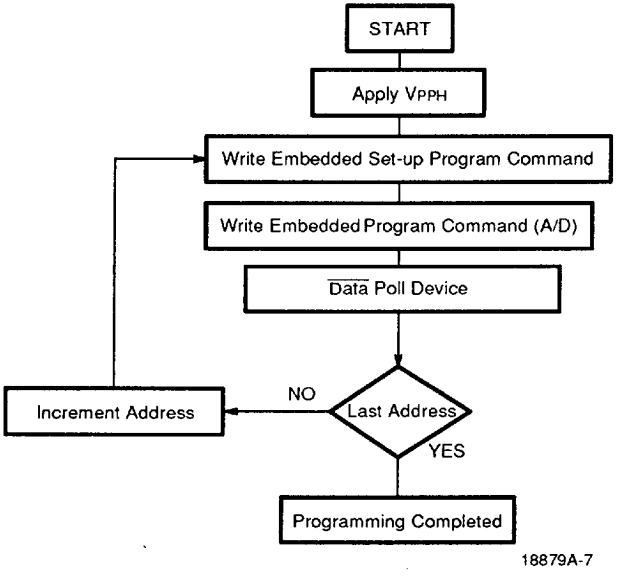


Figure 6. Embedded Programming Algorithm

Table 5. Embedded Programming Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} Ramp to V_{PPH} (1)
Write	Embedded Program Set-Up Command	Data = 10H or 50H
Write	Embedded Program Command	Valid Address/Data
Read		$\overline{\text{Data}}$ Polling to Verify Completion
Read		Available for Read Operations

Note:

1. *See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V. Refer to Functional Description. Device is either powered-down, erase inhibit or program inhibit.*

Write Operation Status

$\overline{\text{Data}}$ Polling—DQ7

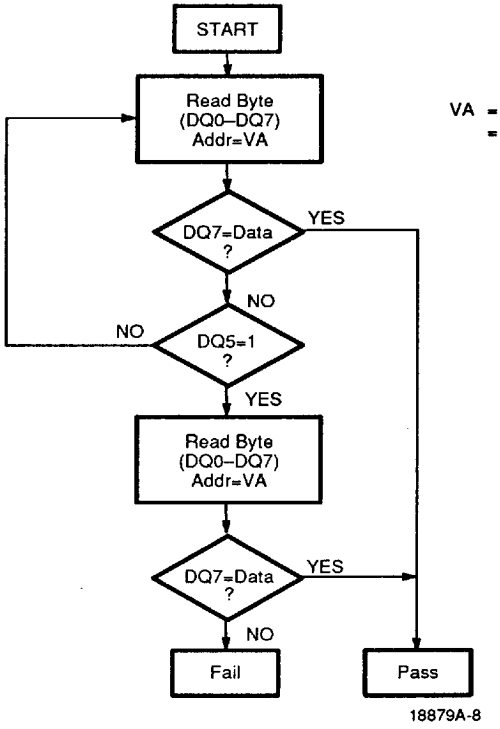
The Am28F256A features $\overline{\text{Data}}$ Polling as a method to indicate to the host system that the Embedded algorithms are either in progress or completed.

While the Embedded Programming algorithm is in operation, an attempt to read the device at a valid address will produce the complement of expected Valid data on DQ7. Upon completion of the Embedded Program algorithm an attempt to read the device at a valid address will produce Valid data on DQ7. The $\overline{\text{Data}}$ Polling feature is valid after the rising edge of the second $\overline{\text{WE}}$ pulse of the two write pulse sequence.

While the Embedded Erase algorithm is in operation, DQ7 will read "0" until the erase operation is completed. Upon completion of the erase operation, the data on DQ7 will read "1." The $\overline{\text{Data}}$ Polling feature is valid after the rising edge of the second $\overline{\text{WE}}$ pulse of the two Write pulse sequence.

The $\overline{\text{Data}}$ Polling feature is only active during Embedded Programming or erase algorithms.

See Figures 7a and 8a for the $\overline{\text{Data}}$ Polling timing specifications and diagrams. $\overline{\text{Data}}$ Polling is the standard method to check the write operation status, however, an alternative method is available using Toggle Bit.



Note:

1. DQ7 is rechecked even if DQ5="1" because DQ7 may change simultaneously with DQ5 or after DQ5.

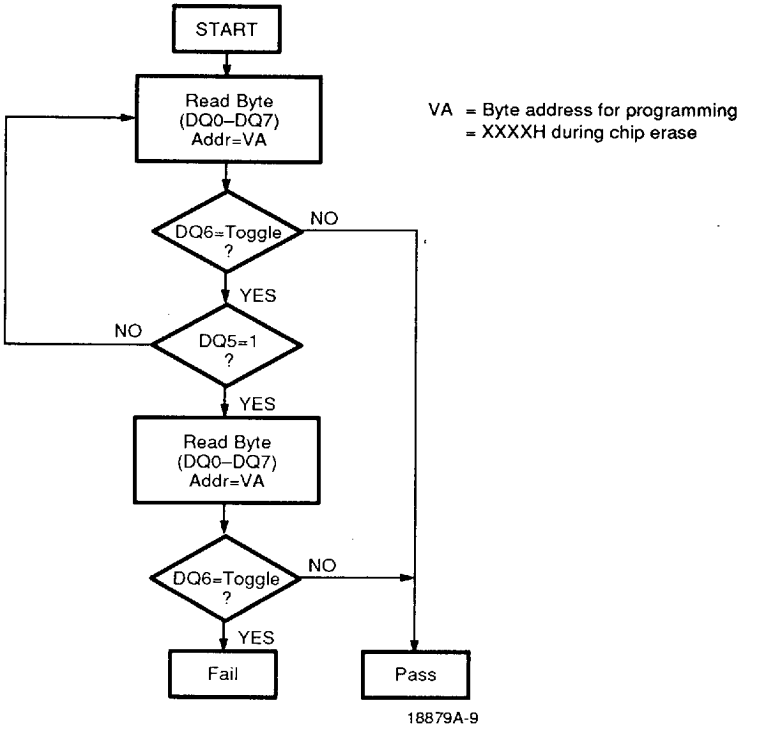
Figure 7a. $\overline{\text{Data}}$ Polling Algorithm

Toggle Bit—DQ6

The Am28F256A also features a "Toggle Bit" as a method to indicate to the host system that the Embedded algorithms are either in progress or completed.

Successive attempts to read data from the device at a valid address, while the Embedded Program algorithm is in progress, or at any address while the Embedded Erase algorithm is in progress, will result in DQ6 toggling between one and zero. Once the Embedded Program or Erase algorithm is completed, DQ6 will stop toggling to indicate the completion of either Embedded operation. Only on the next read cycle will valid data be obtained. The toggle bit is valid after the rising edge of the first $\overline{WE}$ pulse of the two write pulse sequence, unlike $\overline{Data}$ Polling which is valid after the rising edge of the second $\overline{WE}$ pulse. This feature allows the user to determine if the device is partially through the two write pulse sequence.

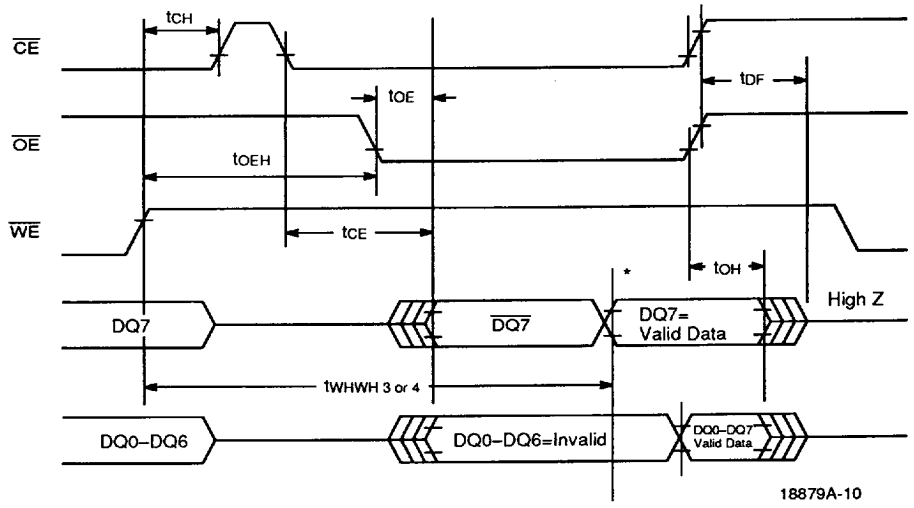
See Figures 7b and 8b for the Toggle Bit timing specifications and diagrams.



Note:

1. *DQ6 is rechecked even if DQ5="1" because DQ6 may stop toggling at the same time as DQ5 changing to "1".*

Figure 7b. Toggle Bit Algorithm



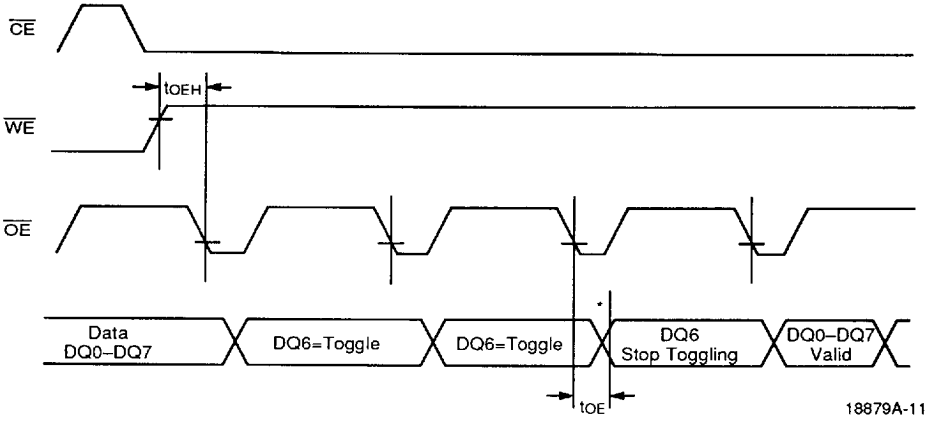
Note:
**DQ7=Valid Data (The device has completed the Embedded operation).*

Figure 8a. AC Waveforms for $\overline{\text{Data}}$ Polling During Embedded Algorithm Operations

DQ5

Exceeded Timing Limits

DQ5 will indicate if the program or erase time has exceeded the specified limits. This is a failure condition and the device may not be used again (internal pulse count exceeded). Under these conditions DQ5 will produce a "1." The program or erase cycle was not successfully completed. Data Polling is the only operating function of the device under this condition. The $\overline{CE}$ circuit will partially power down the device under these conditions (to approximately 2 mA). The $\overline{OE}$ and $\overline{WE}$ pins will control the output disable functions as described in Table 1.



Note:

**DQ6 stops toggling (The device has completed the Embedded operation).*

Figure 8b. AC Waveforms for Toggle Bit During Embedded Algorithm Operations

Parallel Device Erasure

The Embedded Erase algorithm greatly simplifies parallel device erasure. Since the erase process is internal to the device, a single erase command can be given to multiple devices concurrently. By implementing a parallel erase algorithm, total erase time may be minimized.

Note that the Flash memories may erase at different rates. If this is the case, when a device is completely erased, use a masking code to prevent further erasure (over-erasure). The other devices will continue to erase until verified. The masking code applied could be the read command (00H).

Power-Up Sequence

The Am28F256A powers-up in the Read only mode. Power supply sequencing is not required.

Reset Command

The Reset command initializes the Flash memory device to the Read mode. In addition, it also provides the user with a safe method to abort any device operation (including program or erase).

The Reset must be written two consecutive times after the Set-up Program command (10H or 50H). This will reset the device to the Read mode.

Following any other Flash command, write the Reset command once to the device. This will safely abort any previous operation and initialize the device to the Read mode.

The Set-up Program command (10H or 50H) is the only command that requires a two-sequence reset cycle. The first Reset command is interpreted as program data. However, FFH data is considered as null data during programming operations (memory cells are only programmed from a logical "1" to "0"). The second Reset command safely aborts the programming operation and resets the device to the Read mode.

Memory contents are not altered in any case.

This detailed information is for your reference. It may prove easier to always issue the Reset command two consecutive times. This eliminates the need to determine if you are in the Set-up Program state or not.

In-System Programming Considerations

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the circuit board.

Auto Select Command

AMD's Flash memories are designed for use in applications where the local CPU alters memory contents. In order to correctly program any Flash memories in-system, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not a generally desired system design practice.

The Am28F256A contains an Auto Select operation to supplement traditional PROM programming methodologies. The operation is initiated by writing 80H or 90H into the command register. Following this command, a read cycle address 0000H retrieves the manufacturer code of 01H (AMD). A read cycle from address 0001H returns the device code 2FH (see Table 2). To terminate the operation, it is necessary to write another valid command, such as Reset (FFH), into the register.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Ceramic Packages ..... −65°C to +150°C
Plastic Packages ..... −65°C to +125°C

Ambient Temperature
with Power Applied ..... −55°C to + 125°C

Voltage with Respect To Ground
All pins except A9 and V_{PP}
(Note 1) ..... −2.0 V to +7.0 V

V_{CC} (Note 1) ..... −2.0 V to +7.0 V

A9 (Note 2) ..... −2.0 V to +14.0 V

V_{PP} (Note 2) ..... −2.0 V to +14.0 V

Output Short Circuit Current (Note 3) ..... 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is −0.5 V. During voltage transitions, inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *Minimum DC input voltage on A9 and V_{PP} pins is −0.5 V. During voltage transitions, A9 and V_{PP} may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC input voltage on A9 and V_{PP} is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.*
3. *No more than one output shorted at a time. Duration of the short circuit should not be greater than one second*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Case Temperature (Tc) ..... 0°C to +70°C

Industrial (I) Devices
Case Temperature (Tc) ..... −40°C to +85°C

Extended (E) Devices
Case Temperature (Tc) ..... −55°C to +125°C

Military (M) Devices
Case Temperature (Tc) ..... −55°C to +125°C

V_{CC} Supply Voltages
V_{CC} for Am28F256A–X5 ..... +4.75 V to +5.25 V

V_{CC} for Am28F256A–XX0 ..... +4.50 V to +5.50 V

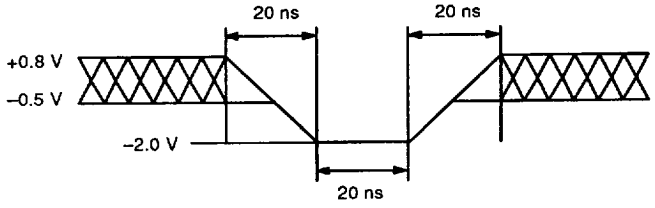
V_{PP} Supply Voltages
Read ..... −0.5 V to +12.6 V

Program, Erase, and Verify ..... +11.4 V to +12.6 V

Operating ranges define those limits between which the funtionality of the device is guaranteed.

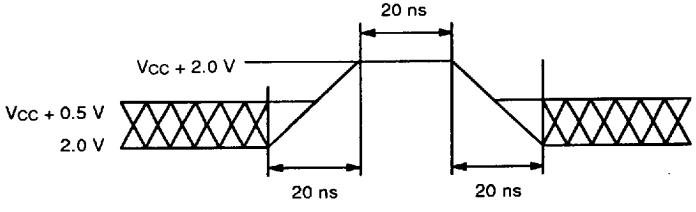
MAXIMUM OVERSHOOT

Maximum Negative Input Overshoot



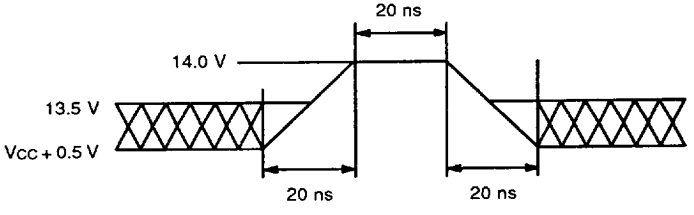
18879A-12

Maximum Positive Input Overshoot



18879A-13

Maximum V_{PP} Overshoot



18879A-14

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1–4)

DC CHARACTERISTICS-TTL/NMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max, V_{IN} = V_{CC} or V_{SS}			±1.0	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max, V_{OUT} = V_{CC} or V_{SS}			±1.0	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max $\overline{CE}$ = V_{IH}		0.2	1.0	mA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max, $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH} I_{OUT} = 0 mA, at 6 MHz		10	30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE}$ = V_{IL} Programming in Progress (Note 4)		10	30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE}$ = V_{IL} Erasure in Progress (Note 4)		10	30	mA
I_{PPS}	V_{PP} Standby Current	V_{PP} = V_{PPL}			±1.0	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{PPH}		70	200	µA
		V_{PP} = V_{PPL}			±1.0	
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPH} Programming in Progress (Note 4)		10	30	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress (Note 4)		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA V_{CC} = V_{CC} Min			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA V_{CC} = V_{CC} Min	2.4			V
V_{ID}	A9 Auto Select Voltage	A9 = V_{ID}	11.5		13.0	V
I_{ID}	A9 Auto Select Current	A9 = V_{ID} Max V_{CC} = V_{CC} Max		5	50	µA
V_{PPL}	V_{PP} during Read-Only Operations	***Note:*** *Erase/Program are inhibited when* V_{PP} = V_{PPL}	0.0		V_{CC} +2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2			V

Notes:

1. ***Caution:*** *the Am28F256A must not be removed from (or inserted into) a socket when* V_{CC} *or* V_{PP} *is applied.*
2. I_{CC1} *is tested with* $\overline{OE}$ = V_{IH} *to simulate open outputs.*
3. *Maximum active power usage is the sum of* I_{CC} *and* I_{PP}.
4. *Not 100% tested.*

DC CHARACTERISTICS—CMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max, V_{IN} = V_{CC} or V_{SS}			± 1.0	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max, V_{OUT} = V_{CC} or V_{SS}			± 1.0	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max $\overline{CE}$ = V_{CC} + 0.5 V		15	100	µA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max, $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH} I_{OUT} = 0 mA, at 6 MHz		10	30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE}$ = V_{IL} Programming in Progress (Note 4)		10	30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE}$ = V_{IL} Erasure in Progress (Note 4)		10	30	mA
I_{PPS}	V_{PP} Standby Current	V_{PP} = V_{PPL}			± 1.0	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{PPH}		70	200	µA
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPH} Programming in Progress (Note 4)		10	30	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress (Note 4)		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		0.7 V_{CC}		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA V_{CC} = V_{CC} Min			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA, V_{CC} = V_{CC} Min	0.85 V_{CC}			V
V_{OH2}		I_{OH} = –100 µA, V_{CC} = V_{CC} Min	V_{CC} –0.4			
V_{ID}	A9 Auto Select Voltage	A9 = V_{ID}	11.5		13.0	V
I_{ID}	A9 Auto Select Current	A9 = V_{ID} Max V_{CC} = V_{CC} Max		5	50	µA
V_{PPL}	V_{PP} during Read-Only Operations	***Note:*** *Erase/Program are inhibited when* V_{PP} = V_{PPL}	0.0		V_{CC} + 2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2			V

Notes:

1. ***Caution:*** *the Am28F256A must not be removed from (or inserted into) a socket when* V_{CC} *or* V_{PP} *is applied.*
2. I_{CC1} *is tested with* $\overline{OE}$ = V_{IH} *to simulate open outputs.*
3. *Maximum active power usage is the sum of* I_{CC} *and* I_{PP}.
4. *Not 100% tested.*

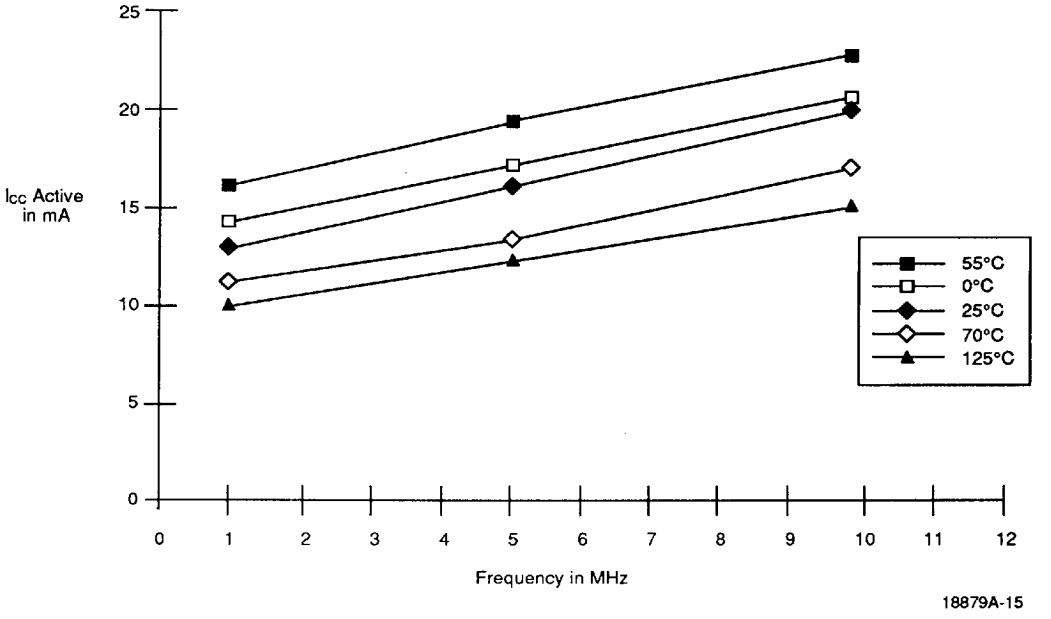


Figure 9. Am28F256A – Average I_{CC} Active vs. Frequency
V_{CC} = 5.5 V, Addressing Pattern = Minmax
Data Pattern = Checkerboard

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	8	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	12	pF
C_{IN2}	V_{PP} Input Capacitance	V_{PP} = 0	8	12	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz*

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

AC CHARACTERISTICS—Read Only Operation (Notes 1–4)

Parameter Symbols				Am28F256A						Unit
JEDEC	Standard	Parameter Description		— -75	-90 -95	-120 —	-150 —	-200 —	-250 —	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 4)	Min Max	70	90	120	150	200	250	ns
t_{ELQV}	t_{CE}	Chip Enable Access Time	Min Max	70	90	120	150	200	250	ns
t_{AVQV}	t_{ACC}	Address Access Time	Min Max	70	90	120	150	200	250	ns
t_{GLOV}	t_{OE}	Output Enable Access Time	Min Max	35	35	50	55	55	55	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low Z (Note 4)	Min Max	0	0	0	0	0	0	ns
t_{EHQZ}	t_{DF}	Chip Disable to Output in High Z (Note 3)	Min Max	20	20	30	35	35	35	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z (Note 4)	Min Max	0	0	0	0	0	0	ns
t_{GHQZ}	t_{DF}	Output Disable to Output in High Z (Note 4)	Min Max	20	20	30	35	35	35	ns
t_{AXQX}	t_{OH}	Output Hold from first of Address, $\overline{CE}$, or $\overline{OE}$ Change (Note 4)	Min Max	0	0	0	0	0	0	ns
t_{WHGL}		Write Recovery Time before Read	Min Max	6	6	6	6	6	6	µs
t_{VCS}		V_{CC} Set-up Time to Valid Read (Note 4)	Min Max	50	50	50	50	50	50	µs

Notes:

1. *Output Load: 1 TTL gate and C_L = 100 pF*
   Input Rise and Fall Times: ≤ 10 ns
   Input Pulse levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V
2. *The Am28F256A-75 and Am28F256A-95 Output Load: 1 TTL gate and C_L = 100 pF*
   Input Rise and Fall Times: ≤ 10 ns
   Input Pulse levels: 0 V to 3 V
   Timing Measurement Reference Level: 1.5 V inputs and outputs.
3. *Guaranteed by design not tested.*
4. *Not 100% tested.*

AC CHARACTERISTICS—Write/Erase/Program Operations (Notes 1–6)

Parameter Symbols				Am28F256A						
JEDEC	Standard	Parameter Description		— -75	-90 -95	-120 —	-150 —	-200 —	-250 —	Unit
tAVAV	tWC	Write Cycle Time (Note 6)	Min Max	70	90	120	150	200	250	ns
tAVWL	tAS	Address Set-Up Time	Min Max	0	0	0	0	0	0	ns
tWLAX	tAH	Address Hold Time	Min Max	45	45	50	60	75	75	ns
tDVWH	tDS	Data Set-Up Time	Min Max	45	45	50	50	50	50	ns
tWHDX	tDH	Data Hold Time	Min Max	10	10	10	10	10	10	ns
tOEH		Output Enable Hold Time for Embedded Algorithm only (See Figure 8)	Min Max	10	10	10	10	10	10	ns
tGHWL		Read Recovery Time before Write	Min Max	0	0	0	0	0	0	µs
tELWLE	tCSE	Chip Enable Embedded Algorithm Setup Time	Min Max	20	20	20	20	20	20	ns
tWHEH	tCH	Chip Enable Hold Time	Min Max	0	0	0	0	0	0	ns
tWLWH	tWP	Write Pulse Width	Min Max	45	45	50	60	60	60	ns
tWHWL	tWPH	Write Pulse Width HIGH	Min Max	20	20	20	20	20	20	ns
tWHWH3		Embedded Programming Operation (Note 4)	Min Max	14	14	14	14	14	14	µs
tWHWH4		Embedded Erase Operation (Note 5)	Typ Max	3	5	5	5	5	5	s
tVPEL		V_{PP} Set-Up Time to Chip Enable LOW (Note 6)	Min Max	100	100	100	100	100	100	ns
tVCS		V_{CC} Set-Up Time to Chip Enable LOW (Note 6)	Min Max	50	50	50	50	50	50	µs
tVPPR		V_{PP} Rise Time 90% V_{PPH} (Note 6)	Min Max	500	500	500	500	500	500	ns
tVPPF		V_{PP} Fall Time 90% V_{PPL} (Note 6)	Min Max	500	500	500	500	500	500	ns
tLKO		$V_{CC} < V_{LKO}$ to Reset (Note 6)	Min Max	100	100	100	100	100	100	ns

Notes:

1. *Read timing characteristics during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read Only operations.*
2. *All devices except Am28F256A-75 and Am28F256A-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.45 V t o 2.4 V. Timing Measurement Reference Level: Inputs: 0.8 V and 2.0 V; Outputs: 0.8 V and 2.0 V*
3. *Am28F256A-75 and Am28F256A-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.0 V to 3.0 V Timing Measurement Reference Level: Inputs and Outputs: 1.5 V*
4. *Embedded Program Operation of 14 µs consists of 10 µs program pulse and 4 µs write recovery before read. This is the minimum time for one pass through the programming algorithm.*
5. *Embedded erase operation of 5 sec consists of 4 sec array pre-programming time and one sec array erase time. This is a typical time for one embedded erase operation.*
6. *Not 100% tested.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS

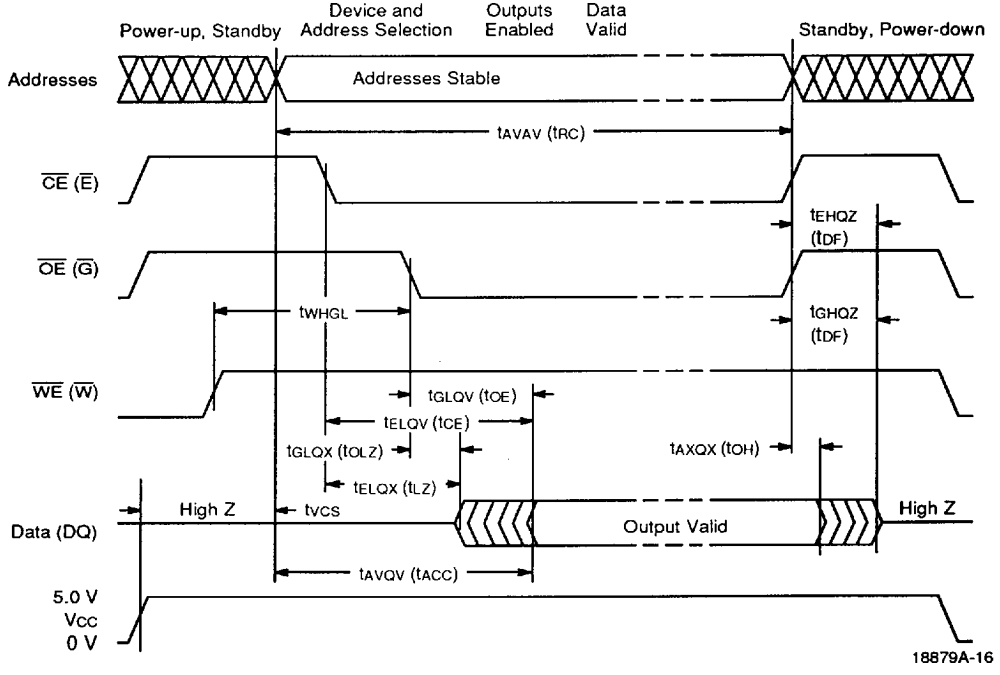
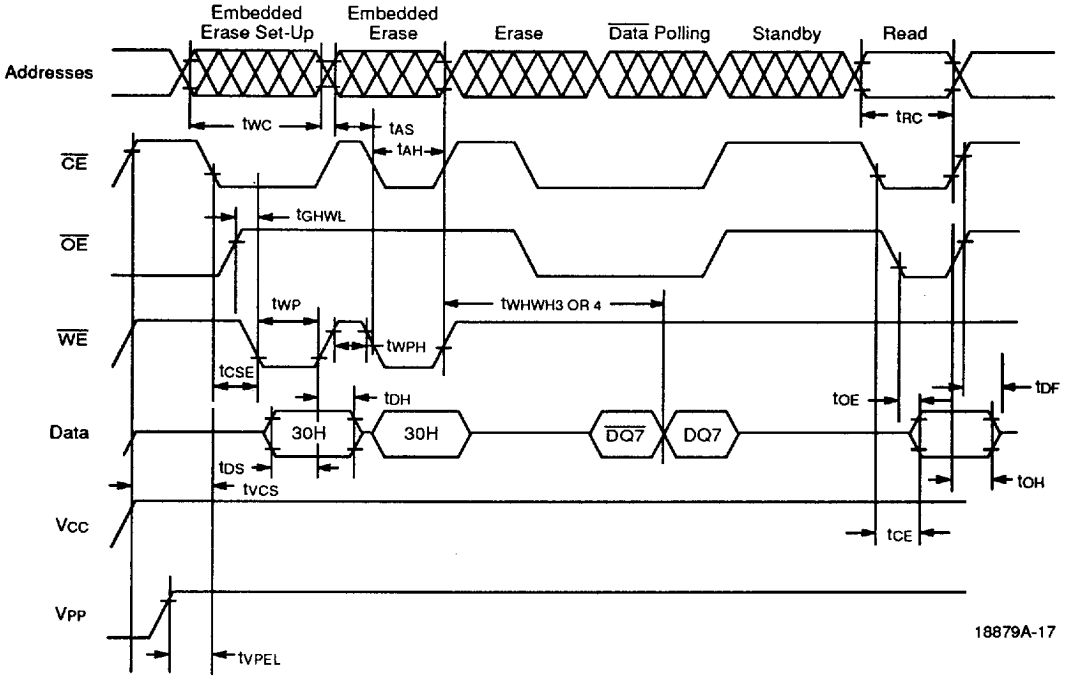


Figure 10. AC Waveforms for Read Operations

SWITCHING WAVEFORMS

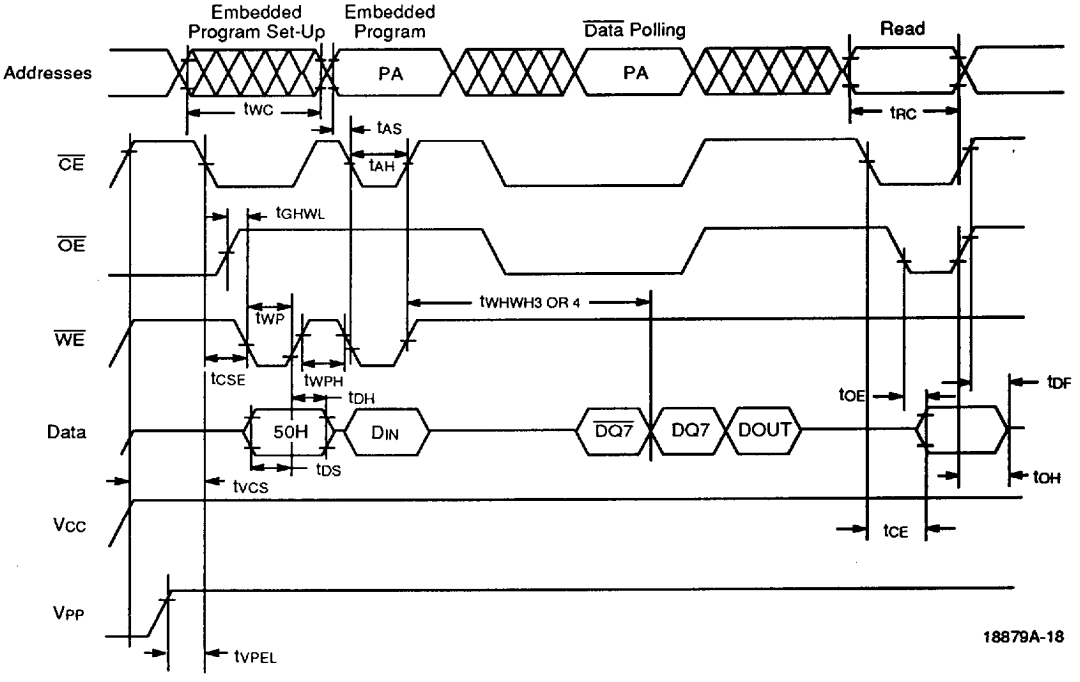


Note:

1. $\overline{DQ7}$ is the output of the complement of the data written to the device.

Figure 11. AC Waveforms for Embedded Erase Operation

SWITCHING WAVEFORMS



Notes:

1. *D_{IN} is data input to the device.*
2. *$\overline{DQ7}$ is the output of the complement of the data written to the device.*
3. *D_{OUT} is the output of the data written to the device.*

Figure 12. AC Waveforms for Embedded Programming Operation

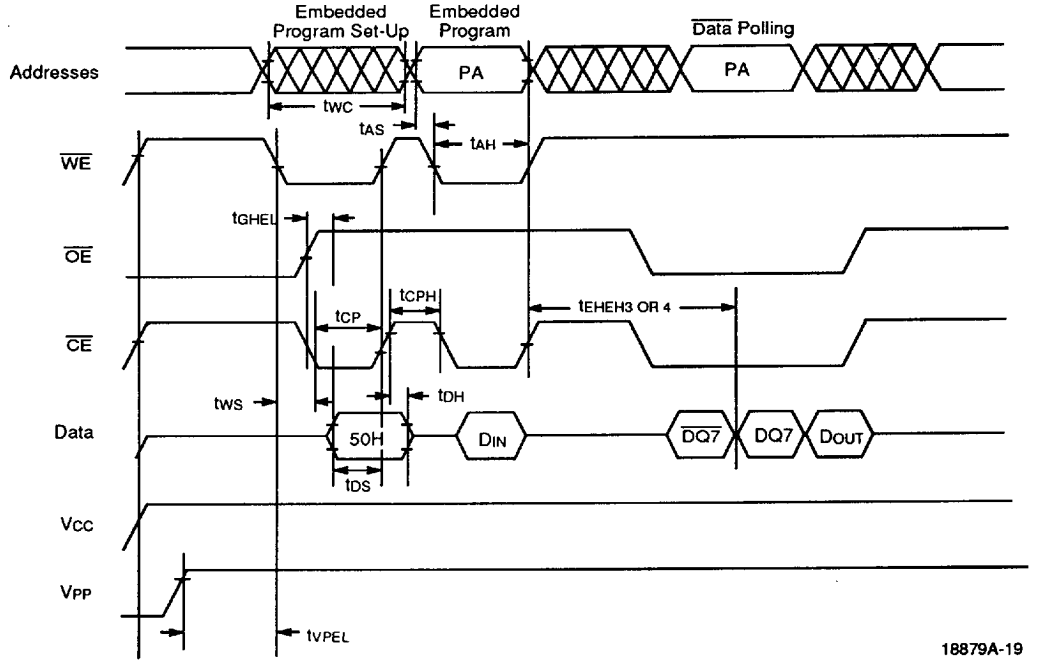
AC CHARACTERISTICS—Write/Erase/Program Operations (Notes 1– 6)
Alternate $\overline{CE}$ Controlled Writes

Parameter Symbols				Am28F256A						Unit
JEDEC	Standard	Parameter Description		— -75	-90 -95	-120 —	-150 —	-200 —	-250 —	
tAVAV	tWC	Write Cycle Time (Note 6)	Min Max	70	90	120	150	200	250	ns
tAVEL	tAS	Address Set-Up Time	Min Max	0	0	0	0	0	0	ns
tELAX	tAH	Address Hold Time	Min Max	45	45	50	60	75	75	ns
tDVEH	tDS	Data Set-Up Time	Min Max	45	45	50	50	50	50	ns
tEHDX	tDH	Data Hold Time	Min Max	10	10	10	10	10	10	ns
tOEH		Output Enable Hold Time for Embedded Algorithm only (See Figure 8)	Min Max	10	10	10	10	10	10	ns
tGHEL		Read Recovery Time Before Write	Min Max	0	0	0	0	0	0	µs
tWLEL	tWS	WE Set-Up Time by $\overline{CE}$	Min Max	0	0	0	0	0	0	ns
tEHWK	tWH	WE Hold Time	Min Max	0	0	0	0	0	0	ns
tELEH	tCP	Write Pulse Width	Min Max	65	65	70	80	80	80	ns
tEHEL	tCPH	Write Pulse Width HIGH	Min Max	20	20	20	20	20	20	ns
tEHEH3		Embedded Programming Operation (Note 4)	Min Max	14	14	14	14	14	14	µs
tEHEH4		Embedded Erase Operation (Note 5)	Min Max	3	3	3	3	3	3	s
tVPEL		VPP Set-Up Time to Chip Enable LOW (Note 6)	Min Max	100	100	100	100	100	100	ns
tVCS		VCC Set-Up Time to Chip Enable LOW (Note 6)	Min Max	50	50	50	50	50	50	µs
tVPPR		VPP Rise Time 90% VPPH (Note 6)	Min Max	500	500	500	500	500	500	ns
tVPPF		VPP Fall Time 90% VPPL (Note 6)	Min Max	500	500	500	500	500	500	ns
tLKO		VCC < VLKO to Reset (Note 6)	Min Max	100	100	100	100	100	100	ns

Notes:

1. *Read timing characteristics during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read Only operations.*
2. *All devices except Am28F256A-75 and Am28F256A-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.45 V to 2.4 V. Timing Measurement Reference Level: Inputs: 0.8 V and 2.0 V; Outputs: 0.8 V and 2.0 V*
3. *Am28F256A-75 and Am28F256A-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.0 V to 3.0 V Timing Measurement Reference Level: Inputs and Outputs: 1.5 V*
4. *Embedded Program Operation of 14 µs consists of 10 µs program pulse and 4 µs write recovery before read. This is the minimum time for one pass through the programming algorithm.*
5. *Embedded erase operation of 5 sec consists of 4 sec array pre-programming time and one sec array erase time. This is a typical time for one embedded erase operation.*
6. *Not 100% tested.*

SWITCHING WAVEFORMS

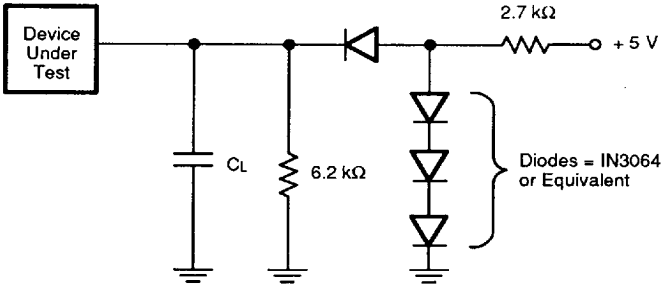


Notes:

1. *D_{IN} is data input to the device.*
2. *$\overline{DQ7}$ is the output of the complement of the data written to the device.*
3. *D_{OUT} is the output of the data written to the device.*

Figure 13. AC Waveforms for Embedded Programming Operation Using $\overline{CE}$ Controlled Writes

SWITCHING TEST CIRCUIT



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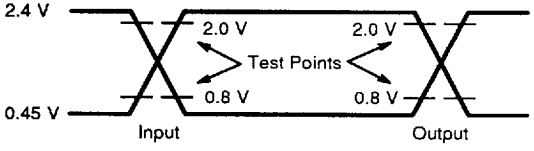
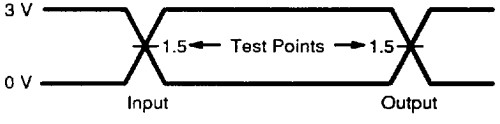
C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORMS



All Devices Except Am28F256A-75 and Am28F256A-95

AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are < 10 ns.



For Am28F256A-75 and Am28F256A-95

AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are < 10 ns.

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ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min	Typ	Max (Note 3)		
Chip Erase Time		1 (Note 1)	10 (Note 2)	s	Excludes 00H programming prior to erasure
Chip Programming Time		0.5 (Note 1)	4	s	Excludes system-level overhead
Write/Erase Cycles	100,000			Cycles	
Byte Program Time		14		µs	
			96 (Note 4)	ms	

Notes:

1. *25°C, 12 V V_{PP}*
2. *The Embedded algorithm allows for 60 second erase time for military temperature range operations.*
3. *Maximum time specified is lower than worst case. Worst case is derived from the Embedded Algorithm internal counter which allows for a maximum 6000 pulses for both program and erase operations. Typical worst case for program and erase is significantly less than the actual device limit.*
4. *Typical worst case = 84 µs. DQ5 = "1" only after a byte takes longer than 96 ms to program.*

LATCHUP CHARACTERISTICS

	Min	Max
Input Voltage with respect to V_{SS} on all pins except I/O pins (Including A9 and V_{PP})	−1.0 V	13.5 V
Input Voltage with respect to V_{SS} on all pins I/O pins	−1.0 V	V_{CC} + 1.0 V
Current	−100 mA	+100 mA
Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.		

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years