Z89165/167/169 AND Z89166/168 (ROMLESS)

ENHANCED DUAL-PROCESSOR DTAD CONTROLLERS

FEATURES

Part Number	Z8 ROM (KBytes)	Z8 RAM* (KBytes)	Speed (MHz)
Z89165	24	236	20
Z89166	ROMless	236	20
Z89167	24	236	24
Z89168	ROMless	236	24
Z89169	32	236	24

  *General-Purpose

Part Number	DSP ROM (Words)	DSP RAM (Words)	Speed (MHz)
Z89165	6K	512	20
Z89166	6K	512	20
Z89167	8K	512	24
Z89168	8K	512	24
Z89169	8K	512	24

- 68- and 84-Pin PLCC Packages
- 4.5- to 5.5-Volt Operating Range
- Low-Power Consumption (200 mW Typical)
- 0°C to +70°C Temperature Range
- 25 Expanded Register Files
- 47 Input/Output Lines (Z89165)
  31 Input/Output Lines (Z89166)
  43 Input/Output Lines (Core Processor)
- Six Vectored, Prioritized Z8 Interrupts with Programmable Polarity
- Three Vectored, Prioritized DSP Interrupts with Programmable Polarity
- Two Analog Comparators
- Two Programmable Z8 8-Bit Counter/Timers, Each with Two 6-Bit Programmable Prescaler
- Watch-Dog Timer /Power-On Reset
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive
- RAM and ROM Protect, Low-EMI Option

GENERAL DESCRIPTION

Zilog's Digital Voice Processor Controller family combines a Z8® microcontroller and a DSP processor on-chip for a cost-effective turnkey system in digital telephone answering devices and other voice processing applications.

The dual-processor architecture is loosely coupled by mailbox registers and an interrupt system, enabling DSP or Z8 programs to be directed by events in each other's domain.

The Z8 microcontroller uses an expanded register file to allow access to register-mapped peripheral and I/O circuits for programming versatility.

The 16-bit DSP processor features a 24-bit ALU and accumulator with single-cycle instructions, providing the algorithm processing power necessary for telephone voice quality.

The Z89165/166 devices offer a half-flash 8-bit A/D converter with up to 128 kHz sample rate and a 10-bit Pulse-Width modulator (PWM) D/A converter, eliminating the need for an external CODEC.

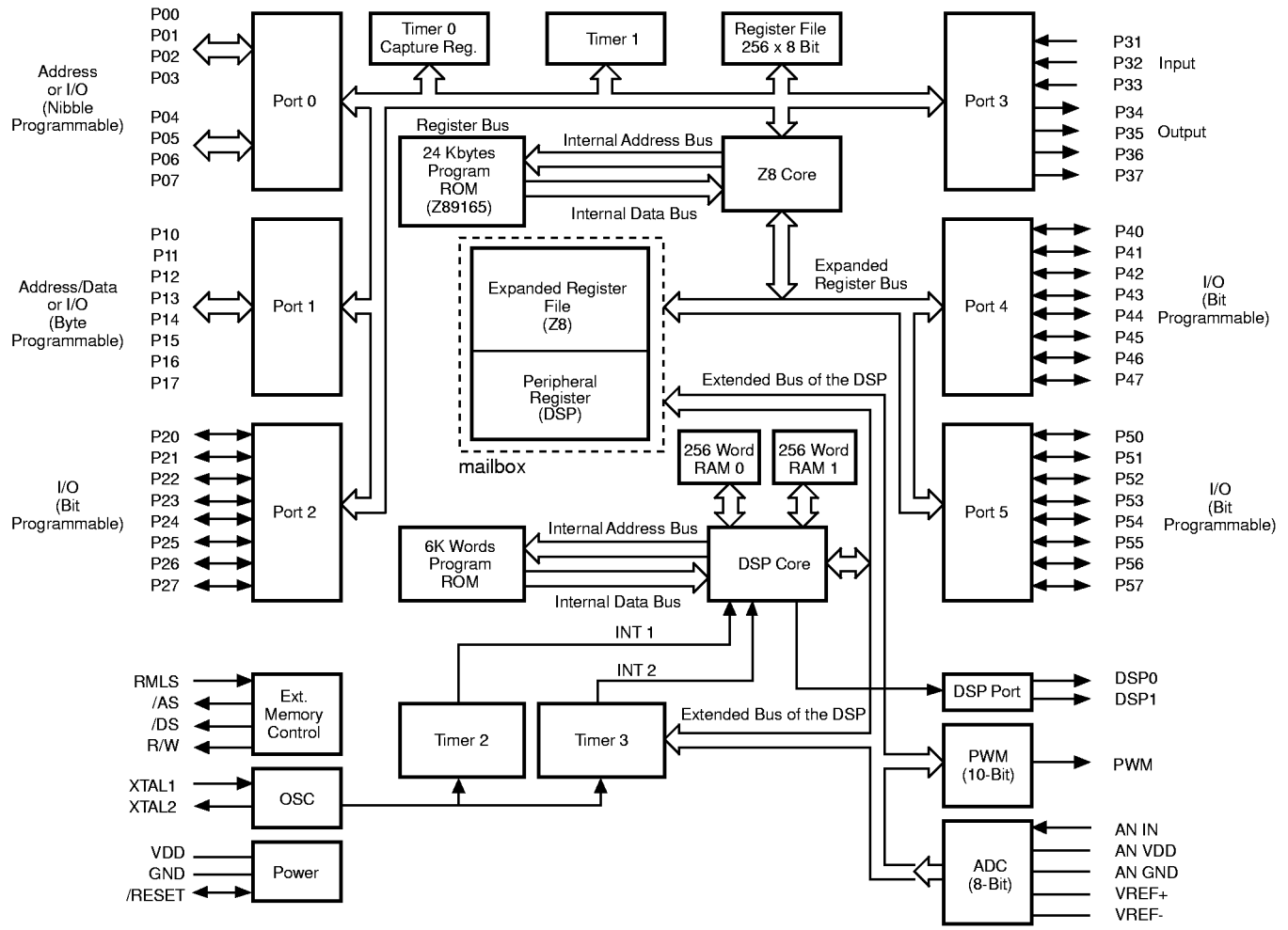
The Z89167/168/169 devices feature a hardware ARAM interface, as well as a dual-CODEC interface. A 10-bit PWM D/A converter is also on-chip.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

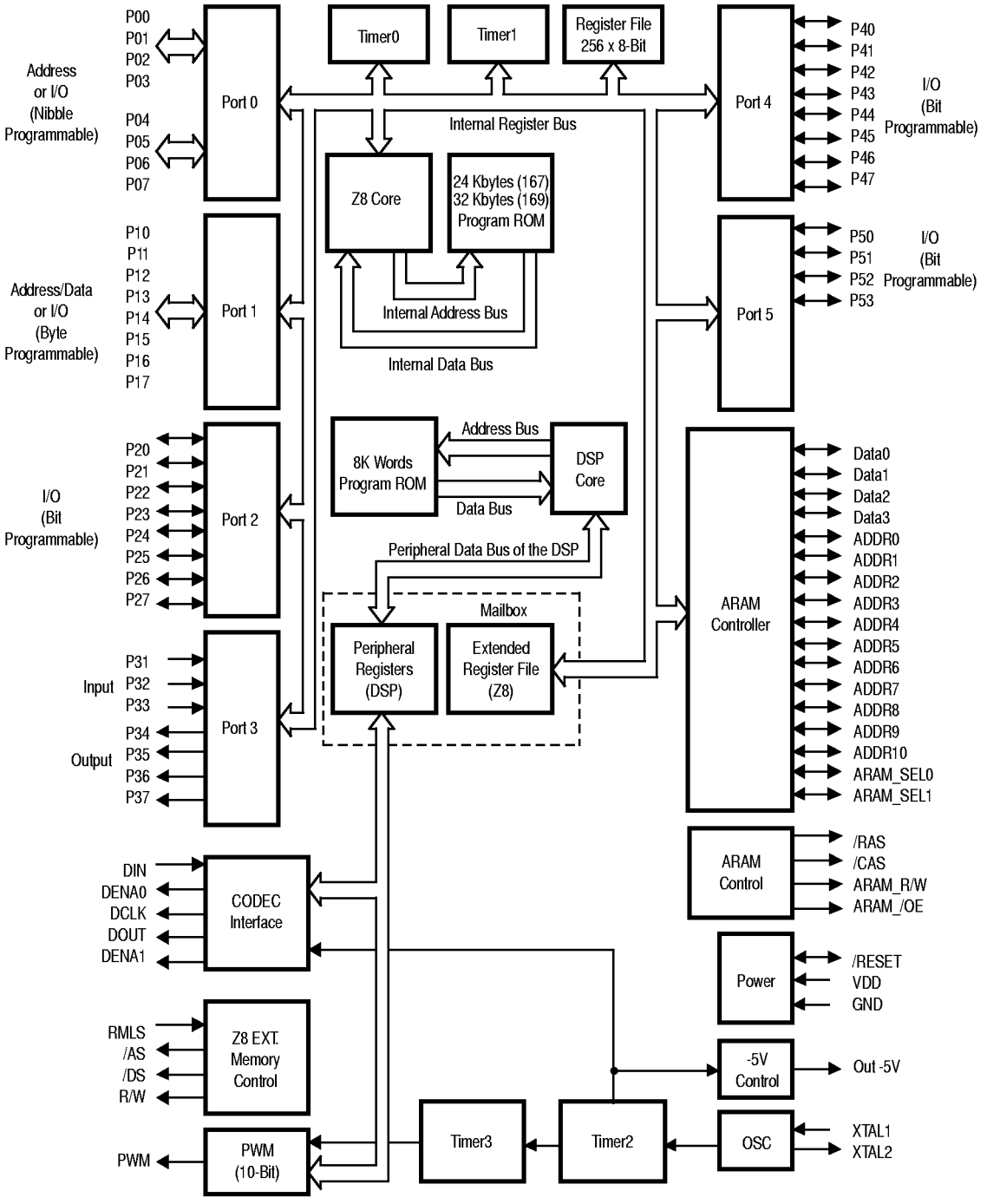
Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)



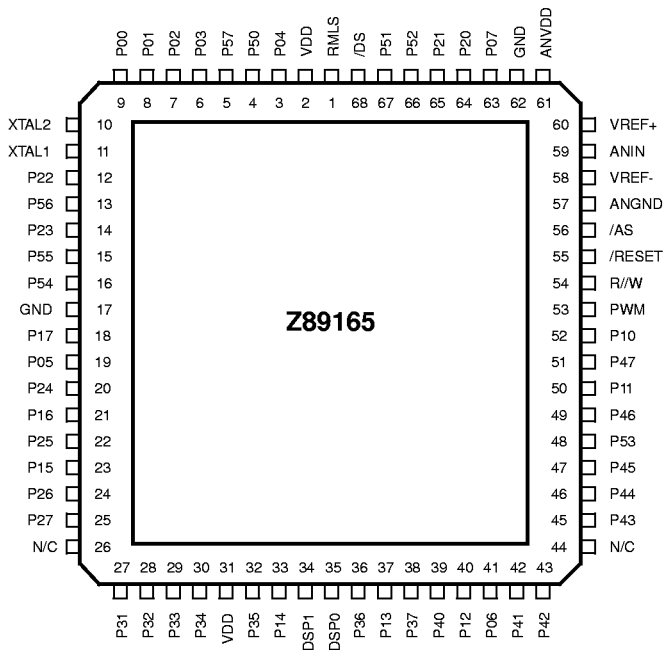
Z89165/166 Functional Block Diagram

GENERAL DESCRIPTION (Continued)

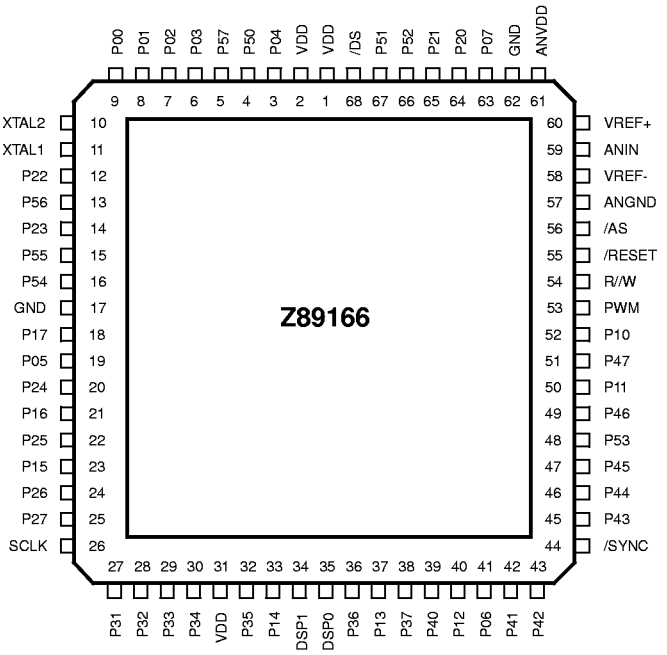


Z89167/168/169 Functional Block Diagram

PIN DESCRIPTION



Z89165 68-Pin PLCC Pin Identification



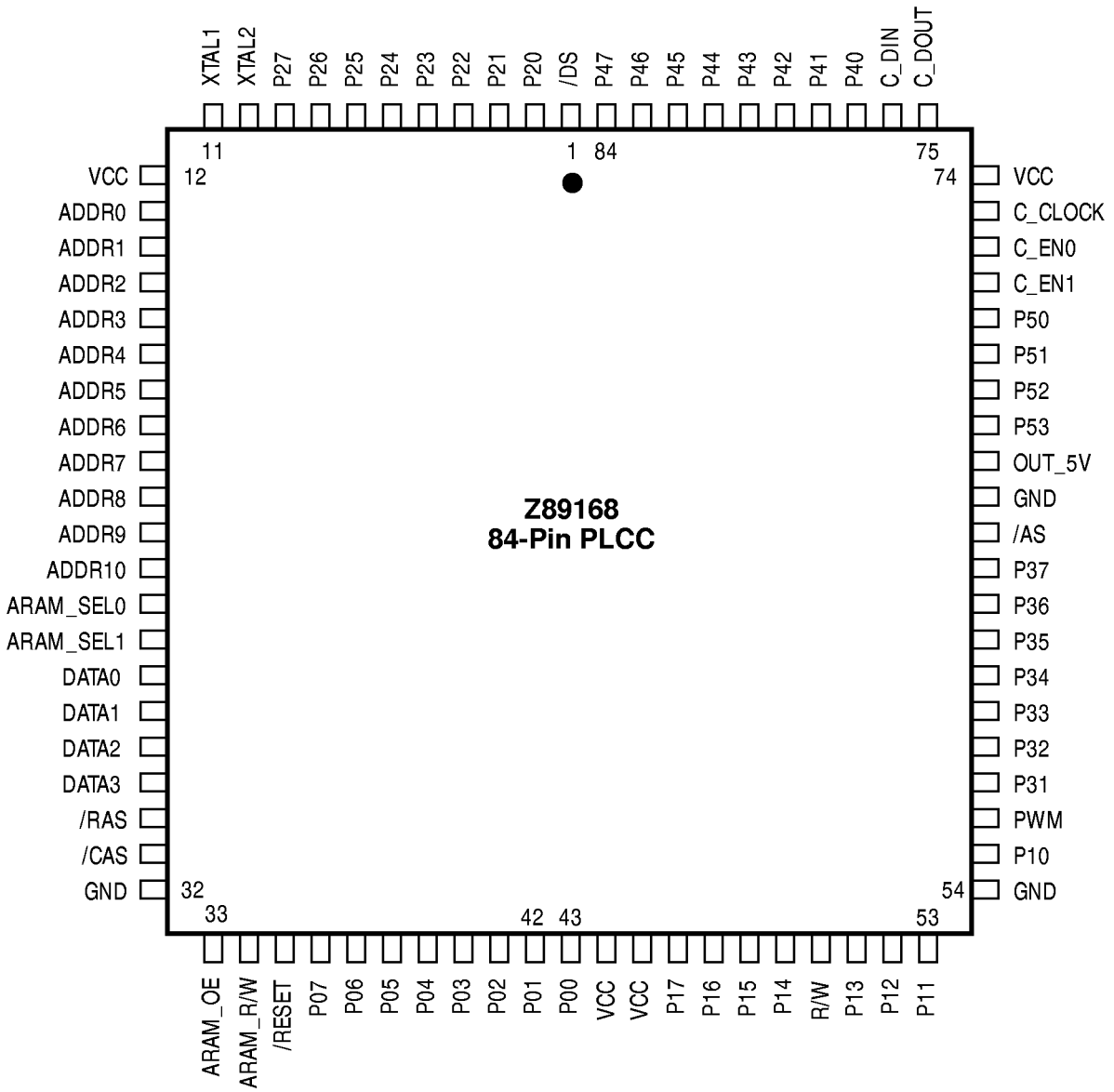
Z89166 68-Pin PLCC Pin Identification

Pin Identification

Pin Name	Function	Direction
+5V	Power	5V Power Input (Digital Power)
GND	Power	Device Ground (Digital Ground)
AN	AIN	8-Bit A to D Converter Input
Vref–	AIN	Low Reference Level for A to D Converter
Vref+	AIN	High Reference Level for A to D Converter
AN VDD	Power	ADC +5V Power (Analog Power)
AN GND	Power	ADC Ground (Analog Ground)
P00-P07 Data	I/O	General-Purpose I/O Port
P10-P17 Data	I/O	General-Purpose I/O Port
P20-P27 Data	I/O	General-Purpose I/O Port

Pin Name	Function	Direction
P31-P37 Data	I/O	General-Purpose I/O Port
P40-P47 Data	I/O	General-Purpose I/O Port
P50-P57 Data	I/O	General-Purpose I/O Port
DSP0-DSP1 Data	0	General-Purpose 0 Port
XTAL1	OSC1	20.48 MHz Crystal Oscillator Input
XTAL2	OSC2	20.48 MHz Crystal Oscillator Input
/RESET	I/O	System RESET
PWM	Out	10-Bit PWM, 5V TTL Output

PIN DESCRIPTION (Continued)



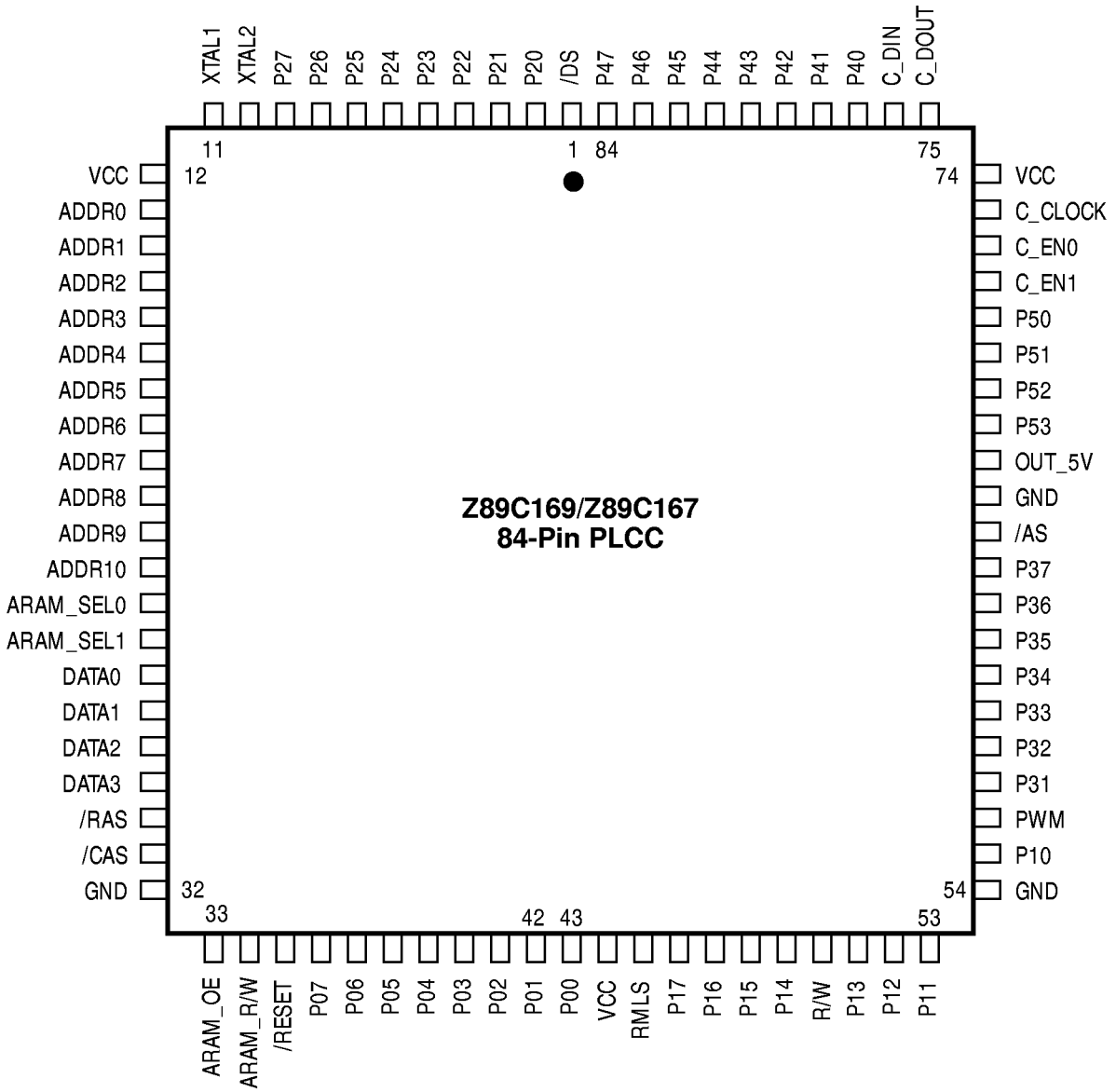
Z89168 84-Pin PLCC Pin Identification

PIN DESCRIPTION (Continued)

Z89168 84-Pin PLCC Pin Identification

I/O Port Functions	Pin Number	I/O	Function
V_{SS}	32, 54, 65		Digital Ground
V_{CC}	12, 44, 74, 45		Digital VCC = +5 V
P00-P07	43-36	Input/Output	P00-P07 (General-purpose nibble programmable I/O port.)
P10-P17	55, 53-51, 49-46	Input/Output	P10-P17 (General-purpose byte programmable I/O port.)
P20-P27	2-9	Input/Output	P20-P27 (General-purpose bit programmable I/O.)
P31-P37	57-63	Input/Output	P31-P37 (General-purpose I/O port. Bits P31-P33 are inputs, while bits P34-P37 are outputs.)
P40-P47	77-84	Input/Output	P40-P47 (General-purpose bit programmable I/O.)
P50-P53	70-67	Input/Output	P50-P53 (General-purpose bit programmable I/O.)
C_DIN	76	Input	Data input from CODEC.
C_DOUT	75	Output	Data output to CODEC.
C_CLOCK	73	Output	CODEC clock (2.048 MHz)
C_ENA0	72	Output	CODEC 0 enable (8 kHz)
C_ENA1	71	Output	CODEC 1 enable (8 kHz)
PWM	56	Output	Pulse Width Modulator output
DATA0	26	Input/Output	Data 0 I/O of the ARAM Interface
DATA1	27	Input/Output	Data 1 I/O of the ARAM Interface
DATA2	28	Input/Output	Data 2 I/O of the ARAM Interface
DATA3	29	Input/Output	Data 3 I/O of the ARAM Interface
ADDR0	13	Output	Address 0 line of the ARAM Interface
ADDR1	14	Output	Address 1 line of the ARAM Interface
ADDR2	15	Output	Address 2 line of the ARAM Interface
ADDR3	16	Output	Address 3 line of the ARAM Interface
ADDR4	17	Output	Address 4 line of the ARAM Interface
ADDR5	18	Output	Address 5 line of the ARAM Interface
ADDR6	19	Output	Address 6 line of the ARAM Interface
ADDR7	20	Output	Address 7 line of the ARAM Interface
ADDR8	21	Output	Address 8 line of the ARAM Interface
ADDR9	22	Output	Address 9 line of the ARAM Interface
ADDR10	23	Output	Address 10 line of the ARAM Interface for 4 Meg ARAMs. Select 2 output of ARAM Interface for 1 Meg ARAMs support. The latter mode is used to switch between different pages of ARAM.
ARAM_SEL0	24	Output	Select 0 output of ARAM Interface. Used to switch between different pages of ARAM.
ARAM_SEL1	25	Output	Select 1 output of ARAM Interface. Used to switch between different pages of ARAM.
/RAS	30	Output	Row Address Strobe of ARAM Interface.
/CAS	31	Output	Column Address Strobe of ARAM Interface.
ARAM_R/W	34	Output	Read/Write Strobe of ARAM Interface.
ARAM_/OE	33	Output	Output Enable Strobe of ARAM Interface.
XTAL1	11	Input	24.57 MHz crystal input
XTAL2	10	Output	24.57 MHz crystal output
/Reset	35	Input	/RESET input
R/W	50	Output	Z8® external memory interface R/W output
/AS	64	Output	Z8 external memory interface /AS output
/DS	1	Output	Z8 external memory interface /DS output

PIN DESCRIPTION (Continued)



Z89167/169 84-Pin PLCC Pin Identification

PIN DESCRIPTION (Continued)

Z89169/Z89167 84-Pin PLCC, Pin Identification

I/O Port Functions	Pin Number	I/O	Function
V_{SS}	32, 54, 65		Digital Ground
V_{CC}	12, 44, 74		Digital VCC = +5 V
P00-P07	43-36	Input/Output	P00-P07 (General-purpose nibble programmable I/O port.)
P10-P17	55, 53-51, 49-46	Input/Output	P10-P17 (General-purpose byte programmable I/O port.)
P20-P27	2-9	Input/Output	P20-P27 (General-purpose bit programmable I/O.)
P31-P37	57-63	Input/Output	P31-P37 (General-purpose I/O port. Bits P31-P33 are inputs, while bits P34-P37 are outputs.)
P40-P47	77-84	Input/Output	P40-P47 (General-purpose bit programmable I/O.)
P50-P53	70-67	Input/Output	P50-P53 (General-purpose bit programmable I/O.)
C_DIN	76	Input	Data input from CODEC.
C_DOUT	75	Output	Data output to CODEC.
C_CLOCK	73	Output	CODEC clock (2.048 MHz)
C_ENA0	72	Output	CODEC 0 enable (8 kHz)
C_ENA1	71	Output	CODEC 1 enable (8 kHz)
PWM	56	Output	Pulse Width Modulator output
DATA0	26	Input/Output	Data 0 I/O of the ARAM Interface
DATA1	27	Input/Output	Data 1 I/O of the ARAM Interface
DATA2	28	Input/Output	Data 2 I/O of the ARAM Interface
DATA3	29	Input/Output	Data 3 I/O of the ARAM Interface
ADDR0	13	Output	Address 0 line of the ARAM Interface
ADDR1	14	Output	Address 1 line of the ARAM Interface
ADDR2	15	Output	Address 2 line of the ARAM Interface
ADDR3	16	Output	Address 3 line of the ARAM Interface
ADDR4	17	Output	Address 4 line of the ARAM Interface
ADDR5	18	Output	Address 5 line of the ARAM Interface
ADDR6	19	Output	Address 6 line of the ARAM Interface
ADDR7	20	Output	Address 7 line of the ARAM Interface
ADDR8	21	Output	Address 8 line of the ARAM Interface
ADDR9	22	Output	Address 9 line of the ARAM Interface
ADDR10	23	Output	Address 10 line of the ARAM Interface for 4 Meg ARAMs. Select 2 output of ARAM Interface for 1 Meg ARAMs support. The latter mode is used to switch between different pages of ARAM.
ARAM_SEL0	24	Output	Select 0 output of ARAM Interface. Used to switch between different pages of ARAM.
ARAM_SEL1	25	Output	Select 1 output of ARAM Interface. Used to switch between different pages of ARAM.
/RAS	30	Output	Row Address Strobe of ARAM Interface.
/CAS	31	Output	Column Address Strobe of ARAM Interface.
ARAM_R/W	34	Output	Read/Write Strobe of ARAM Interface.
ARAM_/OE	33	Output	Output Enable Strobe of ARAM Interface.
XTAL1	11	Input	24.57 MHz crystal input
XTAL2	10	Output	24.57 MHz crystal output
ROMLESS	45	Input	Z8® Romless mode input (P0 and P1 are switched to D/A mode if this pin is connected to VCC). Internally this pin is tight to GND.
/Reset	35	InputOutput	/RESET input/output
R/W	50	Output	Z8 external memory interface R/W output
/AS	64	Output	Z8 external memory interface /AS output
/DS	1	Output	Z8 external memory interface /DS output

ABSOLUTE MAXIMUM RATINGS

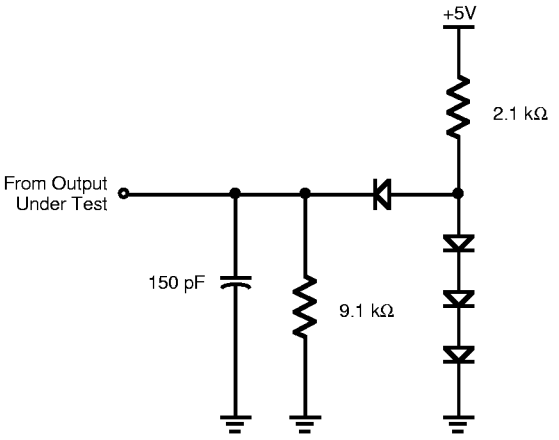
Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage (*)	–0.3	+7.0	V
T_{STG}	Storage Temp	–65°	+150°	C
T_A	Oper Ambient Temp		†	C
	Power Dissipation		2.2	W

Notes:
* Voltage on all pins with respect to GND.
† See Ordering Information.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Test Load Diagram).



Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins to GND.

Parameter	Max
Input capacitance	12 pF
Output capacitance	12 pF
I/O capacitance	12 pF

DC ELECTRICAL CHARACTERISTICS

Sym	Parameter	V_{CC} Note [1]	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Notes
I_{CC}	Supply Current	5.0 V		65	40	mA	
I_{CC1}	Halt Mode Current	5.0 V		20	6	mA	
I_{CC2}	Stop Mode Current						[2]

Notes:
[1] 5.0V ± 0.5V.
[2] The typical Stop Mode Current value is 500 µA. The transient characteristics of the Stop Mode Current will vary according to the application and should be validated in the specific application by the customer.

DC ELECTRICAL CHARACTERISTICS
Z89165/Z89166

Sym	Parameter	V_{CC} Note [1]	T_A = 0° C to +70° Min	Max	Typical @ 25°C	Units	Conditions
V_{MAX}	Max Input Voltage	5.0V		7		V	I_{IN} = 250 µA
V_{CH}	Clock Input High Voltage	5.0V	0.9 V_{CC}	V_{CC}+0.3	2.5	V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	5.0V	GND-0.3	0.1 V_{CC}	1.5	V	Driven by External Clock Generator
V_{IH}	Input High Voltage	5.0V	0.7 V_{CC}	V_{CC}+0.3	2.5	V	
V_{IL}	Input Low Voltage	5.0V	GND-0.3	0.2 V_{CC}	1.5	V	
V_{OH}	Output High Voltage	5.0V	V_{CC}-0.4		4.8	V	I_{OH} = -2.0 mA (Does not include XTAL2)
V_{OL1}	Output Low Voltage	5.0V		0.4	0.1	V	I_{OH} = +4.0 mA
V_{OL2}	Output Low Voltage (Does not include XTAL2)	5.0V		1.2	0.3	V	I_{OL} = +12 mA, 3 Pin Max
V_{RH}	Reset Input High Voltage	5.0V	0.8 V_{CC}	V_{CC}	2.1	V	
V_{RI}	Reset Input Low Voltage	5.0V	GND-0.3	0.2 V_{CC}	1.7	V	
V_{OFFSET}	Comparator Input Offset Voltage	5.0V		25	10	mV	
I_{IL}	Input Leakage	5.0V	-5	5	<5	µA	V_{IN} = OV, V_{CC}
I_{OL}	Output Leakage	5.0V	-5	5	<5	µA	V_{IN} = OV, V_{CC}
I_{IR}	Reset Input Current	5.0V		-55	-30	µA	

Notes:
[1] 5.0 ± 10% (V).

Z891650A ADDITIONAL DC ELECTRICAL CHARACTERISTICS

1. A/D CONVERTER: ABSOLUTE INPUT CURRENT VALUES

Symbol	Parameter	Maximum	Notes	
I_{il}	Anin	40 µA		
I_{ih}	Anin	2 µA		
I_{input}	Vref+	1.1 mA	With Vref– = 0V	Vref+ = 5.5V
		80 µA	With Vref– = Vref+	Vref+ = 5.5V
I_{input}	Vref–	1.1 mA	With Vref+ = 5.5V	Vref– = 0V
		80 µA	With Vref+ = Vref+	Vref– = 0V

The following parameters should be verified on the ATE under these conditions: 5.5V @ 25°C.

2. OTHER PINS

Pin Under Test	Value	Additional	Condition
Romless Pin			
I_{ih}(max) =	6 µA	No Reset	
I_{il}(max) =	6 µA	No Reset	
I_{ih}(max) =	1mA	During Reset	
XTAL1			
I_{ih}(max) =	30 µA	While XTAL2 = 0V	No Reset
I_{il}(max) =	30 µA	While XTAL2 = 5.5V	No Reset
XTAL2			
I_{ih}(max) =	10 µA	While XTAL1 = 0V	Stop Mode Invoked
I_{il}(max) =	10 µA	While XTAL2 = 5V	Stop Mode Invoked
I_{ih}(max) =	1 mA	While XTAL1 = 0V	No Reset
I_{il}(max) =	1 mA	While XTAL2 = 5V	No Reset
I_{ih}(max) =	4 mA	While XTAL1 = 0V	During Reset
I_{il}(max) =	4 mA	While XTAL2 = 5V	During Reset
I_{OL}(min) =	2 mA	V_{OL} = 1V	V_{DD} = 4.5V Temp = 70°C
I_{OH}(min) =	-1mA	V_{OH} = V_{DD} -1V	V_{DD} = 4.5V Temp = 70°C
I_{OL}(max) =	7 mA	V_{OL} = 1V	V_{DD} = 5.5V Temp = 0°C
I_{OH}(max) =	6mA	V_{OH} = V_{DD} -1V	V_{DD} = 5.5V Temp = 0°C
P31, P32, P33			
I_{ih}(max) =	1 µA		
(max) =	1 µA		

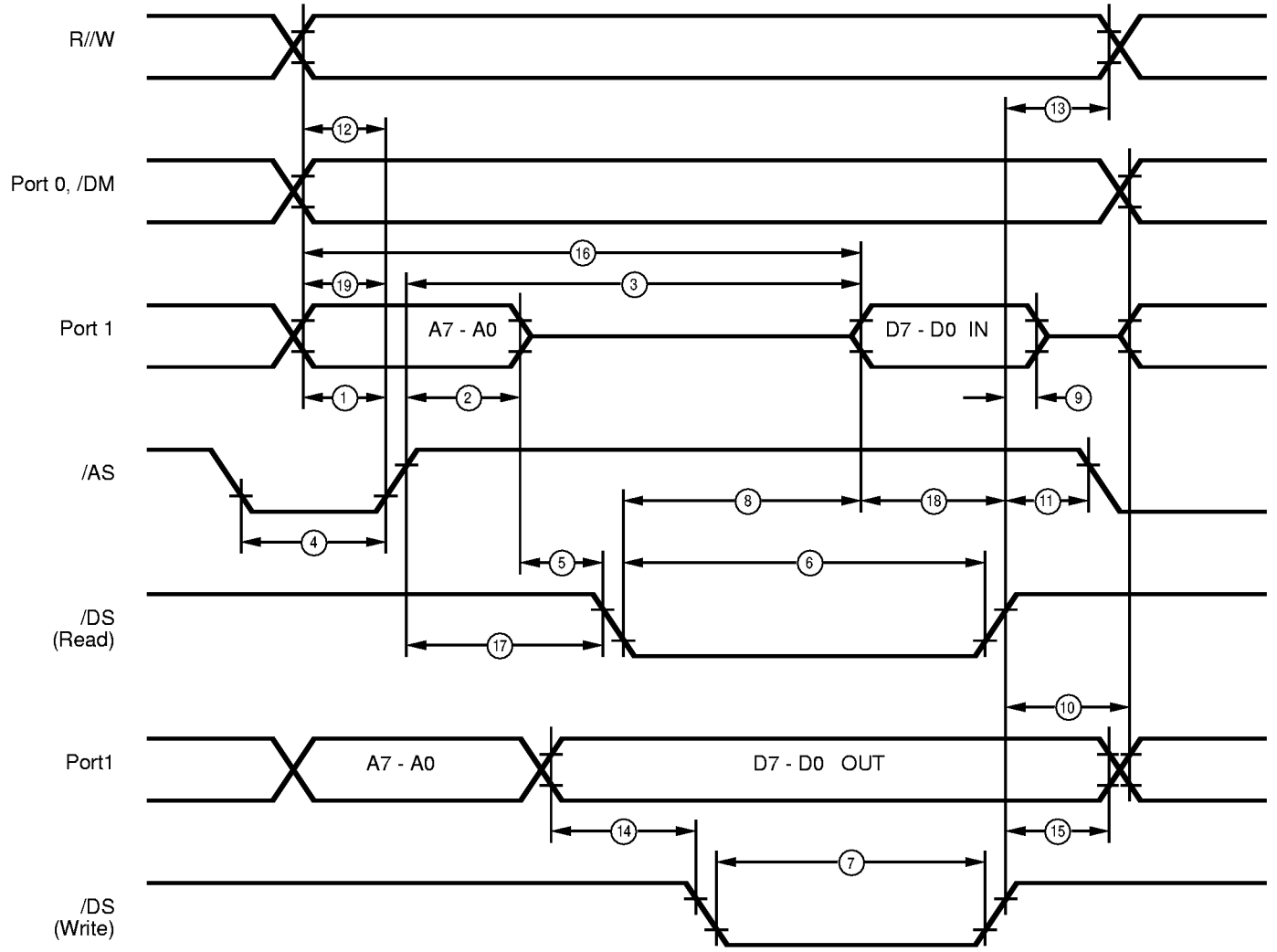
DC ELECTRICAL CHARACTERISTICS
Z89167/168/169

Sym	Parameter	V_{CC}	T_A = 0° C to +70°C Min	Max	Typical 25°C	Units at	Conditions	Notes
	Max Input Voltage	4.5V		7		V	I_{IN} 250 uA	
		5.5V		7		V	I_{IN} 250 uA	
V_{CH}	Clock Input High Voltage	4.5V	0.9 V_{CC}	V_{CC}+0.3	1.3	V	Driven by External Clock Generator	
		5.5V	0.9 V_{CC}	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	4.5V	GND-0.3	0.1 V_{CC}	0.7	V	Driven by External Clock Generator	
		5.5V	GND-0.3	0.1 V_{CC}	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	4.5V	0.7 V_{CC}	V_{CC}+0.3	1.3	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V		
V_{IL}	Input Low Voltage	4.5V	GND-0.3	0.2 V_{CC}	0.7	V		
		5.5V	GND-0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltge	4.5V	V_{CC}-0.4		3.1	V	I_{OH} = -2.0 mA	[1]
		5.5V	V_{CC}-0.4		4.8	V	I_{OH} = -2.0 mA	
V_{OL1}	Output Low Voltage	4.5V	0.6		0.2	V	I_{OH} = +4.0 mA	
		5.5V	0.4		0.1	V	I_{OL} = +4.0 mA	
V_{OL2}	Output Low Voltage	4.5V	1.2		0.3	V	I_{OL} = +6 mA, 3 Pin Max	
		5.5V	1.2		0.3	V	I_{OL} = +12 mA, 3 Pin Max	
V_{RH}	Reset Input High Voltage	4.5V	.8 V_{CC}	V_{CC}	1.5	V		
		5.5V	.8 V_{CC}	V_{CC}	2.1	V		
V_{RI}	Reset Input Low Voltage	4.5V	GND-0.3	0.2 V_{CC}	1.1			
		5.5V	GND-0.3	0.2 V_{CC}	1.7			
V_{OFFSET}	Comparator Input Offset	4.5V		25	10	mV		
	Voltage	5.5V		25	10	mV		
I_{IL}	Input Leakage	4.5V	-5	5	<5	µA	V_{IN} = OV, V_{CC}	
		5.5V	-5	5	<5	µA	V_{IN} = OV, V_{CC}	
I_{OL}	Output Leakage	4.5V	-5	5	<5	µA	V_{IN} = OV, V_{CC}	
		5.5V	-5	5	<5	µA	V_{IN} = OV, V_{CC}	
I_{IR}	Reset Input Current	4.5V		-45	-20	µA		
		5.5V		-55	-30	µA		

Note:
[1] P10, P11 are measured at 4.5V only.

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Diagram



External I/O or Memory Read/Write Timing

AC CHARACTERISTICS
Z89165/166
External I/O or Memory Read and Write Timing Table

No	Symbol	Parameter	V_{CC} Note [4]	T_A=0°C to +70°C Min	Max	Units	Notes
1	TdA(AS)	Address Valid to /AS Rise Delay	5.0V	25		ns	[2,3]
2	TdAS(A)	/AS Rise to Address Float Delay	5.0V	35		ns	[2,3]
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid	5.0V		150	ns	[1,2,3]
4	TwAS	/AS Low Width	5.0V	35		ns	[2,3]
5	TdAZ(DS)	Address Float to /DS Fall	5.0V	-3		ns	
6	TwDSR	/DS (Read) Low Width	5.0V	125		ns	[1,2,3]
7	TwDSW	/DS (Write) Low Width	5.0V	75		ns	[1,2,3]
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid	5.0V		90	ns	[1,2,3]
9	ThDR(DS)	Read Data to /DS Rise Hold Time	5.0V	0		ns	[2,3]
10	TdDS(A)	/DS Rise to Address Active Delay	5.0V	40		ns	[2,3]
11	TdDS(AS)	/DS Rise to /AS Fall Delay	5.0V	35		ns	[2,3]
12	TdR/W(AS)	R/W Valid to /AS Rise Delay	5.0V	25		ns	[2,3]
13	TdDS(R/W)	/DS Rise to R/W Not Valid	5.0V	35		ns	[2,3]
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	5.0V	40		ns	[2,3]
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	5.0V	25		ns	[2,3]
16	TdA(DR)	Address Valid to Read Data Req'd Valid	5.0V		180	ns	[1,2,3]
17	TdAS(DS)	/AS Rise to /DS Fall Delay	5.0V	48		ns	[2,3]
18	TdDI(DS)	Data Input Setup to /DS Rise	5.0V	50		ns	[1,2,3]
19	TdDM(AS)	/DM Valid to /AS Fall Delay	5.0V	20		ns	[2,3]

Notes:
[1] When using extended memory timing add 2 TpC.
[2] Timing numbers given are for minimum TpC.
[3] See clock cycle dependent characteristics table.
[4] 5.0 V ± 0.5 V.

Standard Test Load
All timing references use 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.

AC CHARACTERISTICS
Z89167/168/169
External I/O or Memory Read and Write Timing Table

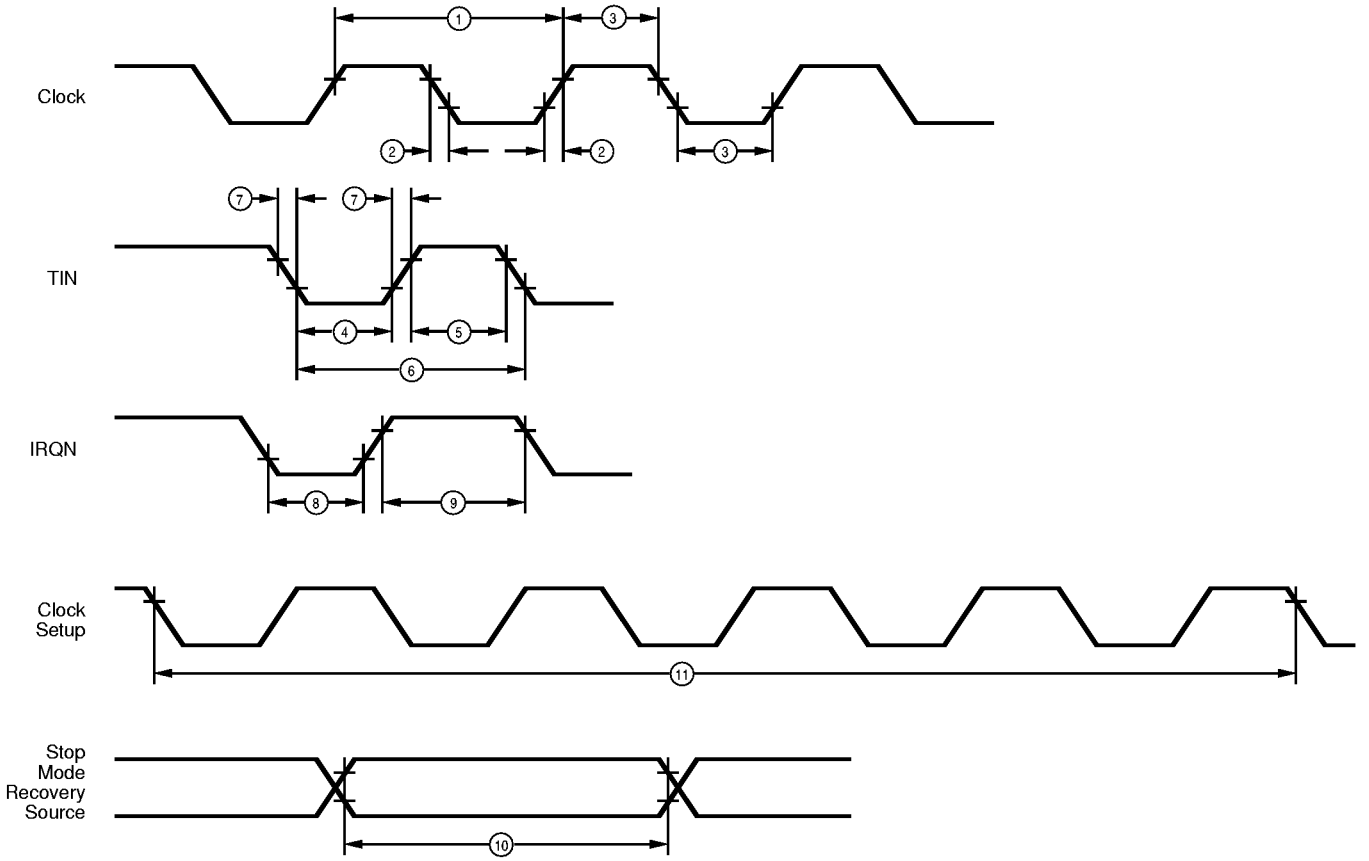
No	Symbol	Parameter	V_{CC} Note [4]	T_A=0°C to +70°C Min	Max	Units	Notes
1	TdA(AS)	Address Valid to /AS Rise Delay	5.0V	18		ns	[2,3]
2	TdAS(A)	/AS Rise to Address Float Delay	5.0V	22		ns	[2,3]
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid	5.0V		130	ns	[1,2,3]
4	TwAS	/AS Low Width	5.0V	28		ns	[2,3]
5	TdAZ(DS)	Address Float to /DS Fall	5.0V	0		ns	
6	TwDSR	/DS (Read) Low Width	5.0V	90		ns	[1,2,3]
7	TwDSW	/DS (Write) Low Width	5.0V	62		ns	[1,2,3]
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid	5.0V		55	ns	[1,2,3]
9	ThDR(DS)	Read Data to /DS Rise Hold Time	5.0V	0		ns	[2,3]
10	TdDS(A)	/DS Rise to Address Active Delay	5.0V	36		ns	[2,3]
11	TdDS(AS)	/DS Rise to /AS Fall Delay	5.0V	25		ns	[2,3]
12	TdR/W(AS)	R/W Valid to /AS Rise Delay	5.0V	18		ns	[2,3]
13	TdDS(R/W)	/DS Rise to R/W Not Valid	5.0V	22		ns	[2,3]
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	5.0V	18		ns	[2,3]
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	5.0V	23		ns	[2,3]
16	TdA(DR)	Address Valid to Read Data Req'd Valid	5.0V		160	ns	[1,2,3]
17	TdAS(DS)	/AS Rise to /DS Fall Delay	5.0V	32		ns	[2,3]
18	TdDI(DS)	Data Input Setup to /DS Rise	5.0V	28		ns	[1,2,3]
19	TdDM(AS)	/DM Valid to /AS Fall Delay	5.0V	18		ns	[2,3]

Notes:
[1] When using extended memory timing add 2 TpC.
[2] Timing numbers given are for minimum TpC.
[3] See clock cycle dependent characteristics table.
[4] 5.0 V ± 0.5 V.

Standard Test Load
All timing references use 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.

AC ELECTRICAL CHARACTERISTICS

Additional Timing Diagram



Additional Timing

AC ELECTRICAL CHARACTERISTICS
Z89165/166
Additional Timing Table

No	Symbol	Parameter	V_{CC} Note [6]	T_A=0°C to +70°C Min	Max	Units	Notes
1	TpC	Input Clock Period	5.0 V	48.83		ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times	5.0 V		6	ns	[1]
3	TwC	Input Clock Width	5.0 V	17		ns	[1]
4	TwTinL	Timer Input Low Width	5.0 V	70		ns	
5	TwTinH	Timer Input High Width	5.0 V	3TpC			[1]
6	TpTin	Timer Input Period	5.0 V	8TpC			[1]
7	TrTin, TfTin	Timer Input Rise & Fall Timer	5.0 V		100	ns	[1]
8A	TwIL	Int. Request Low Time	5.0 V	70		ns	[1,2]
8B	TwIL	Int. Request Low Time	5.0 V	3TpC			[1]
9	TwIH	Int. Request Input High Time	5.0 V	3TpC			[1]
10	Twsm	Stop-Mode Recovery Width Spec	5.0 V	12 5TpC		ns	[1]
11	Tost	Oscillator Startup Time	5.0 V	5TpC			[3]
12	Twdt	Watch-Dog Timer	5.0 V	3		ms	D1=0, D0 = 0 [4]
			5.0 V	6		ms	D1=0, D0 = 1 [4]
			5.0 V	12		ms	D1=1, D0 = 0 [4]
			5.0 V	50		ms	D1=1, D0 = 1 [4]

Notes:
[1] Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
[2] Interrupt request via Port 3 (P31-P33).
[3] SMR-D5 = 0.
[4] Reg. WDT.
[5] 5.0V ± 0.5V.

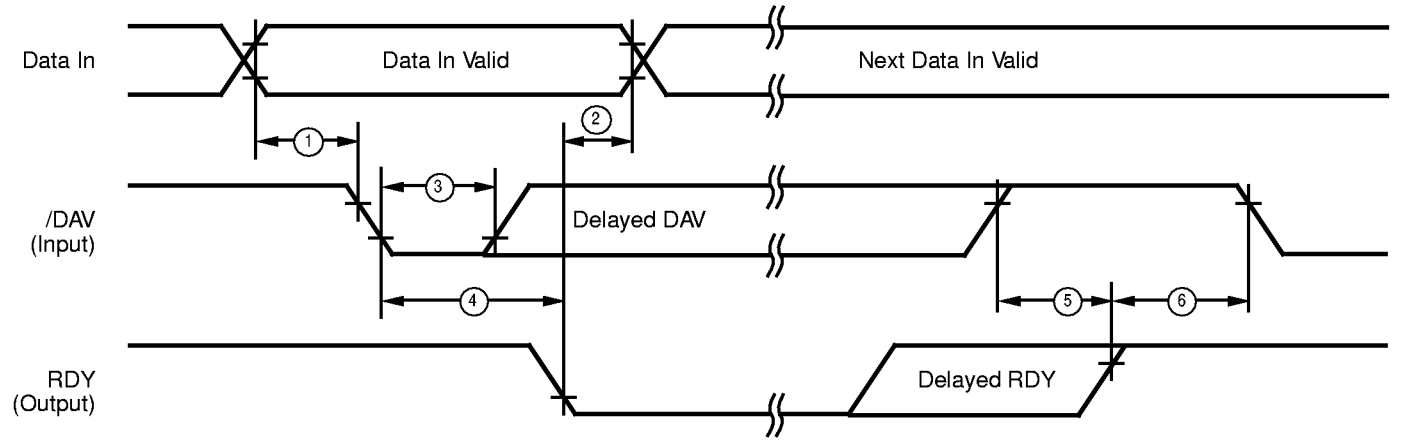
AC ELECTRICAL CHARACTERISTICS
Z89167/168/169
Additional Timing Table

No	Symbol	Parameter	V_{CC} Note [5]	T_A=0°C to +70°C Min	Max	Units	Notes
1	TpC	Input Clock Period	5.0 V	41.67		ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times	5.0 V		6	ns	[1]
3	TwC	Input Clock Width	5.0 V	16		ns	[1]
4	TwTinL	Timer Input Low Width	5.0 V	70		ns	
5	TwTinH	Timer Input High Width	5.0 V	3TpC			[1]
6	TpTin	Timer Input Period	5.0 V	8TpC			[1]
7	TrTin, TfTin	Timer Input Rise & Fall Timer	5.0 V		100	ns	[1]
8A	TwIL	Int. Request Low Time	5.0 V	70		ns	[1,2]
8B	TwIL	Int. Request Low Time	5.0 V	3TpC			[1]
9	TwIH	Int. Request Input High Time	5.0 V	3TpC			[1]
10	Twsm	Stop-Mode Recovery Width Spec	5.0 V	12 5TpC		ns	[1]
11	Tost	Oscillator Startup Time	5.0 V	5TpC			[3]
12	Twdt	Watch-Dog Timer	5.0 V	5		ms	D1=0, D0 = 0 [4]
			5.0 V	15		ms	D1=0, D0 = 1 [4]
			5.0 V	25		ms	D1=1, D0 = 0 [4]
			5.0 V	100		ms	D1=1, D0 = 1 [4]

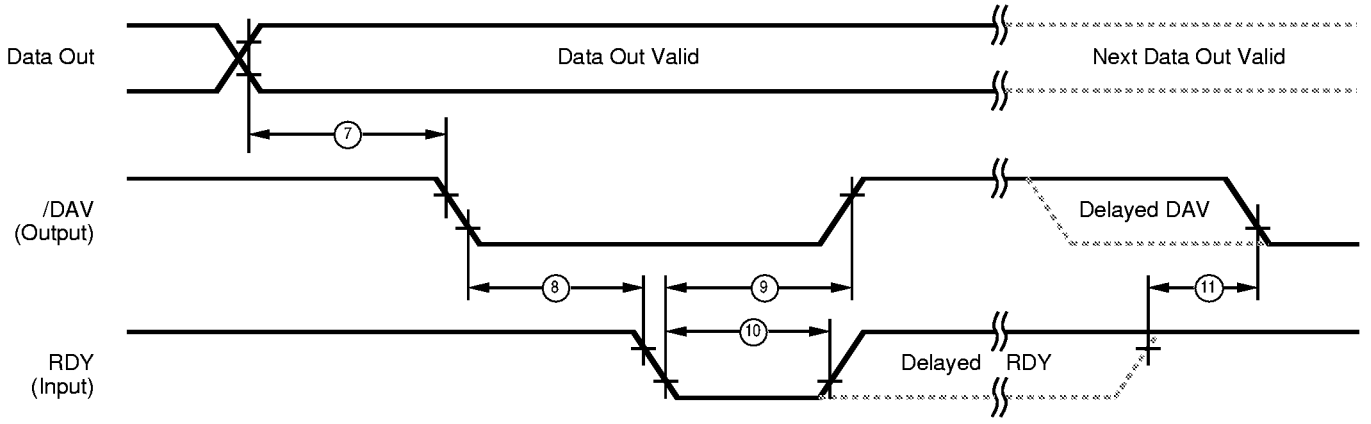
Notes:
[1] Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
[2] Interrupt request via Port 3 (P31-P33).
[3] SMR-D5 = 0.
[4] Reg. WDT.
[5] 5.0V ± 0.5V.

AC ELECTRICAL CHARACTERISTICS

Handshake Timing Diagrams



Input Handshake Timing



Output Handshake Timing

AC ELECTRICAL CHARACTERISTICS
Z89165/166
Handshake Timing Table

No	Symbol	Parameter	V_{CC} Note [1]	T_A=0°C to +70°C Min	Max	Units	Data Direction
1	TsDI(DAV)	Data In Setup Time	5.0 V	0		ns	IN
2	ThDI(RDY)	RDY to Data Hold Time	5.0 V	0		ns	IN
3	TwDAV	Data Available Width	5.0 V	40		ns	IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay	5.0 V		70	ns	IN
5	TdDAVId(RDY)	DAV Rise to RDY Rise Delay	5.0 V		40	ns	IN
6	TdDO(DAV)	RDY Rise to DAV Fall Delay	5.0 V	0		ns	IN
7	TcLDAV0(RDY)	Data Out to DAV Fall Delay	5.0 V	TpC		ns	OUT
8	TcLDAV0(RDY)	DAV Fall to RDY Fall Delay	5.0 V	0		ns	OUT
9	TdRDY0(DAV)	RDY Fall to DAV Rise Delay	5.0 V		70	ns	OUT
10	TwRDY	RDY Width	5.0 V	40		ns	OUT
11	TdRDY0d(DAV)	RDY Rise to DAV Fall Delay	5.0 V		40	ns	OUT

Notes:
[1] 5.0 V ± 0.5 V

AC ELECTRICAL CHARACTERISTICS
Z89167/168/169
Handshake Timing Table

No	Symbol	Parameter	V_{CC} Note [1]	T_A=0°C to +70°C Min	Max	Units	Data Direction
1	TsDI(DAV)	Data In Setup Time	5.0 V	0		ns	IN
2	ThDI(RDY)	Ready to Data In Hold Time	5.0 V	0		ns	IN
3	TwDAV	Data Available Width	5.0 V	110		ns	IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay	5.0 V		115	ns	IN
5	TdDAVId(RDY)	DAV Rise to RDY Rise Delay	5.0 V		80	ns	IN
6	TdDO(DAV)	RDY Rise to DAV Fall Delay	5.0 V	0		ns	IN
7	TcLDAV0(RDY)	Data Out to DAV Fall Delay	5.0 V	25		ns	OUT
8	TcLDAV0(RDY)	DAV Fall to RDY Fall Delay	5.0 V	0		ns	OUT
9	TdRDY0(DAV)	RDY Fall to DAV Rise Delay	5.0 V		115	ns	OUT
10	TwRDY	RDY Width	5.0 V	80		ns	OUT
11	TdRDY0d(DAV)	RDY Rise to DAV Fall Delay	5.0 V		80	ns	OUT

Notes:
[1] 5.0 V ± 0.5 V

ELECTRICAL CHARACTERISTICS
Z89165/166 A/D CONVERTER

A/D Converter Electrical Characteristics

V_{CC} = 5.0V ± 10%

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.5	1	LSB
Differential non-linearity		0.5	1	LSB
Zero Error at 25°C			250	mV
Supply Range	4.5	5.0	5.5	Volts
Input voltage range	VA_{LO}		VA_{HI}	Volts
Conversion time			2	µsec
Input capacitance on ANA	25		60	pF
VA_{HI} range	VA_{LO}+2.5		AV_{CC}	Volts
VA_{LO} range	AN_{GND}		AV_{CC}–2.5	Volts
VA_{HI} --VA_{LO}	2.5		AV_{CC}	Volts

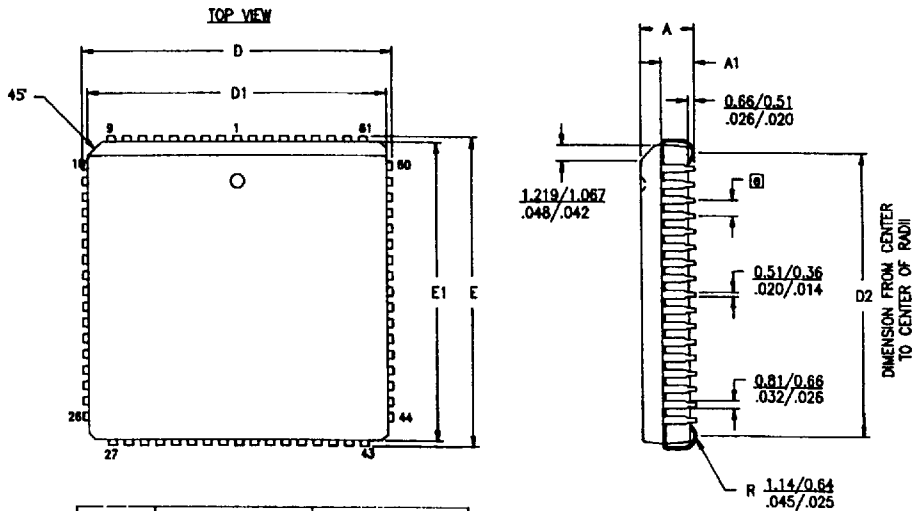
Notes:
Voltage 4.5V –5.5V
Temp 0-70°C

Zilog, Inc. 210 East Hacienda Ave.
Campbell, CA 95008-6600
Telephone (408) 370-8000
Telex 910-338-7621
FAX 408 370-8056
Internet: http://www.zilog.com

PACKAGE INFORMATION

PLCC (Plastic Leaded Chip Carrier) (Continued)

1. Solderability — MIL-STD-883C Method 2003.5
   Eight Hours Steam Age
2. Mark Permanency — 3X soak into Alpha 2110 at 63-70°C.
   30 sec. duration each soak.
   Mech. brush after each soak
3. Coplanarity — Maximum 4 mils deviation



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.32	4.57	.170	.180
A1	2.43	2.92	.095	.115
D/E	25.02	25.40	.985	1.000
D1/E1	24.13	24.33	.950	.958
D2	22.86	23.62	.900	.930
e	1.27 TYP		.050 TYP	

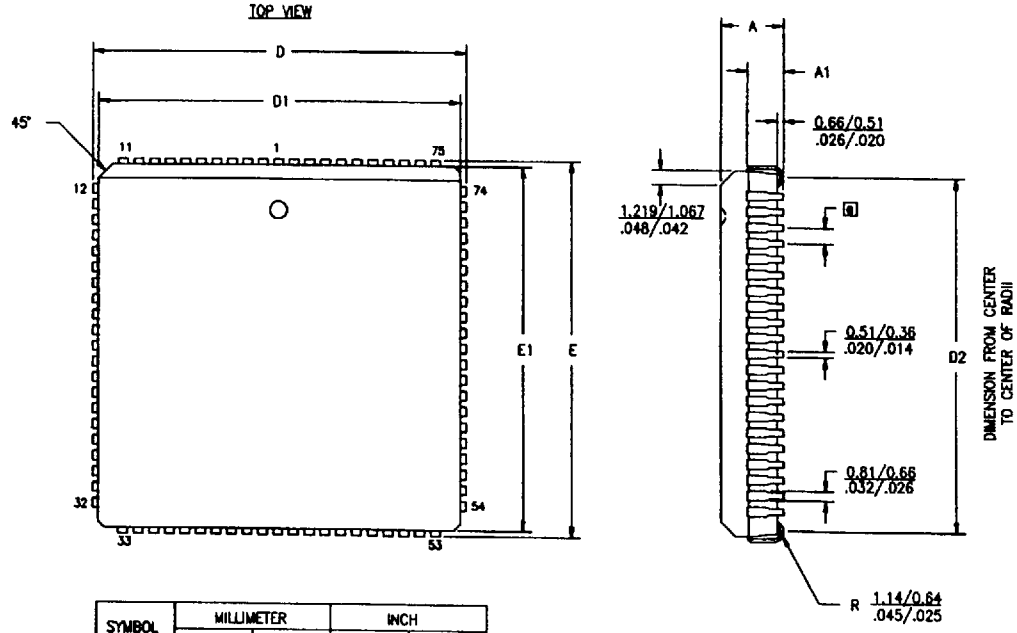
NOTES:
1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN RANGE.
3. DIMENSION : MM / INCH

68-Lead Plastic Leaded Chip Carrier (PLCC)

PACKAGE INFORMATION

PLCC (Plastic Leaded Chip Carrier) (Continued)

1. Solderability	MIL-STD-883C Method 2003.5 Eight Hours Steam Age
2. Mark Permanency	3X soak into Alpha 2110 at 63-70°C. 30 sec. duration each soak. Mech. brush after each soak
3. Coplanarity	Maximum 4 mils deviation



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.32	4.57	.170	.180
A1	2.43	2.92	.095	.115
D/E	30.10	30.35	1.185	1.195
D1/E1	29.21	29.41	1.150	1.158
D2	27.94	28.58	1.100	1.125
e	1.27 TYP		.050 TYP	

NOTES:
1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN RANGE.
3. DIMENSION : MM / INCH

84-Lead Plastic Leaded Chip Carrier (PLCC)